an Intel company

10 Gbit/s Receiver, CDR and DeMUX GD16544

Preliminary

General Description

GD16544 is a 9.95328 Gbit/s Receiver chip for use in SDH STM-64 and SONET OC-192 optical communication systems.

GD16544 is a Clock and Data Recovery IC with:

- an on-chip VCO
- a Bang-Bang Phase Detector
- a 1:16 De-multiplexer
- a Lock Detect
- a Phase and Frequency Detector.

Clock and data are regenerated by using GD16544 in a *Phase Lock Loop* (PLL) with an external loop filter.

The VCO frequency is controlled by two different Phase and Frequency Detectors to ensure capture and lock to the line data rate. When the frequency deviates more than ±500 ppm from the reference clock, GD16544 automatically switches the phase and frequency detector into the PLL loop. In the auto lock mode the locking range is selectable between ±500 or ±2000 ppm.

The Lock Detector circuit monitors the VCO frequency and determines when the VCO is within the locking range. If in lock it switches the Bang-Bang Phase Detector into the PLL.

When the VCO frequency is within the locking range, the Bang-Bang Phase Detector takes over. It controls the phase of the VCO until the sampling point of data is in the middle of the bit period, where the eye opening is largest. A ± 40 mV *Decision Threshold Control* (DTC) is provided at the 10 Gbit/s input.

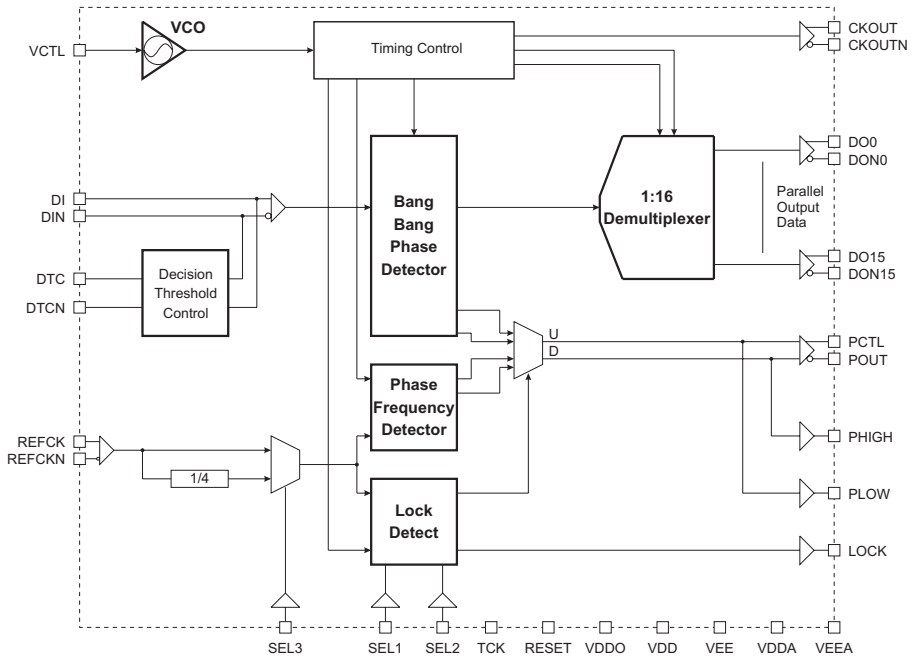
The 10 Gbit/s input data is retimed and de-multiplexed by the 1:16 DeMUX. The parallel output interface is synchronised with the 622 MHz output clock.

GD16544 is manufactured in a Silicon Bipolar process.

GD16544 uses a single -5.2 V supply voltage.

The power dissipation is 2.9 W typical.

GD16544 is delivered in a *Multi Layer Ceramic* (MLC) package, with internal high-speed 50 Ω transmission lines.



Features

- Complete Clock and Data Recovery IC with auto acquisition.
- Low noise 10 GHz VCO with ±5 % tuning range.
- Digital controlled lock to data by a Bang-Bang Phase Detector.
- Automatic capture of the VCO frequency by a true Phase and Frequency Detector.
- Locking range selectable between ±500 and ±2000 ppm.
- Input Decision Threshold Control (DTC): ± 40 mV.
- 1:16 DeMUX with differential 622 Mbit/s data outputs.
- Open collector clock and data outputs.
- 622 MHz Clock output.
- 155 or 622 MHz Reference Clock.
- Single supply operation: -5.2 V.
- Power dissipation: 2.9 W (typ).
- Silicon Bipolar technology.
- 68 pin Multi Layer Ceramic (MLC) package.

Applications

- Telecommunication systems:
  - SDH STM-64
  - SONET OC-192.
- Fibre optic test equipment.
- Submarine systems.

Functional Details

The application of GD16544 is as receiver in SDH STM-64 and SONET OC-192 optical communication systems.

It integrates:

- a Voltage Controlled Oscillator (VCO)
- a Clock and Data Recovery Circuit
- a Lock Detect Circuit
- a 1:16 DeMUX
- a Phase and Frequency Detector (PFD).

VCO

The VCO is an LC-type differential oscillator at 10 GHz, voltage controlled by pin VCTL and with a tuning range of approximately ±5 %.

With the VCTL voltage at approximately -3.5 V the VCO frequency is fixed at 9.953 GHz and by changing the voltage from 0 to -5.2 V the frequency is controlled from 8.9 GHz to 10.2 GHz. The modulation bandwidth of VCTL is 90 MHz (see VCO Measurement on page 14).

PFD

The PFD, ensures predictable locking conditions for the GD16544. It is used during acquisition and pulls the VCO into the locking range where the Bang-Bang Phase Detector acquires lock to the incoming bit-stream. The PFD is made with digital set/reset cells giving it a true phase and frequency characteristic. The reference clock input (REFCK/REFCKN) to the PFD is differential and selectable between 155 MHz or 622 MHz by SEL3.

The reference clock input has 50 Ω internal termination resistors to 0 V. The reference clock is typically an X-tal oscillator type as shown on Figure 1. The reference clock input should be used differential for best performance.

Bang-Bang Phase Detector

The Bang-Bang phase detector is designed as a true digital type producing a binary output. It samples the incoming data prior to, in the vicinity of and after any potential bit transition.

When a transition has occurred, these three samples tell whether the VCO clock leads or lags the data. The binary output is filtered through the (low pass) loop filter, performing an integration of all potential bit transitions. Hence the PLL is controlled by the bit transition point.

Loop Filter

The external loop filter is made using a operational amplifier connected to output pin (PHIGH and PLOW). The characteristics of the phase lock loop are controlled by the loop filter components hence the op-amp is designed as an integrator by a feedback capacitor and a resistor. The gain-bandwidth of the op-amp is larger than the required PLL bandwidth in order not to limit the PLL. The recommended op-amp is Analog Devices (AD8042) with a gain-bandwidth of 160 MHz sufficient for PLL bandwidth up to 50 MHz. The op-amp is used single supplied by –5.2 V. See Figure 1 for application information.

The phase information from the Bang-Bang phase detector are very high frequency pulses (200 ps pulse width) at output pins (PHIGH and PLOW). They are open collector outputs with a 8 mA current drive and are terminated externally by 100 Ω to 0 V. A pre-filtering of the phase pulses are applied by a parallel 10 pF capacitor (see Figure 1).

The PCB layout of the external loop filter and the connecting lines to PHIGH, PLOW and VCTL are critical for the jitter performance of the component. The artwork for the op-amp and the passive components should be placed very close to the pins of GD16544 in order to have connecting lines as short as possible. Ideally the loop filter components are placed on the opposite side of the PCB directly underneath GD16544. For more layout suggestions see the 10 Gbit/s evaluation board GD90244/255.

Alternatively the phase information is also available at output pins (PCTL and POUT) and are used with an external passive loop filter in applications with a low PLL bandwidth (< 1 MHz) instead of the above recommended active loop filter. The PCTL and POUT pins should always be terminated as shown in Figure 1 also even though they are not actively used in the PLL.

POUT is a high impendance input and will be destroyed if connected directly (lowohmic, <25 kΩ) to -2.5 V to 0 V.

Lock Detect Circuit

The lock detect circuit continuously monitors the difference between the reference clock and the VCO clock. If they are apart by more than ±500 (or ±2000 ppm), it switches the PFD into the PLL, to pull it back into the locking range. The status of the lock circuit is given by output pin (LOCK). Manual or automatic lock is selected by SEL1. In auto lock mode, the lock range ±500 or ±2000 ppm is selected by SEL2.

The Inputs

The input amplifier pin (DI/DIN) is designed as a gain buffer stage with high sensitivity and internal 50 Ω resistors terminated to 0 V. After retiming, the data is de-multiplexed down to 622 Mbit/s by the 1:16 DeMUX. The input data is de-multiplexed starting with DO0, DO1...DO15 as the first received bits.

It is recommended to use the 10 Gbit/s inputs differentially.

The 10 Gbit/s inputs (DI and DIN) are not ESD protected and extra precautions are needed when handling these inputs. (Internal 50 Ω resistors provide some ESD hardness making the input low impendance.)

The input voltage decision threshold is adjustable by pin DTC and DTCN when connected to a potentiometer. Adjusting the resistor value of the meter controls the current into DTC and DTCN. This DC current is mirrored to the input pin (DI and DIN) whereby the DC bias voltage at the input is adjustable by ±40 mV. Optimizing the input decision threshold improves the system input sensitivity by 1-2 dB typical.

The input impedance into DTC and DTCN is 1.5 kΩ and when not used they should be de-coupled to 0 V by 100 nF.

The select inputs (SEL1-3, RESET and TCK) are low speed inputs that can be connected directly to the supply rails (0 / -5.2 V).

The Outputs

The data outputs, the clock output and LOCK are differential open collector outputs with an 8 mA output current. They are terminated externally with a resistor (R) to 0 V and the output voltage swing is V = -50 × 8 mA = -400 mV with R = 50 Ω. Increasing the resistor increases the output voltage and reduces the bandwidth.

The open collector outputs can be configurated as CML or ECL compatible using external circuit. (See item “622 Mbit/s Output Interface” on page 6).

When interfacing LDVS see item “Interfacing to a Positive Supply Interface Technology” on next page.

Timing

The timing between GD16544 and the system ASIC at 622 Mbit/s is controlled by the 622 MHz output clock synchronized with the output data. The clock is used as the input clock to the ASIC, clocking the input data into 16 parallel shift registers. The timing relation between clock and data is given by the AC Characteristics.

External Circuit

The external circuits needed to make GD16544 work as a complete clock and data recovery with automatic acquisition are:

- Active loop filter with op-amp
- An x-tal oscillator at 155 MHz or 622 MHz
- Pull up resistors on all outputs and de-coupling capacitors.

Package

GD16544 is packaged in a 68 pin Multi Layer Ceramic package with internal 50 Ω transmission lines. The cavity of the package is down for easy cooling with a mounted head spreader on top.

Mounting and Layout of PCB.

The component can be mounted on a standard FR4 epoxy printed circuit board when special attention is taken in the layout and in the mounting of the component.

It is important for the performance of the component that the leads of pin DI and DIN (10 Gbit/s inputs) are made very short (<1 mm) when mounted on the board. Best way to make the leads short is to cut a hole in the PCB and to mount the component inside the hole. The length of the two critical leads is reduced to less than 0.5 mm whereas the rest of the leads are kept at 2-4 mm in order for mechanical stability. On the backside the head spreader is thermally mounted to a metal block with heat sink compound (see paragraph “Mounting of Component on PCB” on page 15). In cases where the above mounting technical is not applicable, the component can be mounted directly on the board with bend leads accepting longer leads for the 10 Gbit/s inputs e.g. reduced input sensitivity and reflection.

The component is available with straight leads and with gullwing leads, see the package outline drawings.

In the layout of the printed circuit board the 10 Gbit/s inputs are connected with 50 Ω *Micro Strip Lines* (MLS) to the high-speed connector. The micro strip lines should be as short as possible (<15 mm) with a plain and solid ground plan below. The layout artwork for the loop filter is placed preferable on the opposite side of the component with very short connections to the pins of GD16544. The 100 Ω resistors and 10 pF capacitor connected from PHIGH and PLOW to 0 V should be placed very close to the package pin no. 50 and 53.

The environment around the loop filter and the 10 Gbit/s inputs is noise sensitive and no noise generating lines are allowed in this area.

The power supply to GD16544 should be separated from other noise generation components on the board and be decoupled as shown on Figure 2. DC-DC converters are only allowed on the same board if proper noise filtering is applied.

Thermal Condition

The component dissipates 2.9 W with a –5.2 V voltage supply and need forced cooling with a heat sink thermally connected to the heat spreader. The thermal connection should ensure the case temperature in the range from 0 to 70 °C with the given ambient conditions e.g. temperature and air flow etc.

Power Noise Rejection

In a noisy environment special attention must be taken as described above to optimize the jitter performance and to reduce the input sensitivity penalty from injected noise. The *Power Supply Rejection Ratio* (PSRR) is improved by adding a serial resistor (330 Ω) and capacitor (33 nF) from the positive input of the op-amp to the VEEA power pin (no. 52) as shown in Figure 1.

Interfacing to a Positive Supply Interface Technology

The data outputs (DO0-15) and the clock output (CKOUT/N) are externally terminated with top resistors. When interfacing a positive supplied interface technology (e.g. LVDS) the external resistors can be terminated directly to the positive supply.

A version of GD16544 (GD16544/HV-68XX) is offered with all data outputs and the clock output DC tested for a minimum breakdown voltage of 8 V.

The maximum allowed output voltage on all outputs is 2.6 V.

Applications

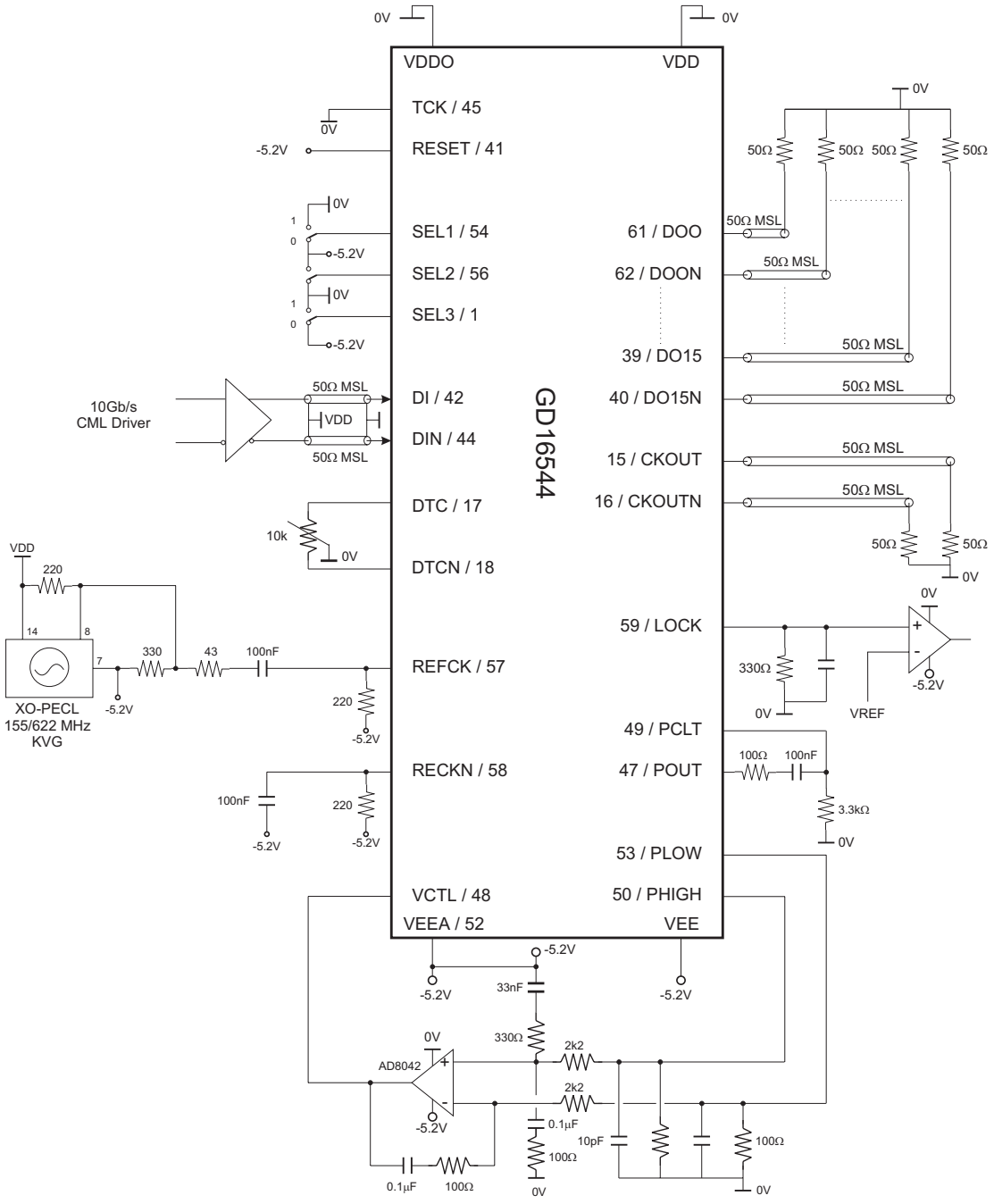
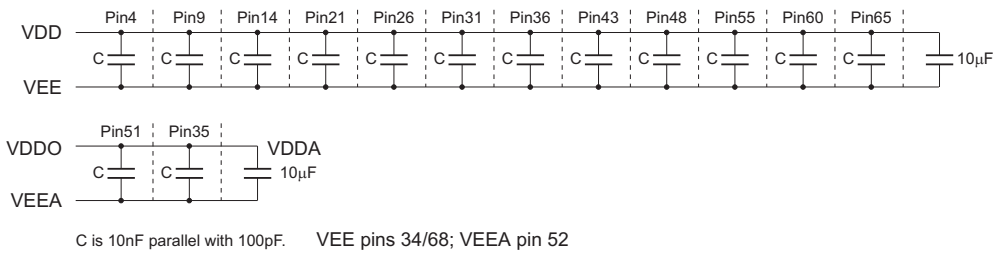


Figure 1. *Application Information.*



C is 10nF parallel with 100pF. VEE pins 34/68; VEEA pin 52

Figure 2. *De-coupling Supply.*

Applications Continued

10 Gbit/s Input Interface

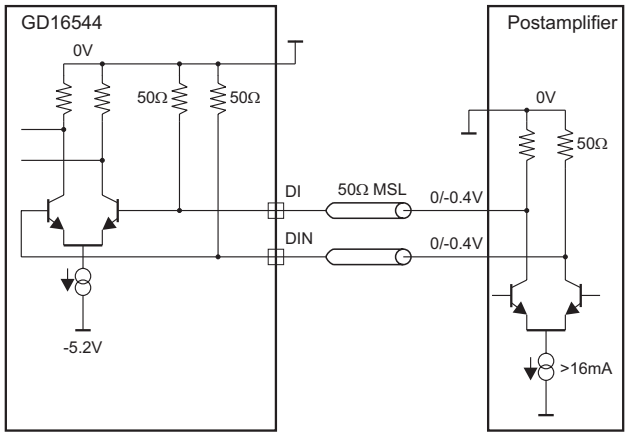


Figure 3. *10 Gbit/s Input (DI/DIN), DC Coupled*

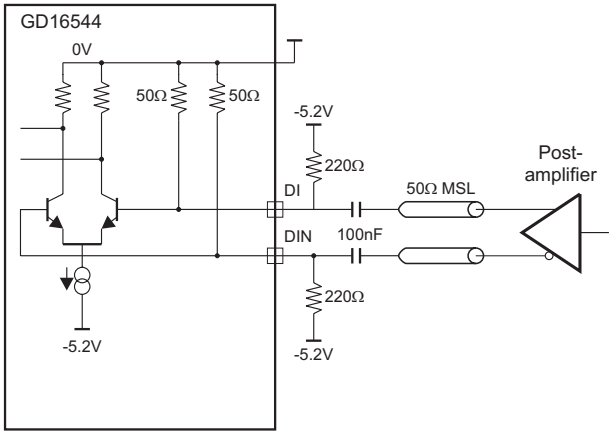


Figure 4. *10 Gbit/s Input (DI/DIN), AC Coupled*

622 Mbit/s Output Interface

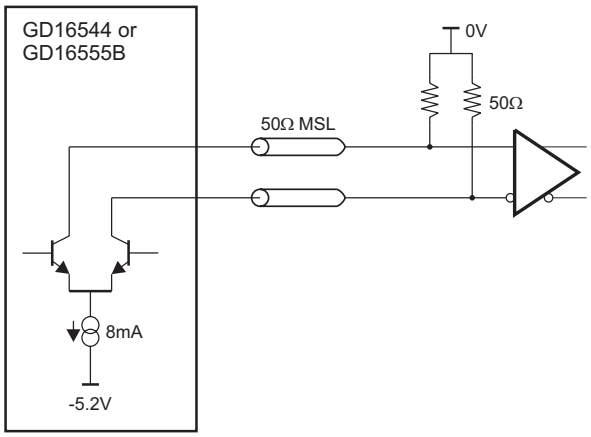


Figure 5. *Open Collector Output*

Open collector outputs should always be terminated at the receiver end, preferably 50 Ω .

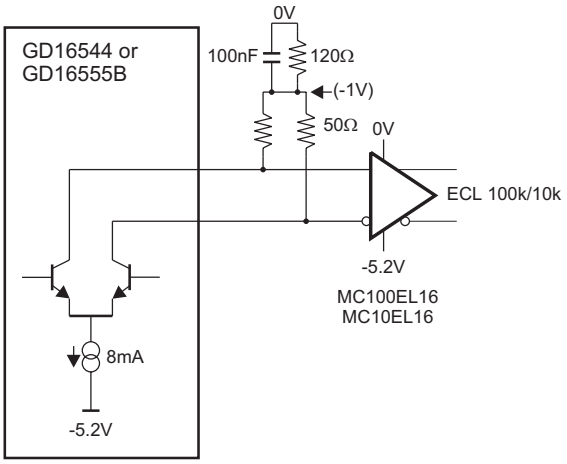


Figure 6. *ECL 100k or 10k Output.*

ECL 100k or 10k output using ECL driver MC100EL16/ MC10EL16.

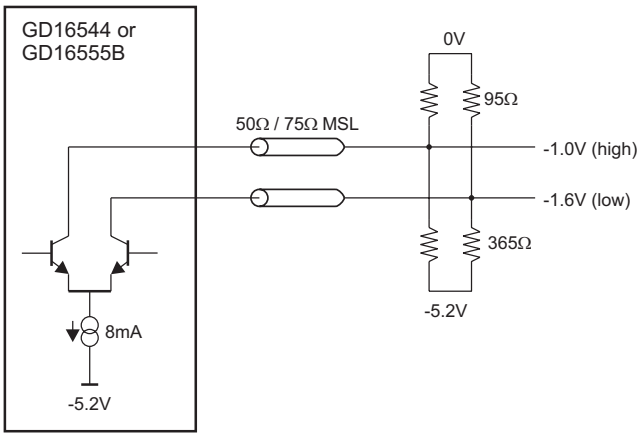


Figure 7. *ECL Compatible Output*

ECL compatible output with a voltage swing of 600 mV (single-ended) or 1200 mV (differential).

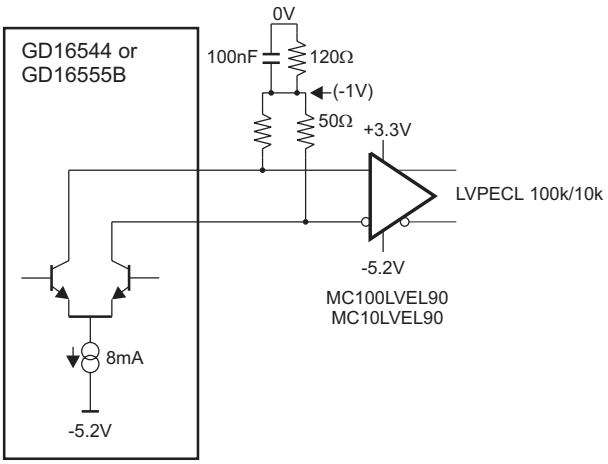


Figure 8. *Low Voltage PECL Output*

Low voltage PECL output using PECL driver MC100LVEL90/ MC10LVEL90.

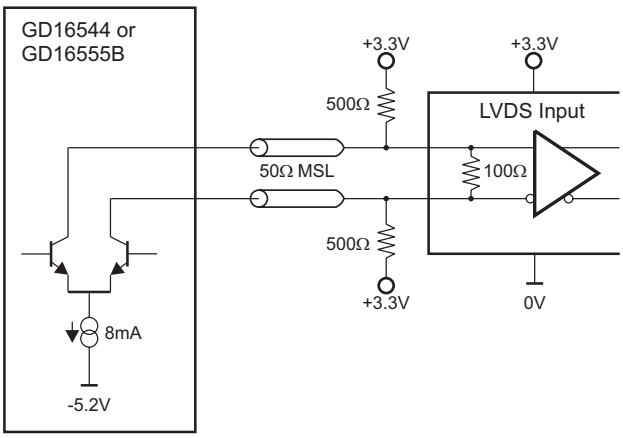


Figure 9. *LVDS Compatible Output. Only applicable with /HV version*

Reference Clock Input

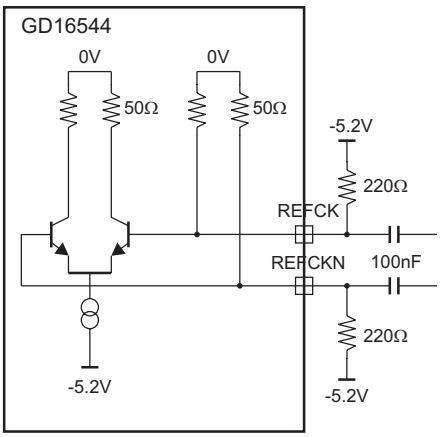


Figure 10. *Reference Clock Input (REFCK/REFCKN), Differential AC Coupled.*

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
DO0, DON0 DO1, DON1 DO2, DON2 DO3, DON3 DO4, DON4 DO5, DON5 DO6, DON6 DO7, DON7 DO8, DON8 DO9, DON9 DO10, DON10 DO11, DON11 DO12, DON12 DO13, DON13 DO14, DON14 DO15, DON15	61, 62 63, 64 66, 67 2, 3 5, 6 7, 8 10, 11 12, 13 19, 20 22, 23 24, 25 27, 28 29, 30 32, 33 36, 37 39, 40	Open Collector	Data output, differential 622 Mbit/s. Demultiplexed to output with DO0, DO1...DO15 as first received bits. All outputs should always be terminated with a resistor.
REFCK, REFCKN	57, 58	CML In	Reference clock input, differential 155 MHz or 622 MHz.
SEL1, SEL2	54, 56	ECL In	Clock and Data recovery setup. SEL1 SEL2 0 0 Auto Lock, 500 ppm. 0 1 Auto Lock, 2000 ppm. 1 0 Manual Phase Freq. Detector (PFD). 1 1 Manual Bang-Bang Phase Detector. When left open, the inputs are pulled to VDD.
SEL3	1	ECL In	SEL3 0 155 MHz Reference Clock. 1 622 MHz Reference Clock. When left open, the input is pulled to VDD.
DI, DIN	42, 44	CML In	Data input, differential 10 Gbit/s. **No ESD input protection.**
CKOUT, CKOUTN	15, 16	Open Collector	Clock output, differential 622 MHz, should always be terminated with a resistor.
LOCK	59	Open Collector	Lock detect output. When low, the divided VCO frequency deviates more than 500/2000 ppm from REFCK/REFCKN, should always be terminated with a resistor to VDD.
PCTL, POUT	49, 47	Analogue Out/In	Phase and Frequency Detector output, should always be terminated with a resistor to VDD.
PHIGH, PLOW	50, 53	Open Collector	Phase and Frequency Detector output, should always be terminated with a resistor to VDD.
VCTL	46	Analogue In	VCO voltage control input.
DTC, DTCN	17, 18	Analogue In	Decision threshold control.
RESET	41	ECL IN	Connect to VEE. Not needed on power up, used for test purpose.
TCK	45	ECL IN	Connect to VDD. Used for test purpose. When left open, the input is pulled to VDD.
VDD	4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65	PWR	Digital Ground 0 V.
VDDA	35	PWR	PLL Ground 0 V.
VDDO	51	PWR	VCO Ground 0 V. For test purpose, connect to VEE.
VEE	34, 68	PWR	-5.2 V Digital supply voltage.
VEEA	52	PWR	-5.2 V PLL supply voltage.

Package Pinout

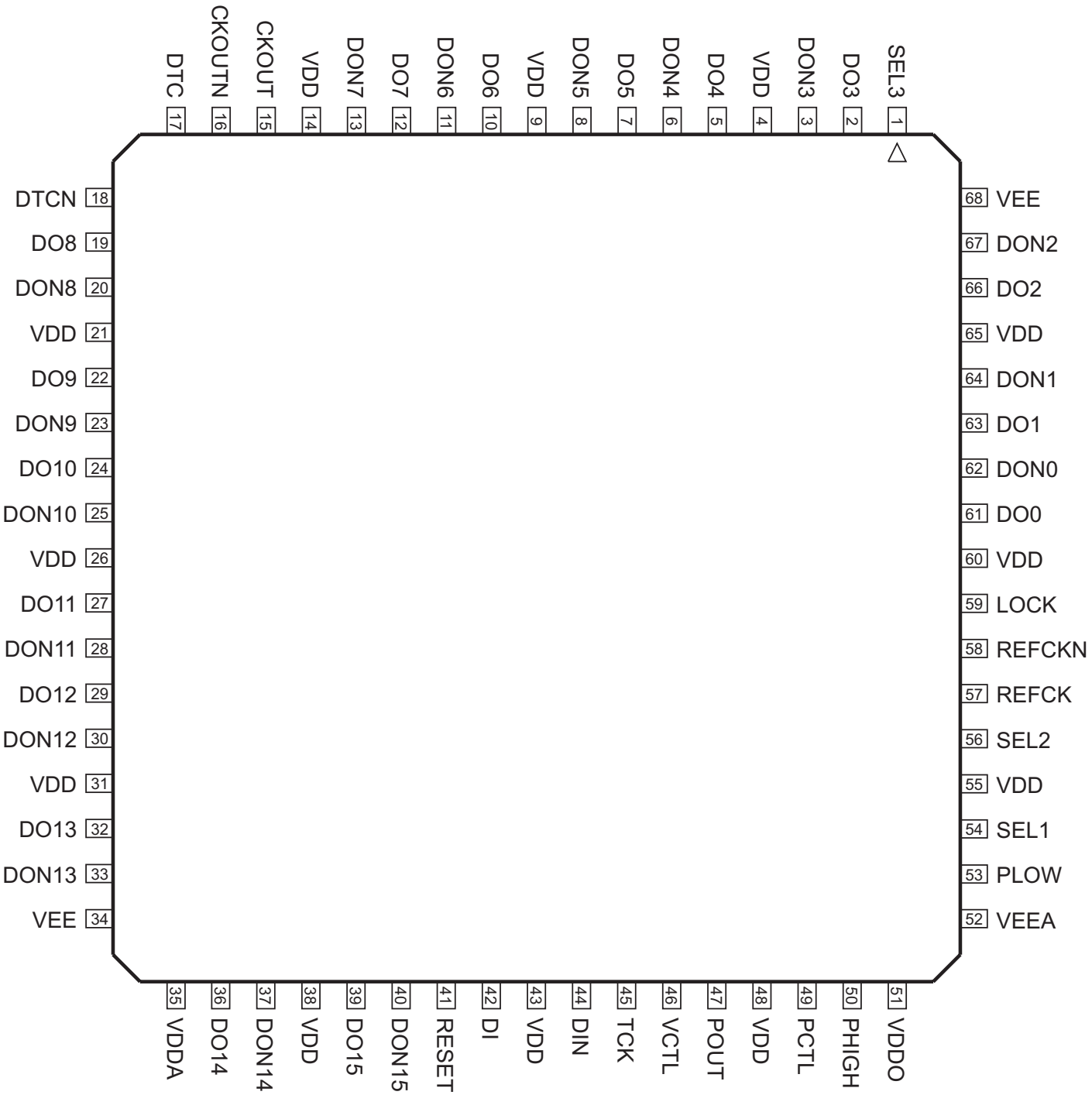


Figure 11. *Package Pinout, Top View*

Note: VDD = Cavity

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VDD.
All currents are defined positive out of the pin.
VDD is 0 V or GND.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Negative Supply		0		-6	V
$V_{O\ CML}$	CML Output Voltage		0		V_{EE}	V
$I_{O\ CML}$	CML Output Current	Note 1	0		-12	mA
$V_{I\ CML}$	CML Input Voltage		V_{CMLT} -1.5		0.5	V
$I_{I\ CML}$	CML Input Current	Note 1	-25		25	mA
P_{OUT}	POUT Voltage	DC	V_{EE}		-3.6	V
V_{ESD}	Static Discharge Voltage	HBM, Note 2			500	V
		CDM, Note 3			50	V
T_J	Junction Temperature		-55		+125	°C
T_S	Storage Temperature		-65		+125	°C

Note 1: Nominal supply voltages.
Note 2: Human Body Model: MIL 883D 3015.7 standard.
Note 3: Charge Device Model.: JESD2-C101 standard.

DC Characteristics

T_{CASE} = 0 °C to 70 °C. VEE = -5.2 V
All voltages in table are referred to VDD.
All currents are defined positive out of pin.
VDD is 0 V or GND.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Negative Supply Voltage		-5.0	-5.2	-5.4	V
I_{EE}	Supply Current		455	550	660	mA
$V_{IH\ CML}$	CML Input Voltage High		-0.1	0	+0.1	V
$V_{IL\ CML}$	CML Input Voltage Low		-0.25	-0.4	-1	V
$V_{OH\ OC}$	Open Collector Output Voltage High	Note 1, 3	-0.05	0	+0.05	V
$V_{OL\ OC}$	Open Collector Output Voltage Low	Note 1, 3	-0.3	-0.4	-0.5	V
$I_{IH\ CML}$	CML Input Current High	V_{IH} *CML*, 50 Ω input		0		mA
$I_{IL\ CML}$	CML Input Current Low	V_{IL} *CML*, 50 Ω input		8		mA
$I_{OH\ OC}$	Open Collector Output Current High	Note 1, 3	-0.1	0	+0.1	mA
$I_{OL\ OC}$	Open Collector Output Current Low	Note 1, 3	-7	-8	-10	mA
$V_{IH\ ECL}$	ECL Input Voltage High	Note 2, 5	0		-1.1	V
$V_{IL\ ECL}$	ECL Input Voltage Low	Note 2, 5	-1.5		V_{EE}	V
$I_{IH\ ECL}$	ECL Input Current High	V = -1.1 V			30	µA
$I_{IL\ ECL}$	ECL Input Current Low	V = -1.5 V			30	µA
VADS	Offset Adjustment by DTC/DTCN, Differential	Note 4, 6		±90		mV
$R_{IN\ CML}$	CML Input Resistor Termination	DC	45	50	55	Ω

Note 1: Output externally terminated by 50 Ω to 0 V.
Note 2: All ECL inputs can be connected directly to VDD/VEE.
Note 3: All open collector outputs should always be terminated with a resistor.
Note 4: With DTC and DTCN connected to a 10k potentiometer with the mid pin grounded (0 V).
Note 5: -5.0 V.
Note 6: With open data inputs.

AC Characteristics

T_{CASE} = 0 °C to 70 °C. VEE = -5.2 V

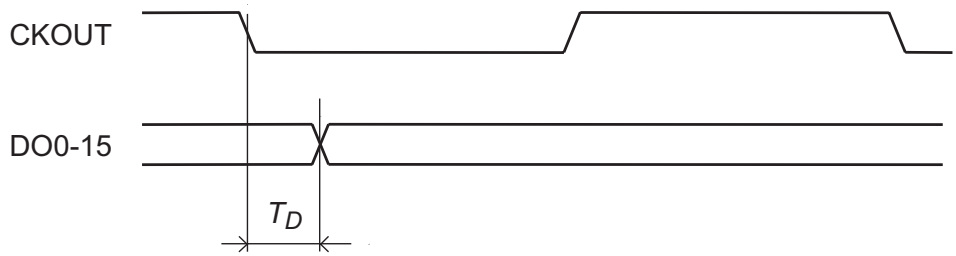


Figure 12. *Timing relation between output clock (CKOUT) and output data (DO0-15)*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{Tol}	Jitter tolerance	2 Hz < F < 400 kHz 4 MHz < F < 80 MHz Note 4	1.5 0.15			UI
T_D	Delay between DO0-15 and CKOUT/CKOUTN		40	160	260	ps
$V_{DI/DIN}$	Data input sensitivity, differential	Note 2			100	mV_{PP}
$\Gamma_{DI/DIN}$	DI/DIN input reflection coefficient	Note 3		-10		dB
$D_{CYCLE\ CKOUT/N}$	CKOUT/CKOUTN frequency		45		55	%
$F_{REFCK/N}$	REFCK/REFCKN frequency	Note 1		155/622		MHz
D_C	REFCK frequency deviation from nominal line frequency		-100		100	ppm
$D_{CYCLE\ REFCK/N}$	REFCK duty cycle		40		60	%

Note 1: Selectable by SEL3.
Note 2: BER = 10^{-9}
Note 3: From DC to 6 GHz. Measured on the GD90244/255 evaluation board.
Depends on lead length, board, soldering etc. of the component.
Note 4: Measured with recommended loop filter (see Figure 1) in the GD90244/255 evaluation board, (1 UI = 100 ps).

Jitter Tolerance Measurements

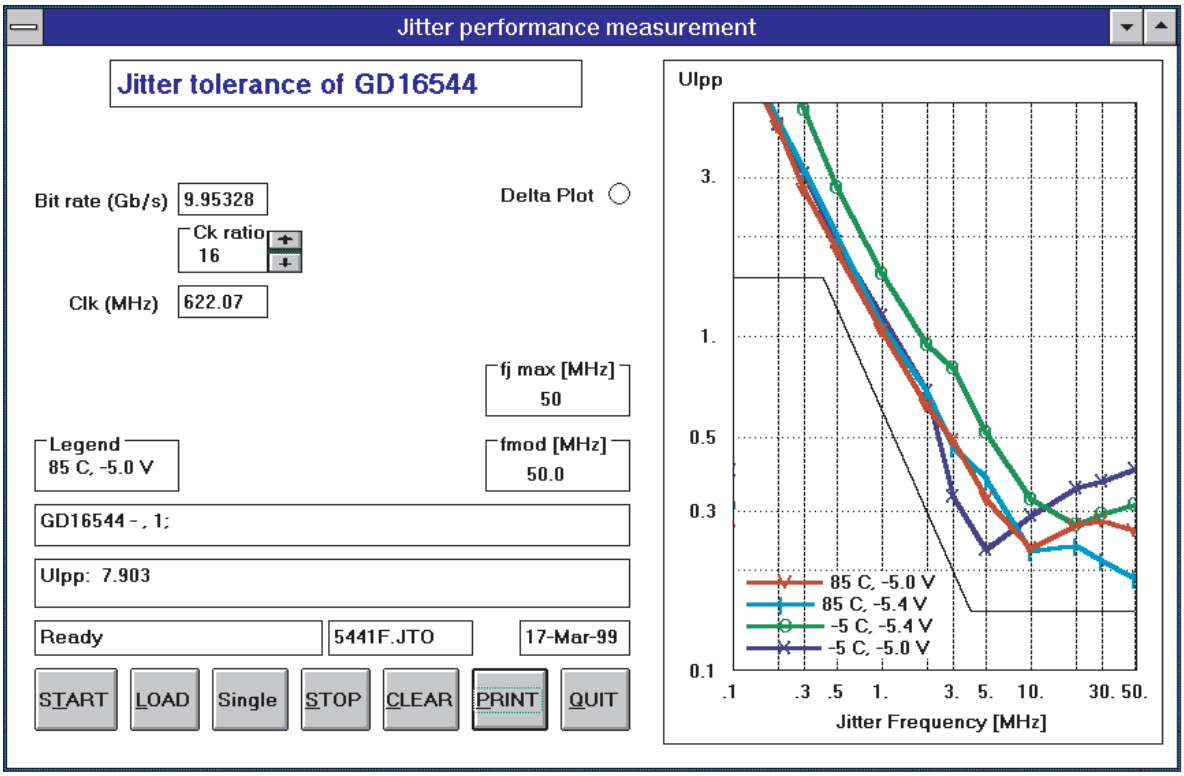


Figure 13. *Jitter tolerance measured with the recommended loop filter (see Figure 1 on page 4) on the 90244/255 evaluation board. The case temperature is 85 °C and -5 ° and the supply voltage is -5 and -5.4 V.*

VCO Measurement

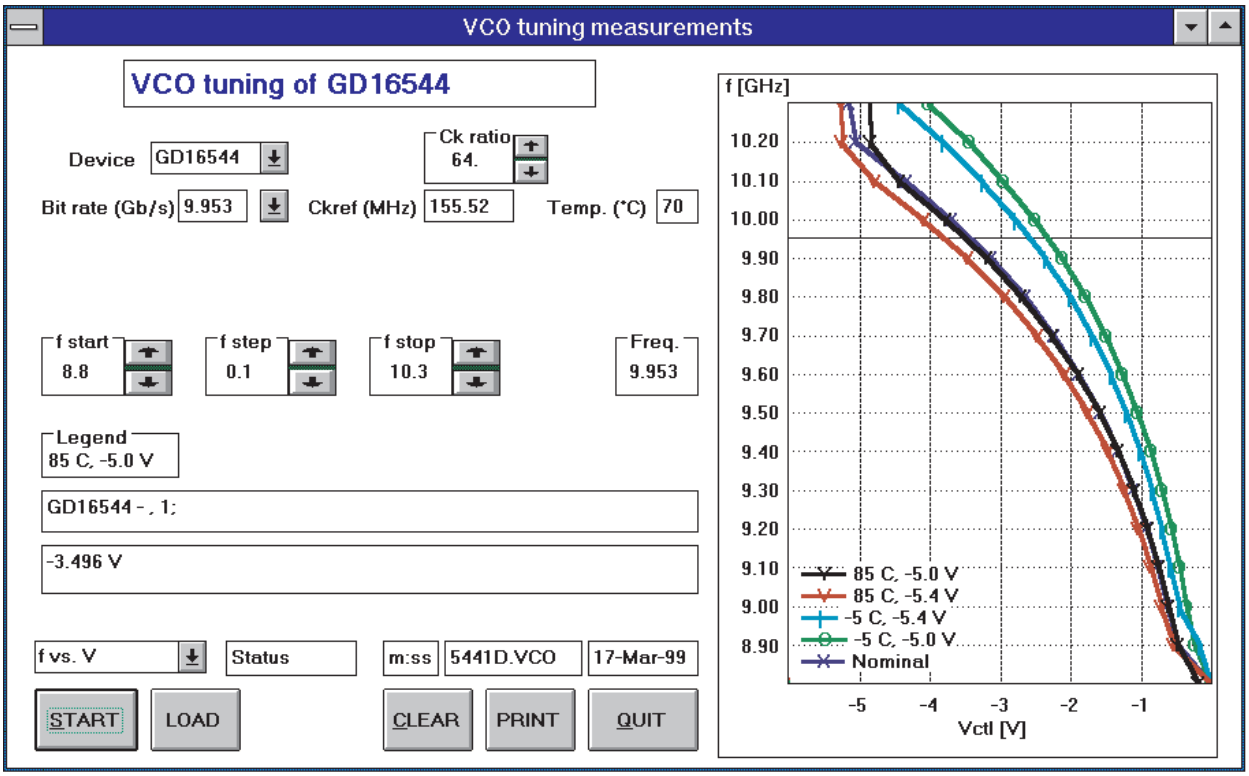


Figure 14. *VCO Tuning Curve*

Mounting of Component on PCB

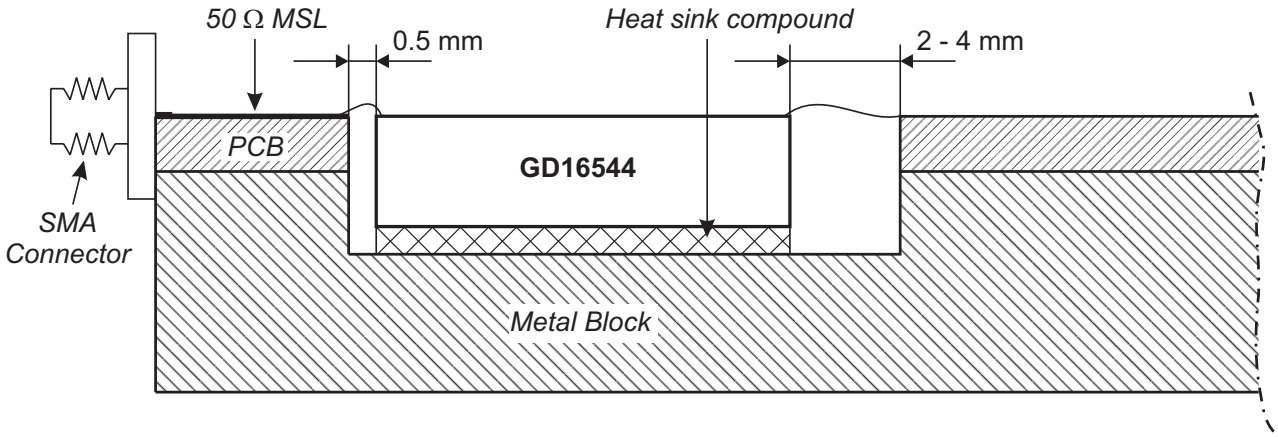


Figure 15. *Example 1.*

Mounting of the component inside a hole in the PCB with short leads for the 10 Gbit/s inputs. The headspreader is down side towards the metal side for best cooling of the component.

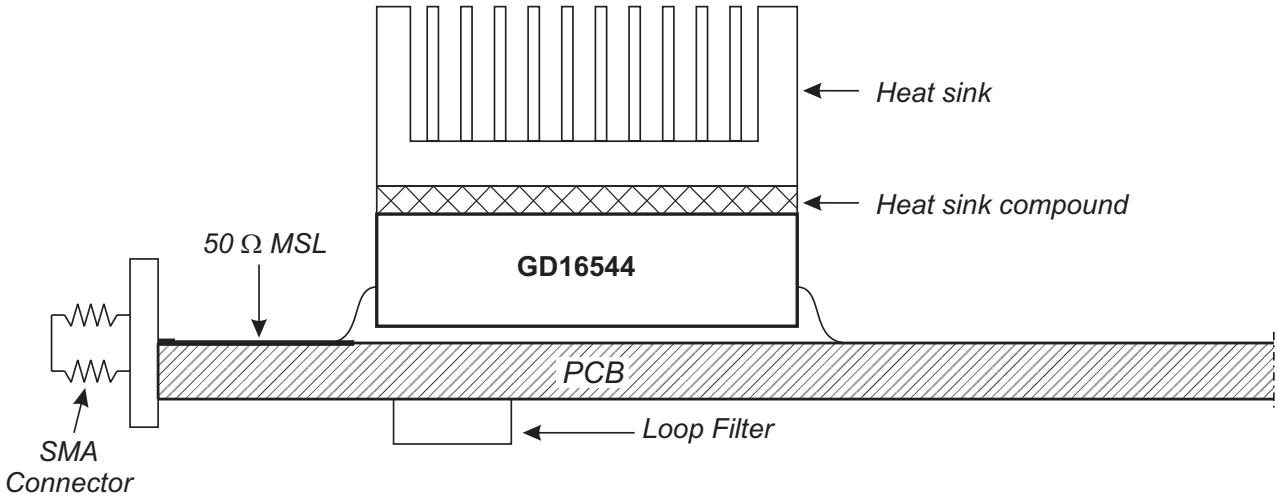


Figure 16. *Example 2.*

Mounting of the component on the PCB with bend leads (gullwings) The headspreader is thermal mounted to a heat sink.

Package Outline

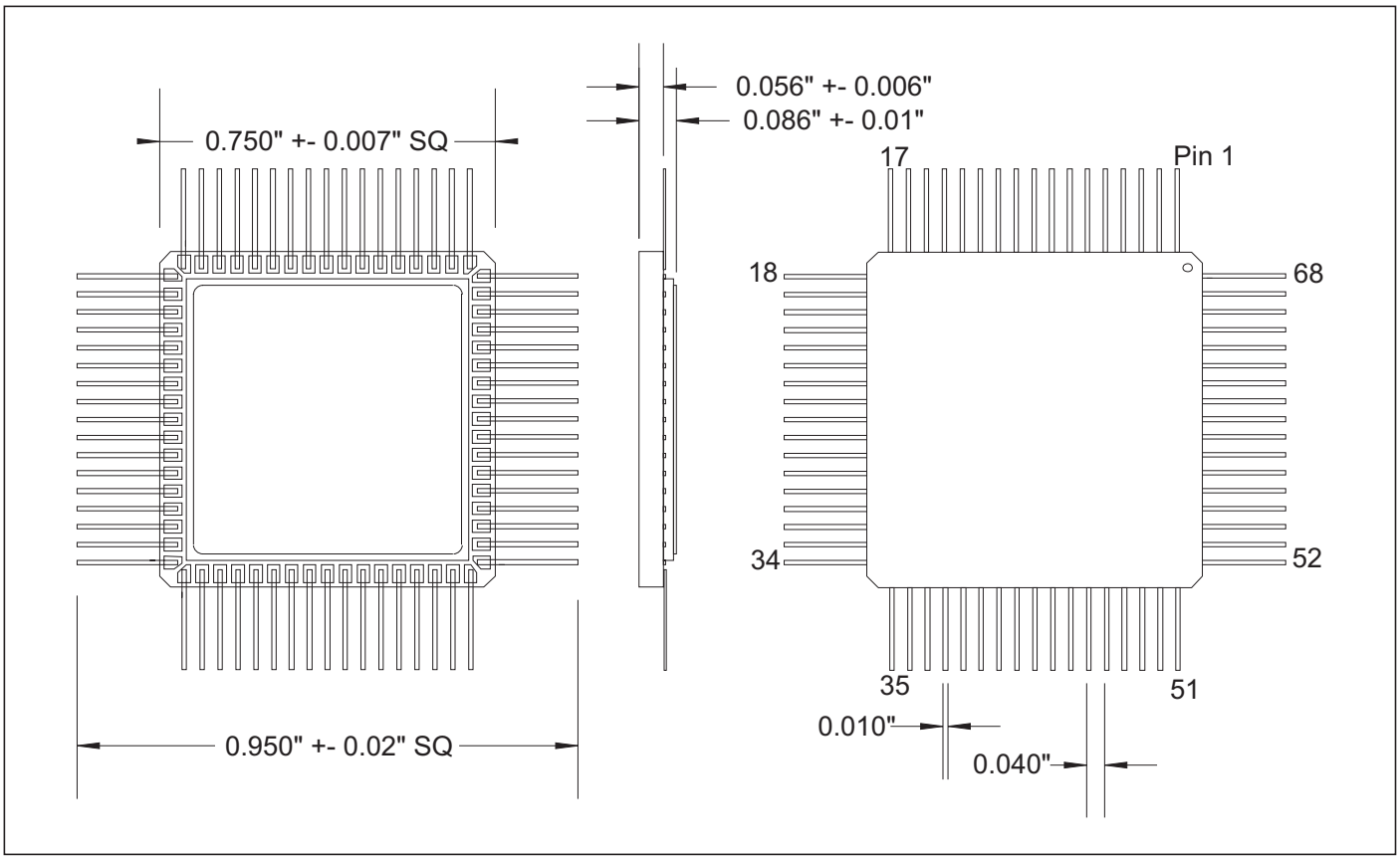


Figure 17. *Package with Straight Leads . All Dimensions are in inch.*

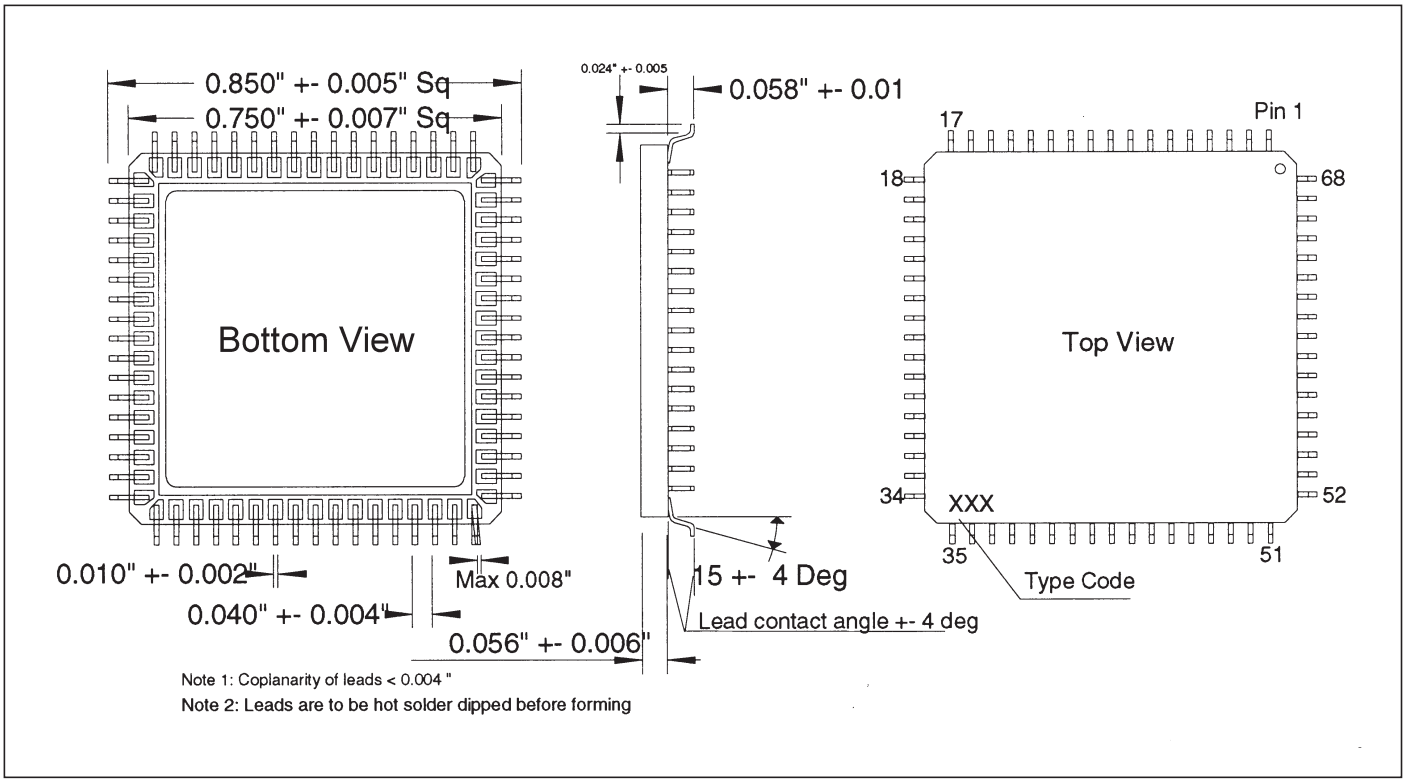


Figure 18. *Package with Gullwings Leads. All Dimensions are in inch.*

Device Marking

Figure 19. *Device Marking, Bottom and Top View*

Ordering Information

To order, please specify as shown below:

Product Name:	Package Type:	Options:	Case Temperature Range:
GD16544-IS	**68 pin Straight Leads,** Multi Layer Ceramic		0..70 °C
GD16544-IG	**68 pin Gullwings Leads,** Multi Layer Ceramic		0..70 °C
GD16544/HV-IS	**68 pin Straight Leads,** Multi Layer Ceramic	Data Outputs DC-tested for 8 V breakdown	0..70 °C
GD16544/HV-IG	**68 pin Gullwings Leads,** Multi Layer Ceramic	Data Outputs DC-tested for 8 V breakdown	0..70 °C

GD16544, Data Sheet Rev.: 06 - Date: 2 November 2001

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