G-LINK Technology

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GLT710008

CMOS SRAM 1M-bit (128K x 8)

Features

- CMOS SRAM organized as 131,072 x 8bits
- Single +5.0V(±10%) Power Supply
- High Speed Access time: 12 and 15 ns
- Low power operation
  - Active: 185 mA (max.)
  - Standby: 55 mA (max.)
- Package Options
  - 32-Pin Plastic SOJ (300 mil)
  - 32-Pin Plastic SOJ (400 mil)
  - 32-Pin Plastic TSOP (Type I)
- Corner Power and Ground

General Description

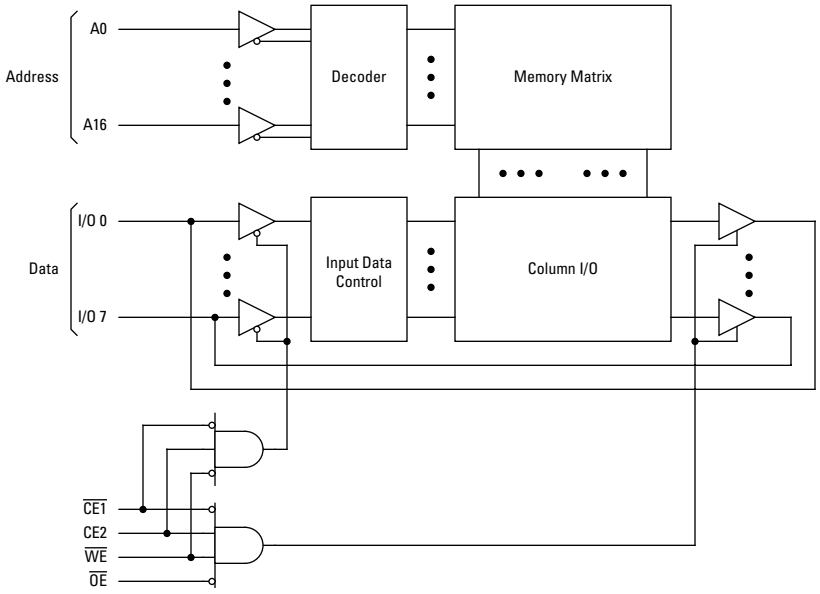
The GLT710008 is a high performance CMOS static RAM organized as 131,072 x 8bits.

Writing to this device is accomplished when the write enable ($\overline{WE}$) and the chip select ($\overline{CE1}$) inputs are both Low and CE2 is high.

Reading is accomplished when $\overline{WE}$ and CE2 is High and $\overline{CE1}$ and the output enable ($\overline{OE}$) are both Low.

The GLT710008 operates from a single +5.0V power supply and all inputs and outputs are fully TTL compatible.

Functional Block Diagram



Pin Description

Symbol	Pin Name
A[16:0]	Address input
I/O[7:0]	Data input/output
$\overline{CE1}$	Chip Enable input
CE2	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input
V_{CC}	Power Supply Pin (+5V)
GND	Ground Pin

Mode Selection Table [1]

$\overline{OE}$	$\overline{WE}$	$\overline{CE1}$	CE2	I/O	MODE
X	X	High	X	High Impedance	Standby
X	X	X	Low	High Impedance	Standby
Low	High	Low	High	Data out	Read
X	Low	Low	High	Data in	Write
High	High	Low	High	High Impedance	Output disable

1. X = don't care.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings [1]

Symbol	Parameter	Rating
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to 7.0 V
T_A	Operating Temperature	0 to 70 °C
T_{STG}	Storage Temperature	-55 to 125 °C
P_T	Power Dissipation	1.0 W
I_{OUT}	DC Output Current	50 mA

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions [1] (0°C to 70°C, GND = 0V, V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	-0.5	-	0.8	V

1. V_{IL}(min) = -3.0V for pulse width less than 20ns.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

I_{DD} Operating Conditions and Maximum Limits

Symbol	Parameter	Max		Unit
		-12	-15	
I_{CC}	Dynamic Operating Current $\overline{CE1} \le V_{IL}$ and CE2 ≥ V_{IH}, V_{CC} = max, f = fmax, I_{OUT} = 0mA, $V_{IN} \ge V_{IH}$ or ≤ V_{IL}	160	155	mA
I_{SB}	Standby Power Supply Current (TTL level) CE1 ≥ V_{IH} and/or CE2 ≤ V_{IL}, V_{CC} = max, f = fmax, $V_{IN} \ge V_{IH}$ or ≤ V_{IL}	35	35	mA
I_{SB1}	Full Standby Power Supply Current (CMOS level) $\overline{CE1} \ge V_{HC}$ and/or CE2 ≤ V_{LC}, V_{CC} = max, f = 0, $V_{IN} \ge V_{HC}$ or ≤ V_{LC}	10	10	mA

DC Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = max, V_{IN} = GND to V_{CC}	-5	5	µA
I_{LO}	Output Leakage Current	V_{CC} = max, $\overline{CE1} \ge V_{IH}$ and/or CE2 ≤ V_{IL}, V_{OUT} = GND to V_{CC}	-5	5	µA
V_{OL}	Output low voltage	I_{OL} = 8 mA, V_{CC} = min	-	0.4	V
		I_{OL} = 10 mA, V_{CC} = min	-	0.5	V
V_{OH}	Output high voltage	I_{OH} = -4 mA, V_{CC} = min	2.4	-	V

AC Characteristics (V_{CC} = 5.0V ± 10%, TA = 0 to +70°C)

Parameter	Symbol [1]	Description	-12		-15		Units
			Min	Max	Min	Max	
Read Cycle	t_{RC}	Read Cycle time	12		15		ns
	t_{AA}	Address access time		12		15	ns
	t_{ACE}	Chip enable access time		12		15	ns
	t_{OH}	Output hold from address change	4		4		ns
	t_{LZCE}	Chip enable to output in low-Z	3		3		ns
	t_{HZCE}	Chip disable to output high-Z		6		7	ns
	t_{PU}	Chip enable to power up time	0		0		ns
	t_{PD}	Chip enable to power down time		12		12	ns
	t_{AOE}	Output enable access time		6		6	ns
	t_{LZOE}	Output enable to output in low-Z	0		0		ns
	t_{HZOE}	Output disable to output in high-Z		6		6	ns
Write Cycle	t_{WC}	Write Cycle time	12		15		ns
	t_{CW}	Chip enable to end of write	10		11		ns
	t_{AW}	Address valid to end of write	10		11		ns
	t_{AS}	Address set-up time	0		0		ns
	t_{AH}	Address hold from end of write	0		0		ns
	t_{WP}	Write pulse width ($\overline{OE} \geq V_{IH}$)	9		11		ns
	t_{DS}	Data set-up time	6		7		ns
	t_{DH}	Data hold time	0		0		ns
	t_{LZWE}	Write disable to output in low-Z	0		0		ns
	t_{HZWE}	Write enable to output in high-Z		5		5	ns

1. t_{LZCE}, t_{LZWE}, t_{HZCE}, t_{LZOE}, t_{HZOE}, t_{PU} and t_{PD} are simulated values.

AC Test Conditions

Parameter	Rating
Input pulse levels	GND to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figure 1

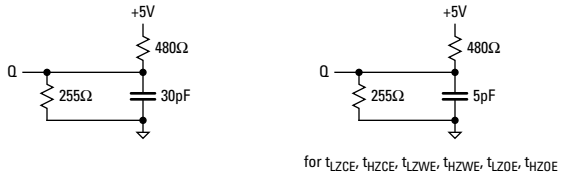


Figure 1. Output Load Equivalent

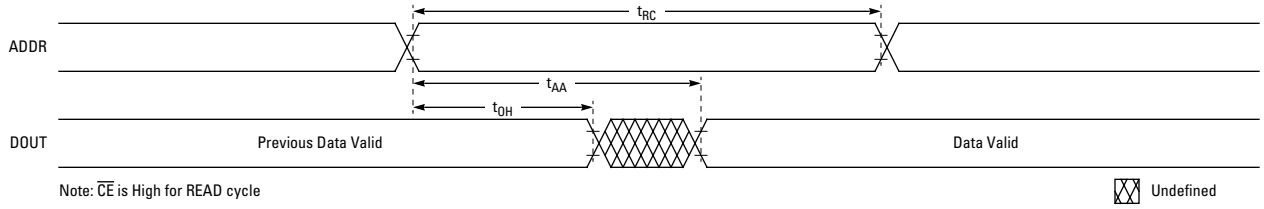


Figure 2. Read Cycle Timing 1

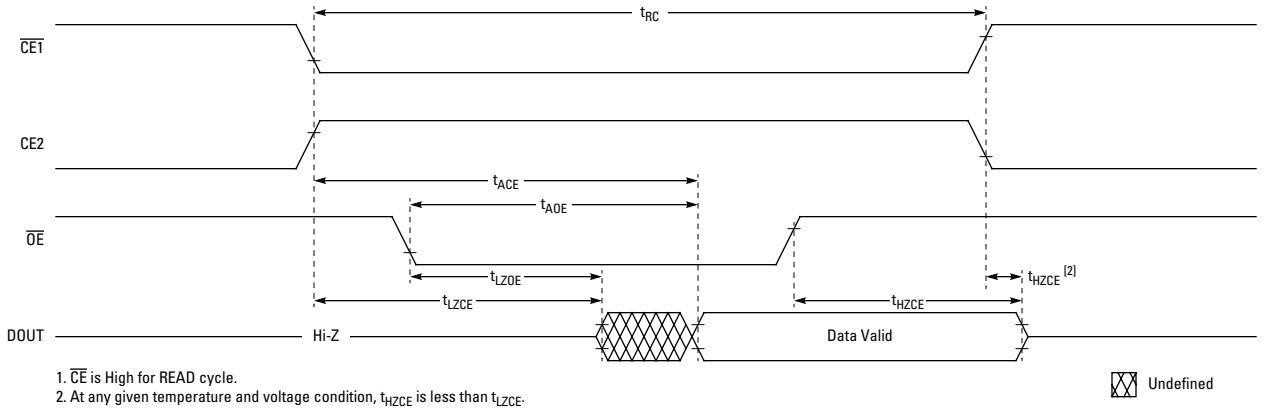


Figure 3. Read Cycle Timing 2

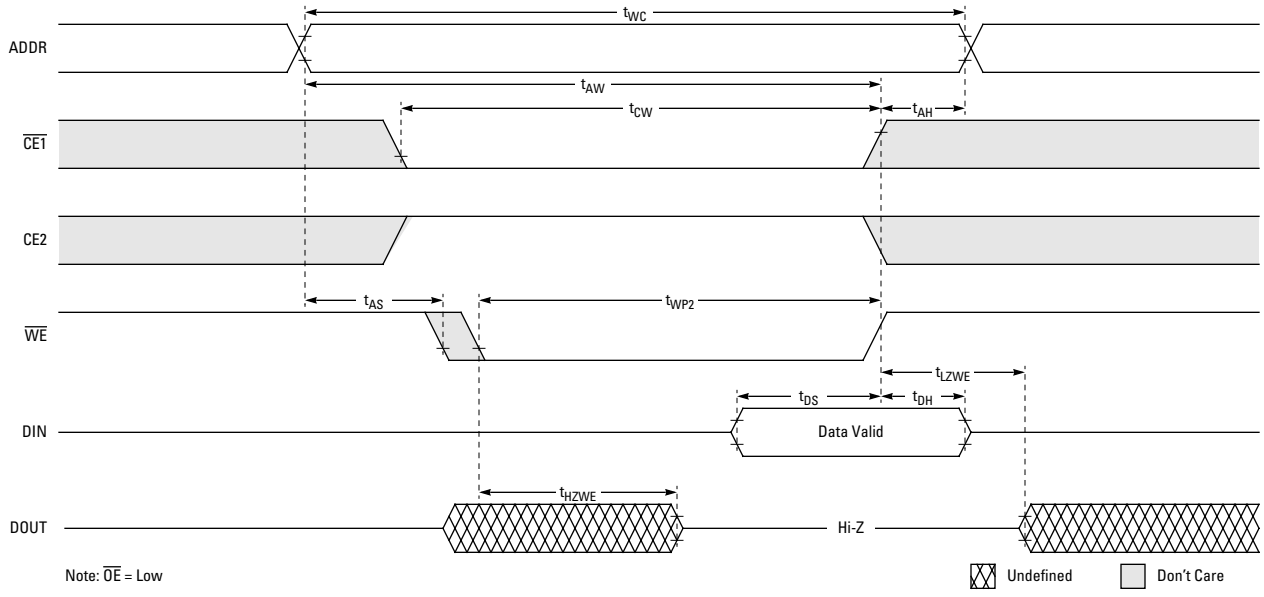


Figure 4. Write Cycle Timing (Write Enabled Controlled, $\overline{OE}$ = Low)

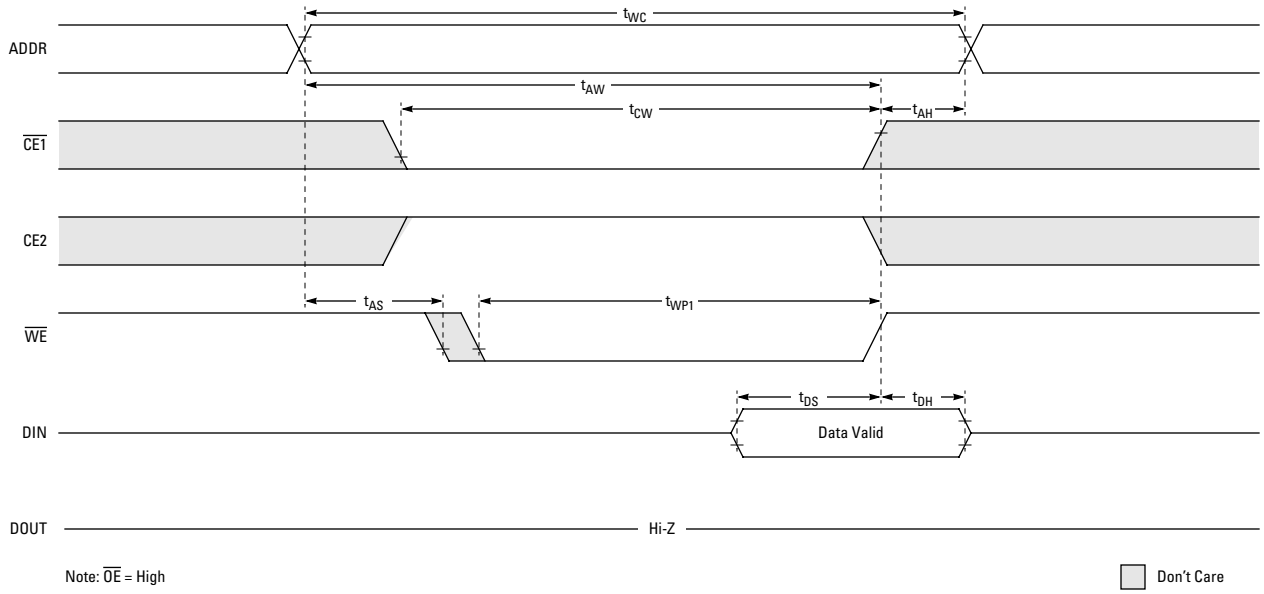


Figure 5. Write Cycle Timing (Chip Enabled Controlled)

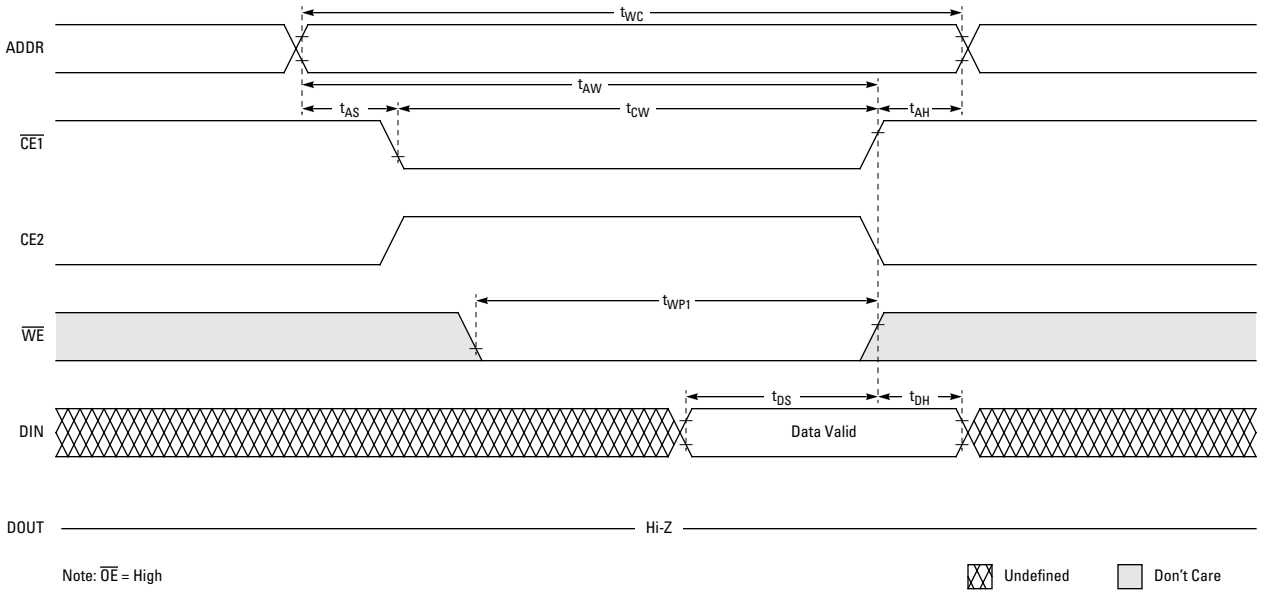


Figure 6. Write Cycle Timing (Chip Enabled Controlled)

Package Information

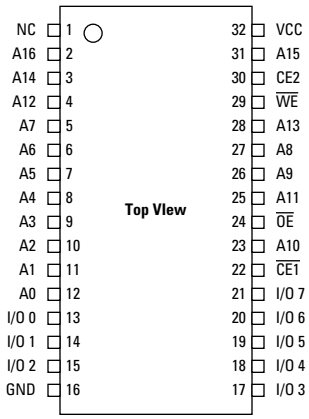
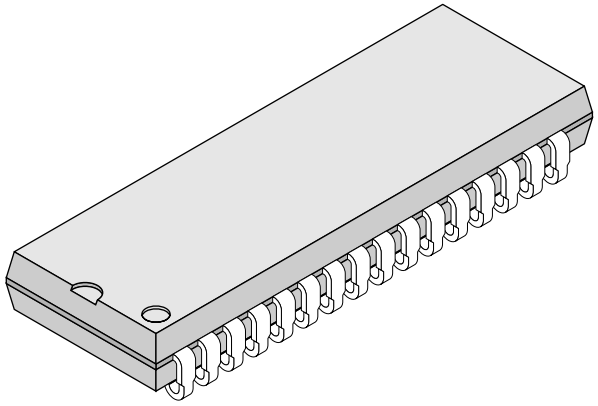


Figure 7. 32-Pin Plastic SOJ/TSOP Logical Pinout



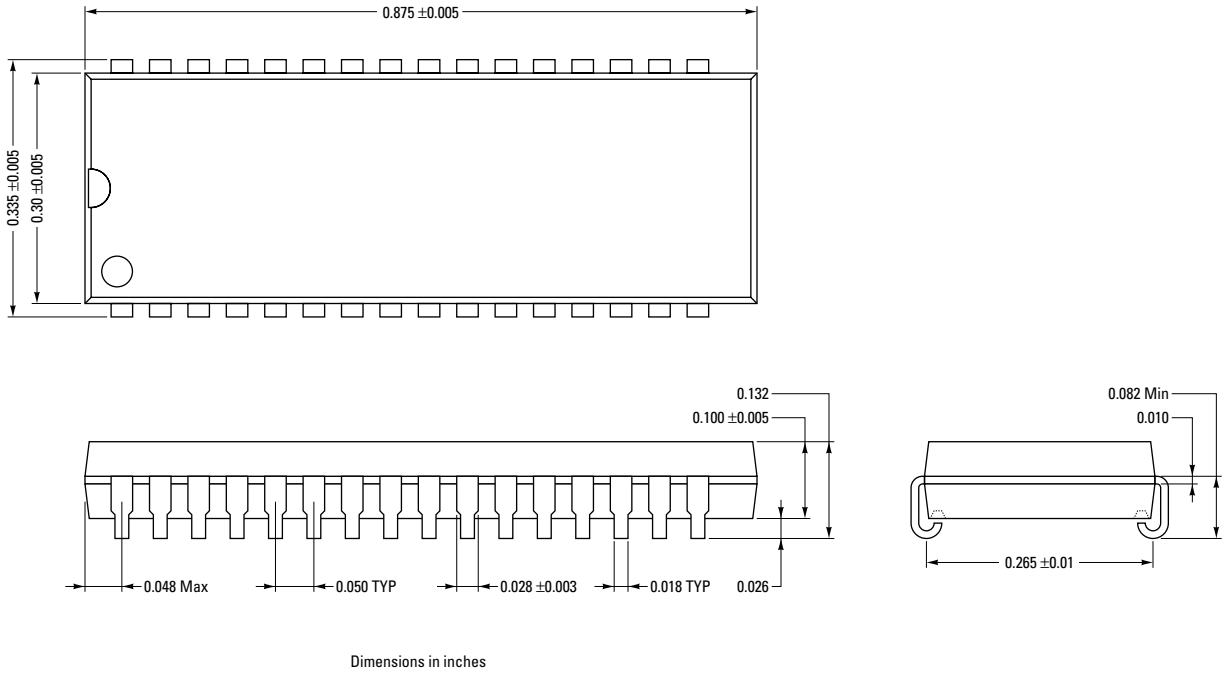
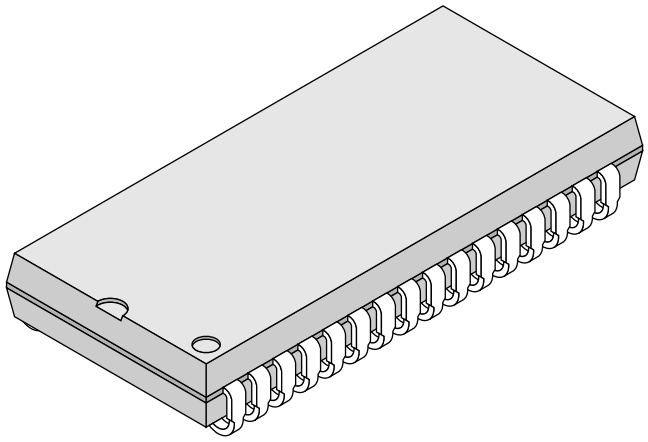


Figure 8. 32-Pin Plastic SOJ (300 mil) Package Dimensions



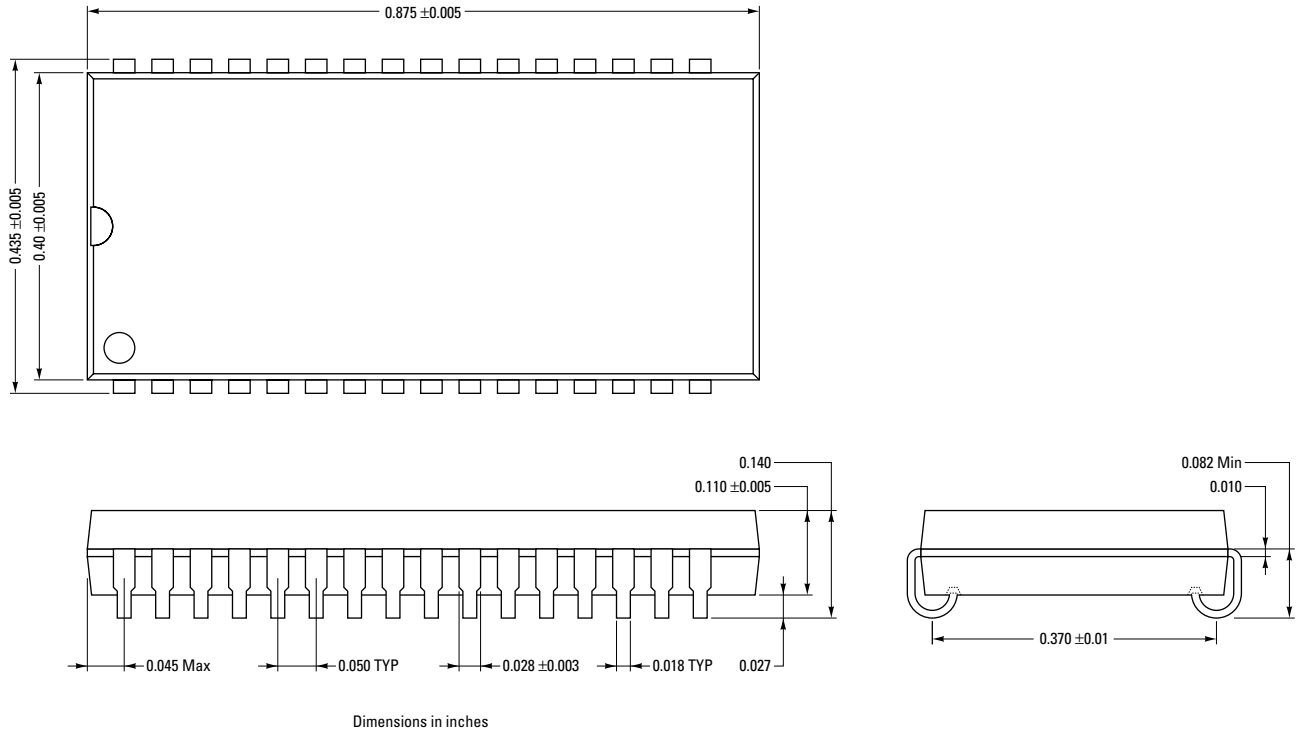
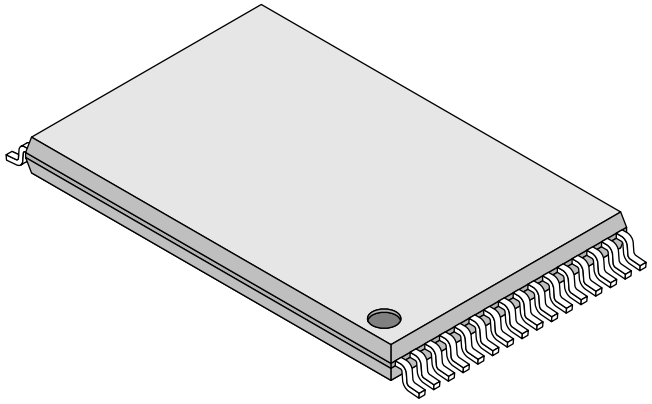


Figure 9. 32-Pin Plastic SOJ (400 mil) Package Dimensions



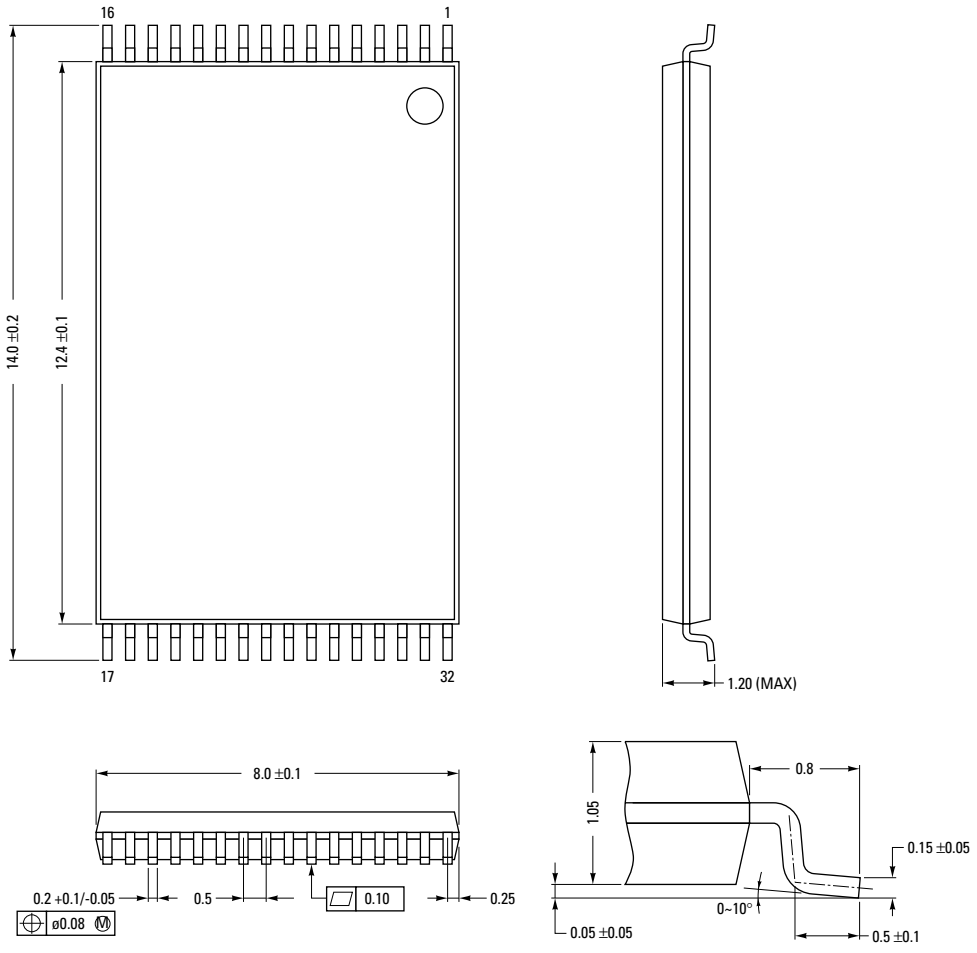


Figure 10. 32-Pin Plastic TSOP (Type I) Package Dimensions

Ordering Info

Part Number	Organization	Power And Ground	Operating Current (mA)	Access Time	Package Type
GLT710008-12J3	128Kx8	Corner	160 mA	12ns	32 pin SOJ (300 mil)
GLT710008-15J3	128Kx8	Corner	155mA	15ns	32 pin SOJ (300 mil)
GLT710008-12J4	128Kx8	Corner	160mA	12ns	32 pin SOJ (400 mil)
GLT710008-15J4	128Kx8	Corner	155mA	15ns	32 pin SOJ (400 mil)
GLT710008-12TS	128Kx8	Corner	160mA	12ns	32 pin TSOP (Type I)
GLT710008-15TS	128Kx8	Corner	155mA	15ns	32 pin TSOP (Type I)

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