

GLT710008

CMOS SRAM 1M-bit (128K x 8)

FEATURES

.....

- ◆ CMOS SRAM organized as 131,072 x 8bits
- ◆ Single +5.0V(±10%) Power Supply
- ◆ High Speed Access time: 12 and 15 ns
- ◆ Low power operation
 - Active: 185 mA (max.)
 - Standby: 55 mA (max.)

- ◆ Package Options
 - 32-Pin Plastic SOJ (300 mil)
 - 32-Pin Plastic SOJ (400 mil)
 - 32-Pin Plastic TSOP (Type I)
- ◆ Corner Power and Ground

GENERAL DESCRIPTION

.....

The GLT710008 is a high performance CMOS static RAM organized as 131,072 x 8bits.

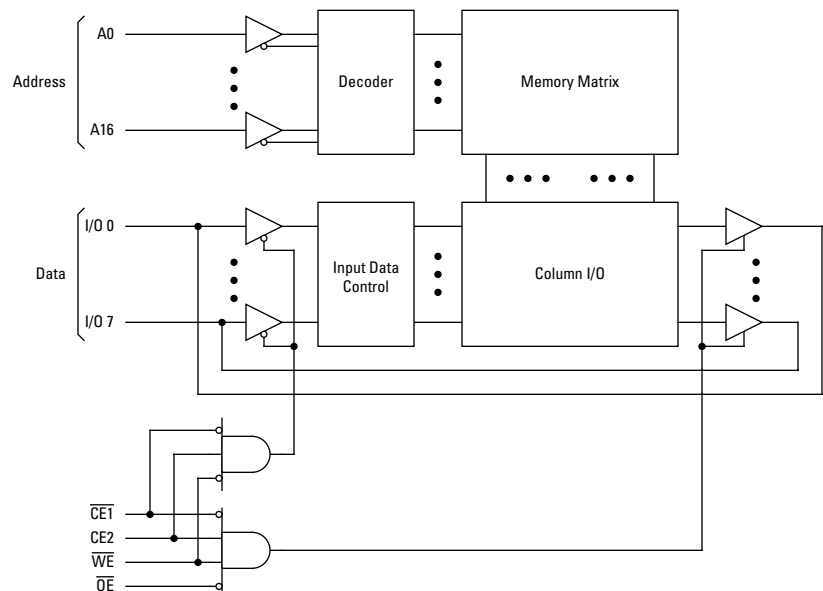
Writing to this device is accomplished when the write enable (\overline{WE}) and the chip select ($\overline{CE1}$) inputs are both Low and CE2 is high.

Reading is accomplished when \overline{WE} and CE2 is High and $\overline{CE1}$ and the output enable (\overline{OE}) are both Low.

The GLT710008 operates from a single +5.0V power supply and all inputs and outputs are fully TTL compatible.

GLT710008

FUNCTIONAL BLOCK DIAGRAM



Pin Description

| Symbol | Pin Name |
|------------------|------------------------|
| A[16:0] | Address input |
| I/O[7:0] | Data input/output |
| $\overline{CE1}$ | Chip Enable input |
| CE2 | Chip Enable input |
| \overline{OE} | Output Enable input |
| \overline{WE} | Write Enable input |
| V _{CC} | Power Supply Pin (+5V) |
| GND | Ground Pin |

Mode Selection Table ^[1]

| \overline{OE} | \overline{WE} | $\overline{CE1}$ | CE2 | I/O | MODE |
|-----------------|-----------------|------------------|------|----------------|----------------|
| X | X | High | X | High Impedance | Standby |
| X | X | X | Low | High Impedance | Standby |
| Low | High | Low | High | Data out | Read |
| X | Low | Low | High | Data in | Write |
| High | High | Low | High | High Impedance | Output disable |

1. X = don't care.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ^[1]

| Symbol | Parameter | Rating |
|------------|--------------------------------------|---------------|
| V_{TERM} | Terminal Voltage with Respect to GND | -0.5 to 7.0 V |
| T_A | Operating Temperature | 0 to 70 °C |
| T_{STG} | Storage Temperature | -55 to 125 °C |
| P_T | Power Dissipation | 1.0 W |
| I_{OUT} | DC Output Current | 50 mA |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions ^[1] (0°C to 70°C, GND = 0V, $V_{CC} = 5.0V \pm 10\%$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------|--------------------|------|-----|----------------|------|
| V_{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| V_{IH} | Input High Voltage | 2.2 | - | $V_{CC} + 0.5$ | V |
| V_{IL} | Input Low Voltage | -0.5 | - | 0.8 | V |

1. $V_{IL}(\min) = -3.0V$ for pulse width less than 20ns.

Capacitance ($T_A = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

| Symbol | Parameter | Condition | Max. | Unit |
|-----------|--------------------|----------------|------|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | 6 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0V$ | 8 | pF |

I_{DD} Operating Conditions and Maximum Limits

| Symbol | Parameter | Max | | Unit |
|-----------|---|-----|-----|------|
| | | -12 | -15 | |
| I_{CC} | Dynamic Operating Current $\overline{CE1} \leq V_{IL}$ and $CE2 \geq V_{IH}$, $V_{CC} = \max$, $f = f_{max}$, $I_{OUT} = 0mA$, $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$ | 160 | 155 | mA |
| I_{SB} | Standby Power Supply Current (TTL level) $CE1 \geq V_{IH}$ and/or $CE2 \leq V_{IL}$, $V_{CC} = \max$, $f = f_{max}$, $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$ | 35 | 35 | mA |
| I_{SB1} | Full Standby Power Supply Current (CMOS level) $\overline{CE1} \geq V_{HC}$ and/or $CE2 \leq V_{LC}$, $V_{CC} = \max$, $f = 0$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ | 10 | 10 | mA |

DC Characteristics ($V_{CC} = 5.0V \pm 10\%$)

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|----------|------------------------|---|------|------|---------|
| I_{LI} | Input Leakage Current | $V_{CC} = \max$, $V_{IN} = \text{GND to } V_{CC}$ | -5 | 5 | μA |
| I_{LO} | Output Leakage Current | $V_{CC} = \max$, $\overline{CE1} \geq V_{IH}$ and/or $CE2 \leq V_{IL}$, $V_{OUT} = \text{GND to } V_{CC}$ | -5 | 5 | μA |
| V_{OL} | Output low voltage | $I_{OL} = 8\text{ mA}$, $V_{CC} = \min$ | - | 0.4 | V |
| | | $I_{OL} = 10\text{ mA}$, $V_{CC} = \min$ | - | 0.5 | V |
| V_{OH} | Output high voltage | $I_{OH} = -4\text{ mA}$, $V_{CC} = \min$ | 2.4 | - | V |

GLT710008

AC Characteristics ($V_{CC} = 5.0V \pm 10\%$, $T_A = 0$ to $+70^\circ C$)

| Parameter | Symbol [1] | Description | -12 | | -15 | | Units |
|-------------|------------|---|-----|-----|-----|-----|-------|
| | | | Min | Max | Min | Max | |
| Read Cycle | t_{RC} | Read Cycle time | 12 | | 15 | | ns |
| | t_{AA} | Address access time | | 12 | | 15 | ns |
| | t_{ACE} | Chip enable access time | | 12 | | 15 | ns |
| | t_{OH} | Output hold from address change | 4 | | 4 | | ns |
| | t_{LZCE} | Chip enable to output in low-Z | 3 | | 3 | | ns |
| | t_{HZCE} | Chip disable to output high-Z | | 6 | | 7 | ns |
| | t_{PU} | Chip enable to power up time | 0 | | 0 | | ns |
| | t_{PD} | Chip enable to power down time | | 12 | | 12 | ns |
| | t_{AOE} | Output enable access time | | 6 | | 6 | ns |
| | t_{LZOE} | Output enable to output in low-Z | 0 | | 0 | | ns |
| | t_{HZOE} | Output disable to output in high-Z | | 6 | | 6 | ns |
| Write Cycle | t_{WC} | Write Cycle time | 12 | | 15 | | ns |
| | t_{CW} | Chip enable to end of write | 10 | | 11 | | ns |
| | t_{AW} | Address valid to end of write | 10 | | 11 | | ns |
| | t_{AS} | Address set-up time | 0 | | 0 | | ns |
| | t_{AH} | Address hold from end of write | 0 | | 0 | | ns |
| | t_{WP} | Write pulse width ($\overline{OE} \geq V_{IH}$) | 9 | | 11 | | ns |
| | t_{DS} | Data set-up time | 6 | | 7 | | ns |
| | t_{DH} | Data hold time | 0 | | 0 | | ns |
| | t_{LZWE} | Write disable to output in low-Z | 0 | | 0 | | ns |
| | t_{HZWE} | Write enable to output in high-Z | | 5 | | 5 | ns |

1. t_{LZCE} , t_{LZWE} , t_{HZCE} , t_{LZOE} , t_{HZOE} , t_{PU} and t_{PD} are simulated values.

AC Test Conditions

| Parameter | Rating |
|-------------------------------|--------------|
| Input pulse levels | GND to 3.0V |
| Input rise and fall times | 3 ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See Figure 1 |

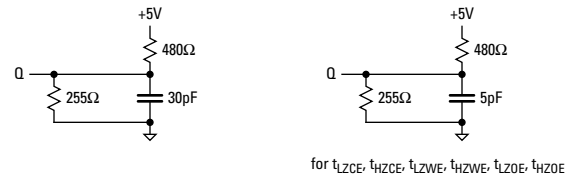


Figure 1. Output Load Equivalent

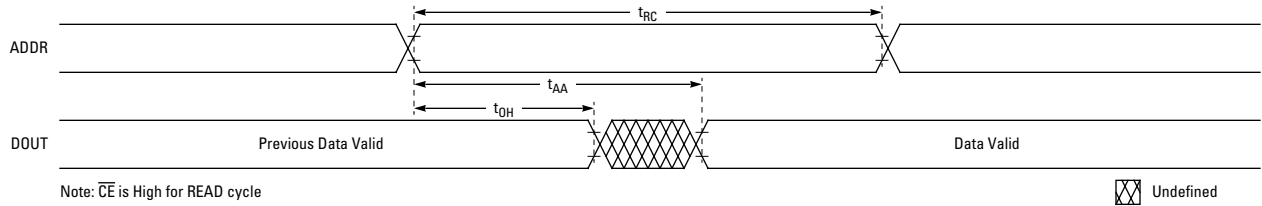


Figure 2. Read Cycle Timing 1

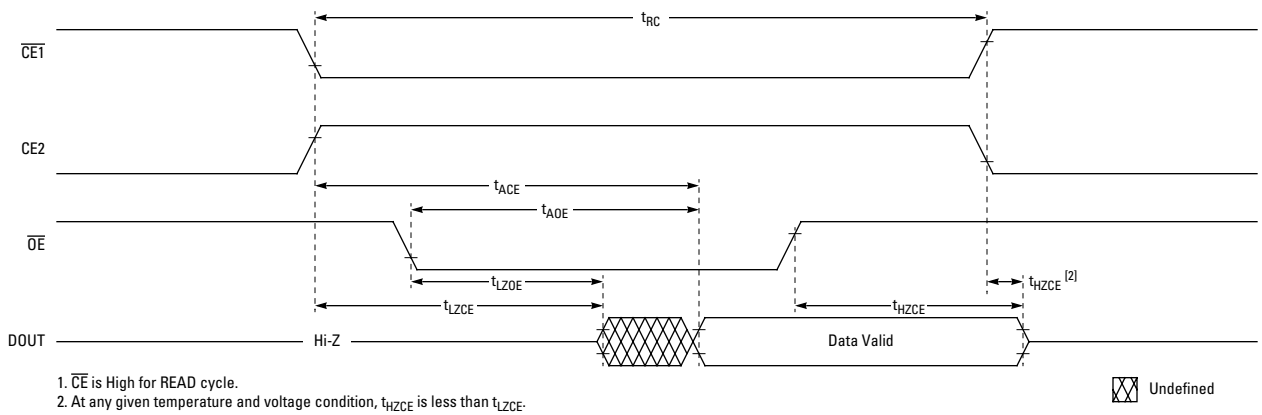


Figure 3. Read Cycle Timing 2

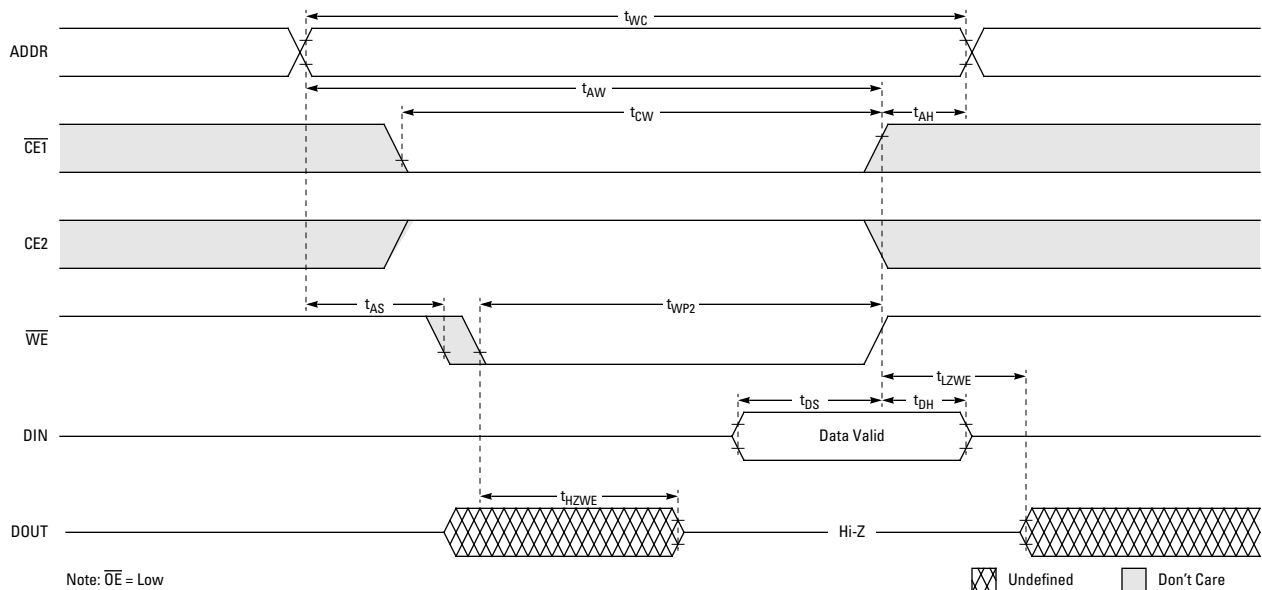


Figure 4. Write Cycle Timing (Write Enabled Controlled, \overline{OE} = Low)

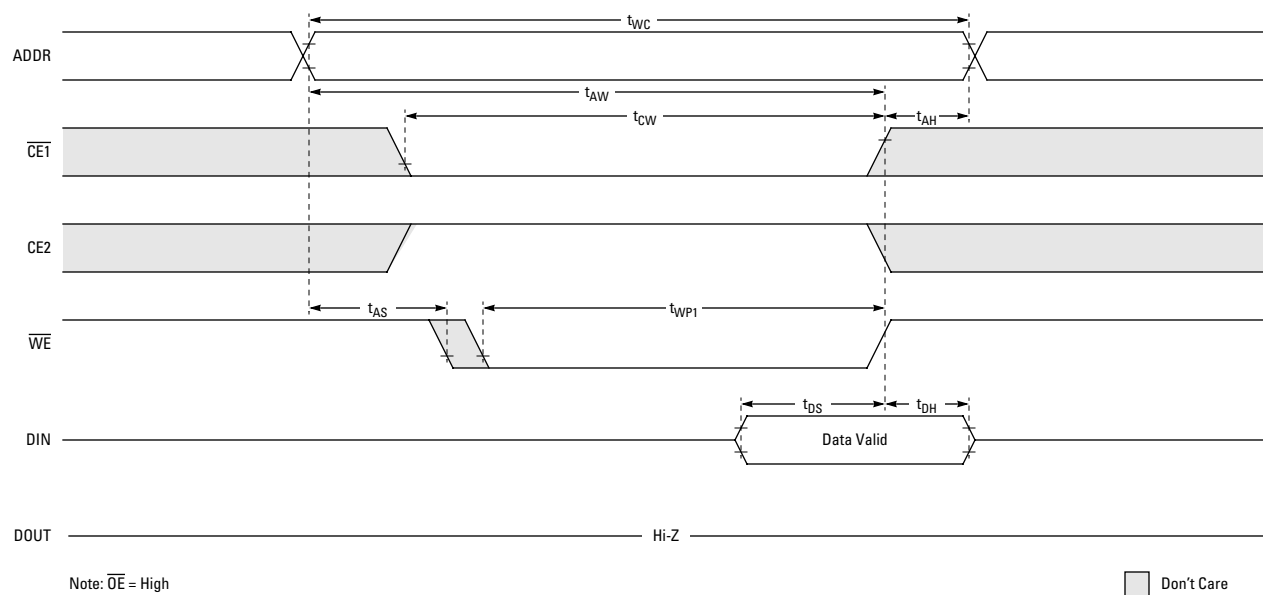


Figure 5. Write Cycle Timing (Chip Enabled Controlled)

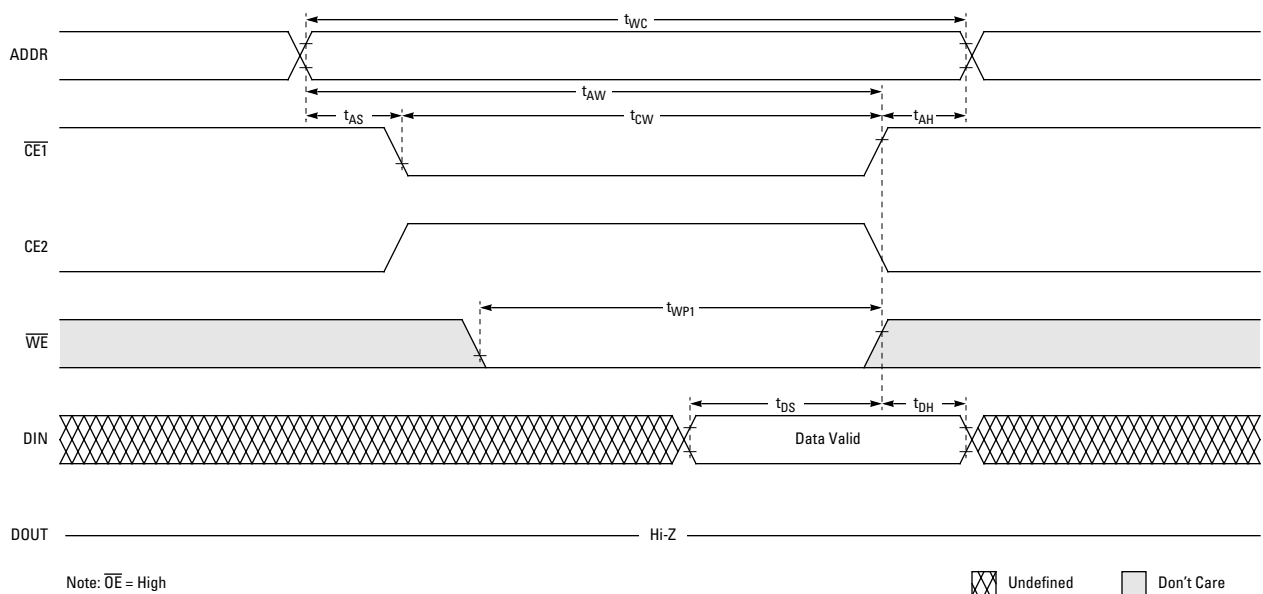


Figure 6. Write Cycle Timing (Chip Enabled Controlled)

PACKAGE INFORMATION

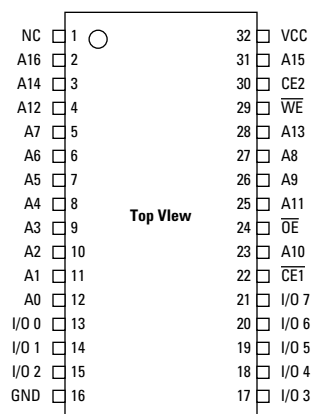


Figure 7. 32-Pin Plastic SOJ/TSOP Logical Pinout

GLT710008

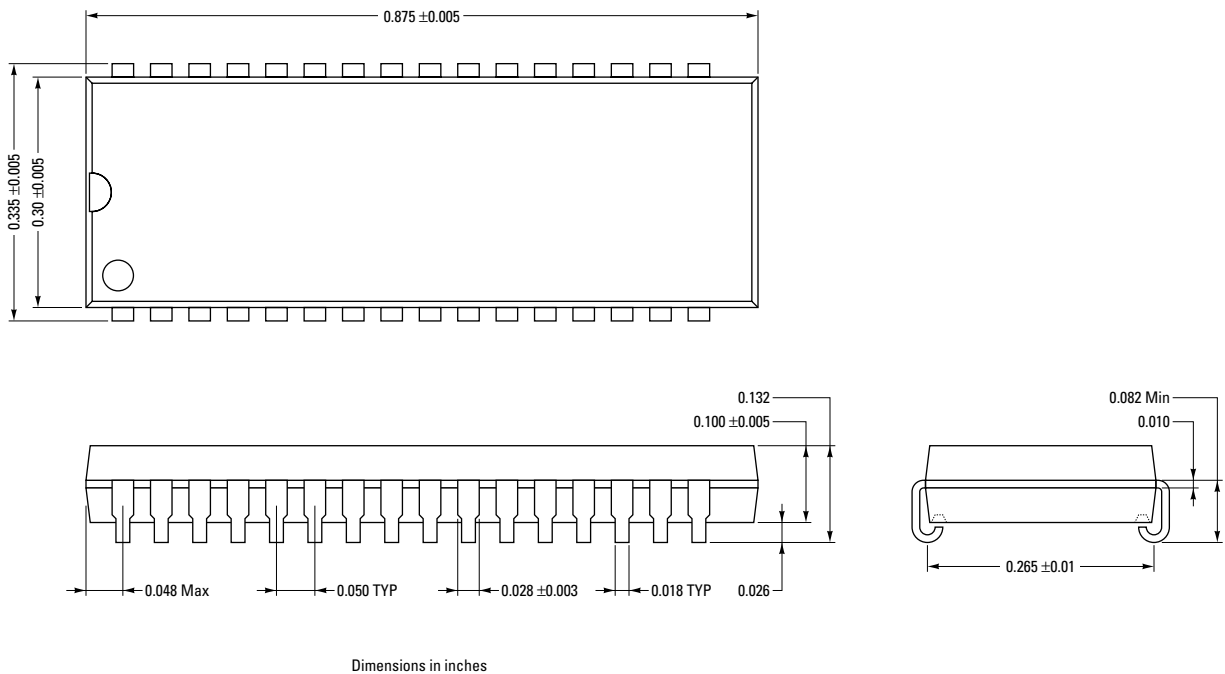
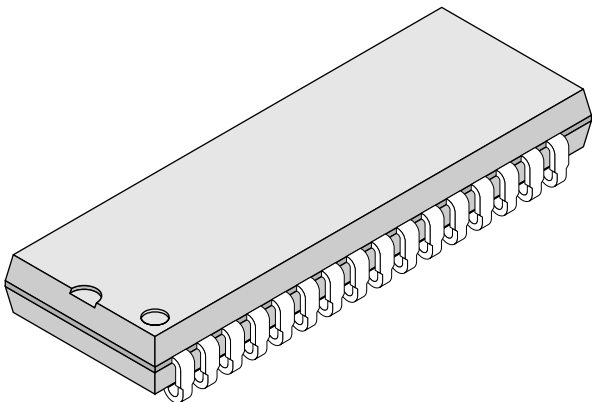


Figure 8. 32-Pin Plastic SOJ (300 mil) Package Dimensions

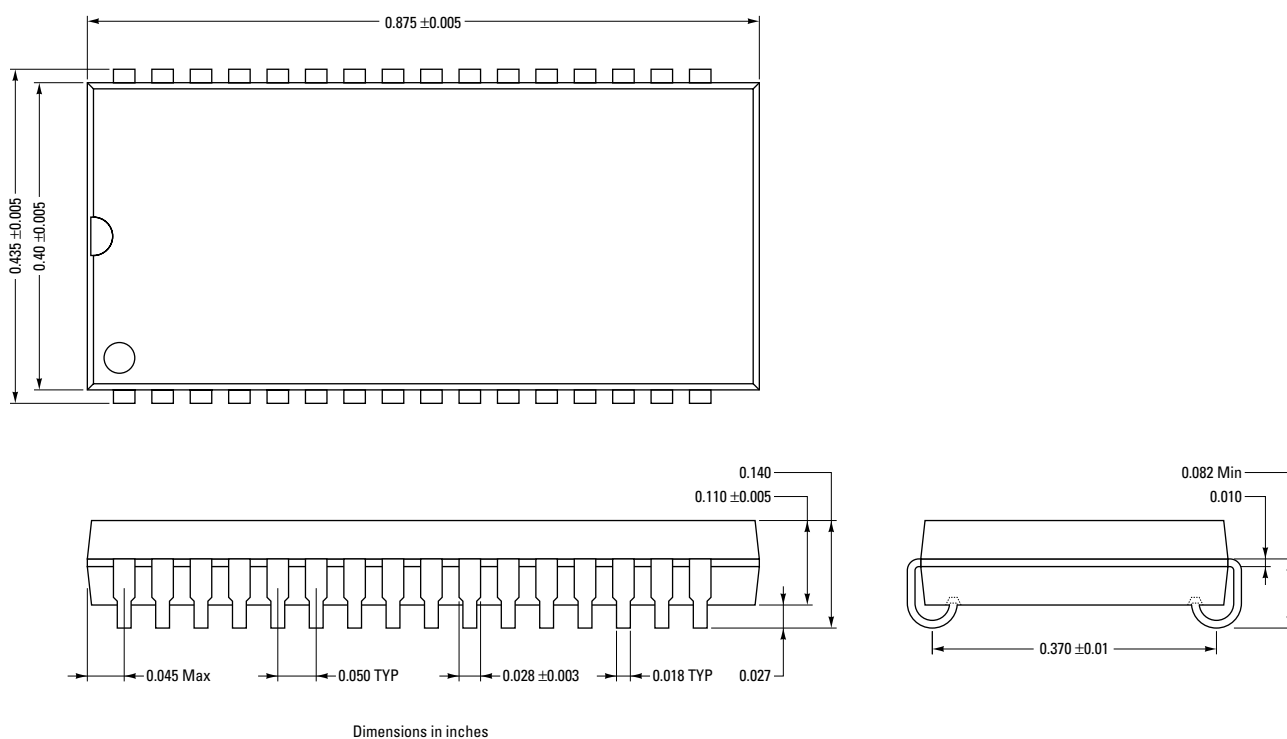
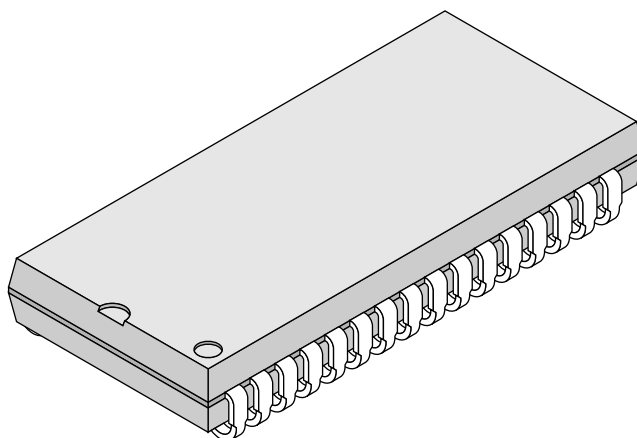


Figure 9. 32-Pin Plastic SOJ (400 mil) Package Dimensions

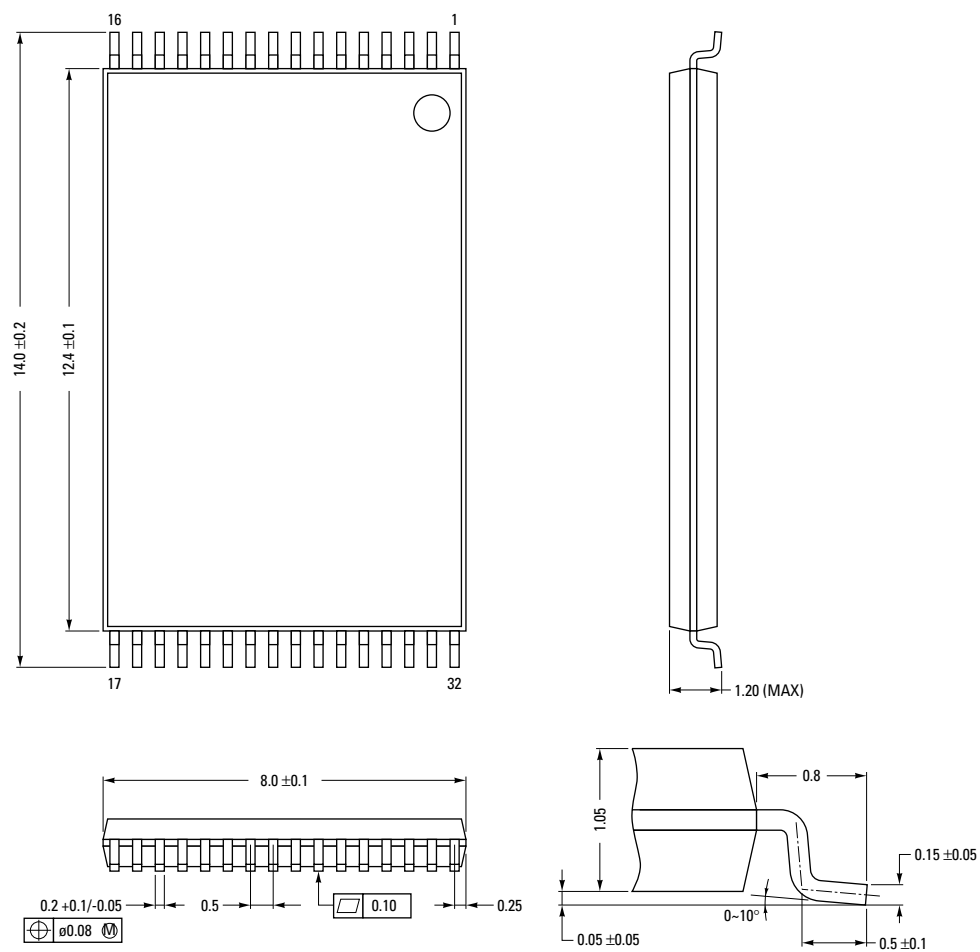
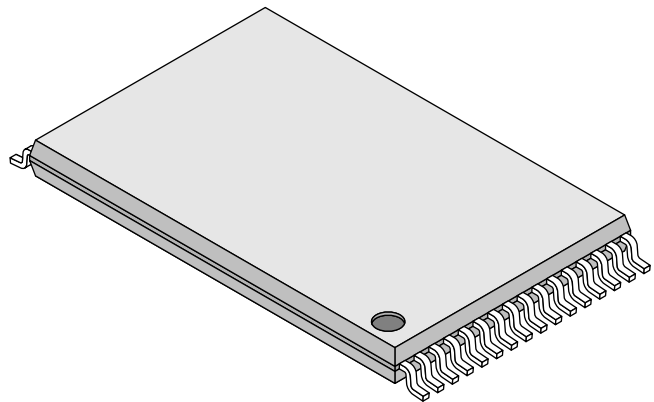


Figure 10. 32-Pin Plastic TSOP (Type I) Package Dimensions

ORDERING INFO

.....

| Part Number | Organization | Power And Ground | Operating Current (mA) | Access Time | Package Type |
|----------------|--------------|------------------|------------------------|-------------|----------------------|
| GLT710008-12J3 | 128Kx8 | Corner | 160 mA | 12ns | 32 pin SOJ (300 mil) |
| GLT710008-15J3 | 128Kx8 | Corner | 155mA | 15ns | 32 pin SOJ (300 mil) |
| GLT710008-12J4 | 128Kx8 | Corner | 160mA | 12ns | 32 pin SOJ (400 mil) |
| GLT710008-15J4 | 128Kx8 | Corner | 155mA | 15ns | 32 pin SOJ (400 mil) |
| GLT710008-12TS | 128Kx8 | Corner | 160mA | 12ns | 32 pin TSOP (Type I) |
| GLT710008-15TS | 128Kx8 | Corner | 155mA | 15ns | 32 pin TSOP (Type I) |



.....
www.glinktech.com

G-LINK Technology

1753 South Main Street
Milpitas, California, 95035, USA
TEL: 408-240-1380 • FAX: 408-240-1385

G-LINK Technology Corporation, Taiwan

6F, No. 24-2, Industry E. Rd. IV
Science-Based Industrial Park
Hsin Chu, Taiwan, R.O.C.
TEL: 03-578-2833 • FAX: 03-578-5820

© 2001 G-LINK Technology

All rights reserved. No part of this document may be copied or reproduced in any form or by any means or transferred to any third party without the prior written consent of G-LINK Technology.

Circuit diagrams utilizing G-LINK products are included as a means of illustrating typical semiconductor applications. Complete information sufficient for design purposes is not necessarily given.

G-LINK Technology reserves the right to change products or specifications without notice.

The information contained in this document does not convey any license under copyrights, patent rights or trademarks claimed and owned by G-LINK or its subsidiaries. G-LINK assumes no liability for G-LINK applications assistance, customer's product design, or infringement of patents arising from use of semiconductor devices in such systems' designs. Nor does G-LINK warrant or represent that any patent right, copyright, or other intellectual property right of G-LINK covering or relating to any combination, machine, or process in which such semiconductor devices might be or are used.

G-LINK Technology's products are not authorized for use in life support devices or systems. Life support devices or systems are device or systems which are: a) intended for surgical implant into the human body and b) designed to support or sustain life; and when properly used according to label instructions, can reasonably be expected to cause significant injury to the user in the event of failure.

The information contained in this document is believed to be entirely accurate. However, G-LINK Technology assumes no responsibility for inaccuracies.