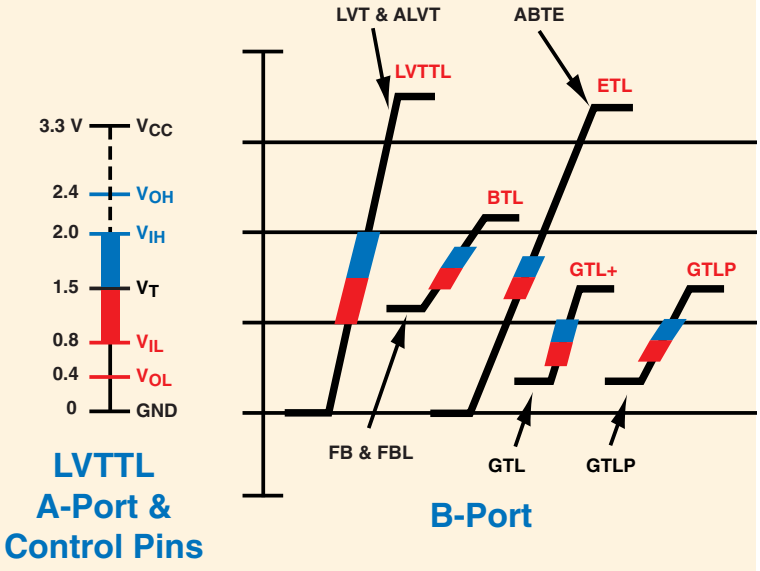
Philips Family of GTLP
Backplane Optimized Translators

GTLPH16612

18-bit GTLP to LVTTL/TTL Bi-Directional Universal Translator

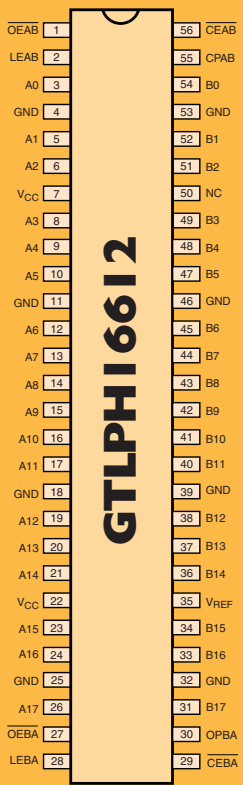
GTL1655

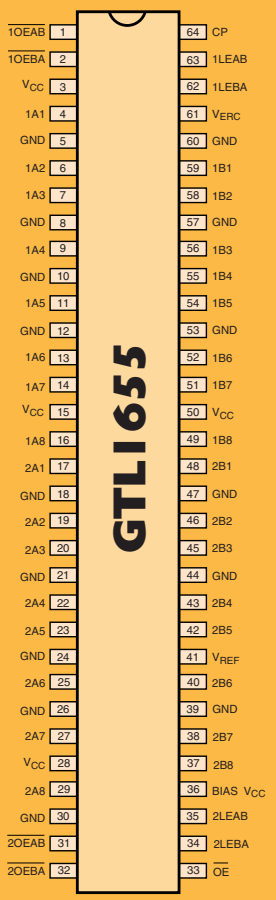
16-bit GTL/GTLP to LVTTL/TTL Bus Transceiver with Live Insertion



GTLP allows higher frequency operation in backplane applications because the controlled edge rates reduce ringing. The ability to match the termination pull-up resistor value with the loaded backplane trace impedance facilitates incident wave switching.

Pin Configurations





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Description

The GTLPH16612 is a medium drive 18-bit GTLP to LVTTL/TTL bi-directional universal translator and the GTL1655 is a high drive 16-bit GTL/GTLP to LVTTL/TTL bi-directional bus translator. The primary application for these devices are the logic signal translation between a LVTTL/TTL processor (like the Motorola Power PC) and a GTLP backplane, such as those used in telecom/networking and other applications that need high-speed transmission of large amounts of information in a multi-point environment. The GTLP family is an improvement over existing LVTTL, BTL or ETL logic for higher frequency operation in multi-point applications and a lower cost parallel alternative to high speed serial solutions in high data rate transfer applications.

GTLPH16612 Features

The GTLPH16612 is a high-performance BiCMOS 18-bit bi-directional universal translator between GTLP signal levels (B port) and LVTTL/TTL logic levels (A port) and can be used as an alternate source for competitors' GTLP16612/GTLPH16612, GTLPH16912 or GTLP18T612 devices, where pin 50 is 5.0 V V_{CC} or 3.3 V BIAS V_{CC} or 3.3 V V_{CC} vs. pin 50 which is a no connect on the Philips device.

- Output capability: +64 mA/-32 mA on the LVTTL side; +40 mA on the GTLP side
- Edge rate control circuitry on the Bn outputs rising/falling edges to minimize system noise in a multi-point backplane environment
- Bus Hold on LVTTL I/Os
- No bus current loading when LVTTL output is tied to 5.0 V bus
- LVTTL input levels on control pins
- Supports hot insertion (I_{OFF} and Power-up 3-state)
- Positive edge triggered clock inputs
- JESD78ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 750 V (Bn I/O exceeds 1000 V) CDM per JESD22-C101
- Latch-up protection exceeds 500 mA per EIA/JEDS78
- Offered in 56-pin SSOP (DL) and TSSOP (DGG)

GTL1655 Features

The GTL1655 is a 16-bit bus transceiver that incorporates HIGH-drive LOW-output-impedance (100 mA/12 Ω) on the GTL I/O (B Port) and translates between GTL/GTLP signal levels and LVTTL/TTL logic levels (A Port). The GTL1655 is the transition device between the point to point GTL and multi-point GTLP families. The device is configured as two 8-bit transceivers that share a common clock and a master output enable pin, but also have individual latch timing, and output enable signals and can be used as an alternate source for competitors' GTL1655, GTLPH1655 or GTLP16T1655 devices.

- Output capability: +/- 24 mA on the LVTTL side; HIGH-drive LOW-output-impedance (100 mA/12 Ω) on the GTL side
- Configurable rise and fall times on B Port using V_{ERC} (pin 61)
- Bus Hold on LVTTL I/Os
- LVTTL input levels on control pins
- Supports live insertion (I_{OFF} , Power-up 3-state, and BIAS V_{CC})
- Minimized switching noise through use of distributed V_{CC} and GND pins
- J ESD78ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up protection exceeds 200 mA per EIA/JEDS78
- Offered in 64-pin TSSOP (DGG)

18-bit GTLP to LVTTL/TTL Bi-Directional Universal Translator
16-bit GTL/GTLP to LVTTL/TTL Bus Transceiver with Live Insertion

GTLPH16612
GTL1655

Operating Characteristics

- Operating voltage is 3.0 V to 3.6 V
- LVTTL I/Os and control inputs are 5.0 V I/O tolerant
- Operating temperature range is -40 °C to 85 °C
- Combination of D-type latches and D-type flip flops for transceiver operation in clocked, latched or transparent mode

GTLP permits 60 MHz – 80 MHz operation in multi-point applications with lower noise and lower EMI. GTLP functions similar to standard logic functions but with open drain outputs on the backplane side like GTL, FB or FBL devices that pull the signal low but require a pull up resistor for high level outputs. The GTLP B-Port backplane outputs are better suited for backplane applications than GTL, FB or FBL devices however since they have a slower edge rate that reduces ringing. The KEY to improved backplane operation using GTLP is matching the termination pull-up resistors (R_{TT}) with the loaded backplane trace impedance ($Z_{O(eff)}$), to ensure incident wave switching and excellent signal integrity. The pull-up termination resistor voltage (V_{TT}) is low (typically 1.5 V) reducing current loading when R_{TT} is equal to $Z_{O(eff)}$, which ranges from 21–40 Ω depending on the natural trace impedance, card spacing, stub length and device pin capacitance. The medium drive GTLPH16612 can support a R_{TT} as low as 40 Ω in a double terminated backplane and the high drive GTL1655 can support a R_{TT} as low as 22 Ω in a double terminated backplane.

The combination of reduced output swing (allows slower edge rates at higher frequencies) and small input threshold levels (reduces skew and increases noise margin) allows higher data rate transfers on GTLP backplanes. B-Port I/O is designed to operate at GTL (V_{TT} = 1.2 V, V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V, V_{REF} = 1.0 V) signaling levels. V_{REF} provides the reference voltage input that varies proportionally with V_{TT} by the use of the R/2R resistor combination. A-Port I/Os and the control inputs operate with LVTTL signal levels and are 5.0 V tolerant.

GTLP backplane construction is simple to implement and uses a pull up resistor on either side of the backplane trace instead of the typical Thevenin termination used for totem pole outputs. When all GTLP outputs connected to that trace are turned off there is no current drain, unlike the Thevenin termination where current is continuously flowing through the resistors. This reduces power consumption up to 50%. Additionally, since GTLP has open drain outputs, there can be multiple devices turned on for wired-OR operation without the danger of bus contention.

The GTLPH16612 is a universal translator with the same pinout as the 16601 standard logic function, except for the substitution the V_{REF} and the no connect (NC) pins for the B-Port V_{CC} pins, while the GTL1655 is similar to the 16501 standard logic function. The universal translator, through the use of the output enable, clock enable, clock and latch enable pins, can perform any of the standard logic functions shown in Table 1.

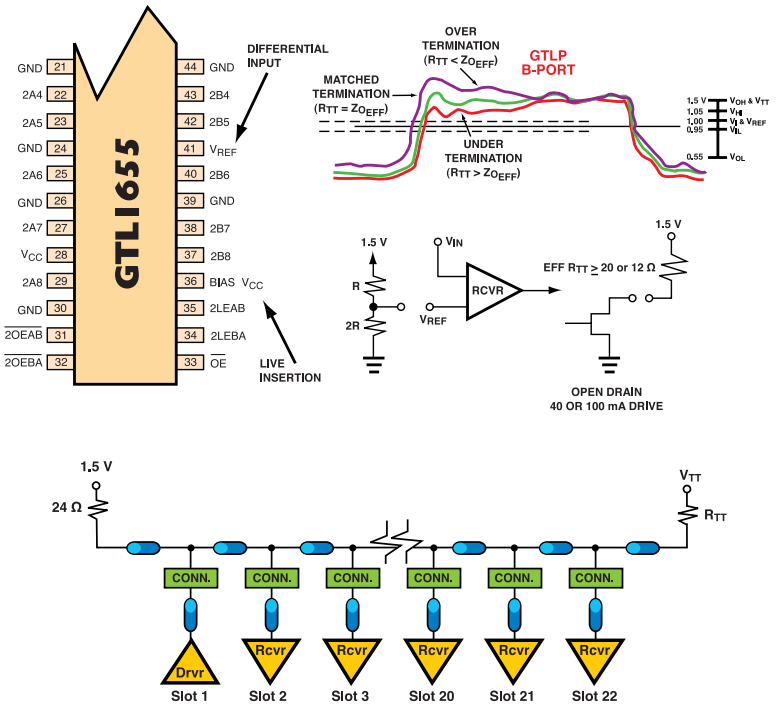

Table 1. Universal Translator Replacement Functions

Function	8-Bit	9-Bit	10-Bit	16-Bit	18-Bit
Transceiver	245, 623, 645	863	861	16245, 16623	16863
Buffer/driver	241, 244, 541		827	16241, 16244, 16541	16825
Latched transceiver	543			16543	16472
Latch	373, 573	843	841	16373	16843
Registered transceiver	646, 652			16646, 16652	16474
Flip-flop	374, 574		821	16374	
Standard UBT					16500/01
Universal bus driver					16835
Registered transceiver with clock enable	2952			16470, 16952	
Flip-flop with clock enable	377	823			16823
Standard UBT with clock enable					16600/01

Note: GTL 1655 functions in darker shaded area only

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