DATA SHEET

gm3020-NH/gm3020-H

Sections in this document and all other related documentation that mention HDCP refer only to the gm3020-H (HDCP-enabled) chip. All other sections apply to both the gm3020-H chip and the gm3020-HN (non-HDCP) chip.

C3020-DAT-01F

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Document History:

Revision	Description	Date
C3020-DAT-01A	Initial Release	June 2000
C3020-DAT-01B	Correction to PWM pin-out (pins 65-67)	August 2000
C3020-DAT-01C	Added Ultra-Reliable DVI™ and updated Electrical Characteristics tables	October 2000
C3020-DAT-01D	Removed references to SXGA	December 2000
C3020-DAT-01E	Added On-chip TCLK Oscillator description in Section 5.9	January 2001
C3020-DAT-01F	Added gm3020-NH and gm3020-H and changed all references to TMDS to DVI and updated section 8	October 2001

Related Documents:

Doc Number	Title	Date
C3020-DSR-01C	Programming Guide	February 2001

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1. OVERVIEW

The Genesis Microchip gm3020-NH/gm3020-H are the industry-leading single-chip scaling solution for digital LCD monitors for resolutions up to XGA. The gm3020-NH/gm3020-H, with the superb image quality of the Genesis' patented Advanced Image Magnification algorithm and the Ultra-Reliable DVI™ receiver for a direct digital connection, integrates all the necessary components required for a high quality digital LCD controller system in a single device.

With features such as High-bandwidth Digital Content Protection (HDCP 1.0) support plus the extra security of Genesis secret key encryption (gm3020-H only), built-in 10-bit gamma correction tables, color filtering in the YUV domain, RealColor™, that allows adjustment for brightness / contrast / hue / saturation / proprietary flesh-tone, programmable PWM control for backlight brightness, and a versatile multi-language On Screen Display (OSD) controller and the **Ultra-Reliable DVI™ receiver providing interoperability to all DVI compliant DVI transmitters**, the gm3020-NH/gm3020-H are the optimal, **low cost solution for Digital Visual Interface (DVI) compliant LCD Monitors.**

2. FEATURES & APPLICATIONS

FEATURES

- **High-quality advance image scaling engine**
  - Fully programmable zoom ratios.
  - Independent horizontal/vertical zoom.
  - Advanced zoom algorithm provides sharpest text images.
- **Ultra-Reliable DVI™ receiver**
  - Single channel DVI specification 1.0 compliant.
  - Supporting Ultra-Reliable DVI™ receiver.
  - Single-channel DVI (1.0) compliant.
  - Supporting input resolutions up to XGA 75Hz.
  - Direct connection to all DVI (1.0) compliant DVI transmitters.
- **High-Bandwidth Digital Content Protection (HDCP) Revision 1.0 Support (gm3020-H only)**
  - Added security of Genesis hardware-supported secret key encryption/decryption.
  - I²C bus for HDCP support.
- **Integrated On-Screen Display Controller**
  - Programmable OSD window size up to 32 by 16 characters.
  - Multi-language font ROM table with 256 characters.
  - Optional external OSD controller (gm3020-H only) can be supported for flexibility.
- **Image Color Controls**
  - Three 256 x 10 gamma lookup tables for color matching and calibration requirements for LCD panels.
  - Color temperature and brightness adjustments for reducing the difference of the color characteristics of various TFT LCD panels.
  - RGB888-to-YUV444 color-space converter allows contrast/brightness/hue/saturation/flesh-tone RealColor™ adjustments in YUV444 domain
- **Integrated High Speed Digital Clock**
  - All output frequencies are generated from a single 50 MHz reference oscillator.
  - Stand alone mode for factory testing and burn-in.
- **Optimized Panel Output Clock**
  - Panel clock frequency is optimized to support each mode at the lowest possible frequency.
  - Panel clock pad drive strength is programmable, also reducing EMI in the panel interface cable.
- **TFT LCD Panel Support**
  - All panel resolutions and sizes are supported up to XGA.
  - Panel interface supports one or two pixel per clock, Sync only, DE only and Sync/DE composite panels.
  - Panel output data dithering gives 18-bit/pixel panels more smoothly shaded colors.
- **Four Wire Interface to Microcontroller**
  - Simple 4 wire serial interface connects directly to monitor micro-controller.
- **Programmable PWM Outputs**
  - One programmable duty-cycle and one fixed 50% duty-cycle PWM outputs for panel backlight brightness control.
- **Standard 128 Pin LQFP Package**
  - XGA operations between 0°C to 70°C

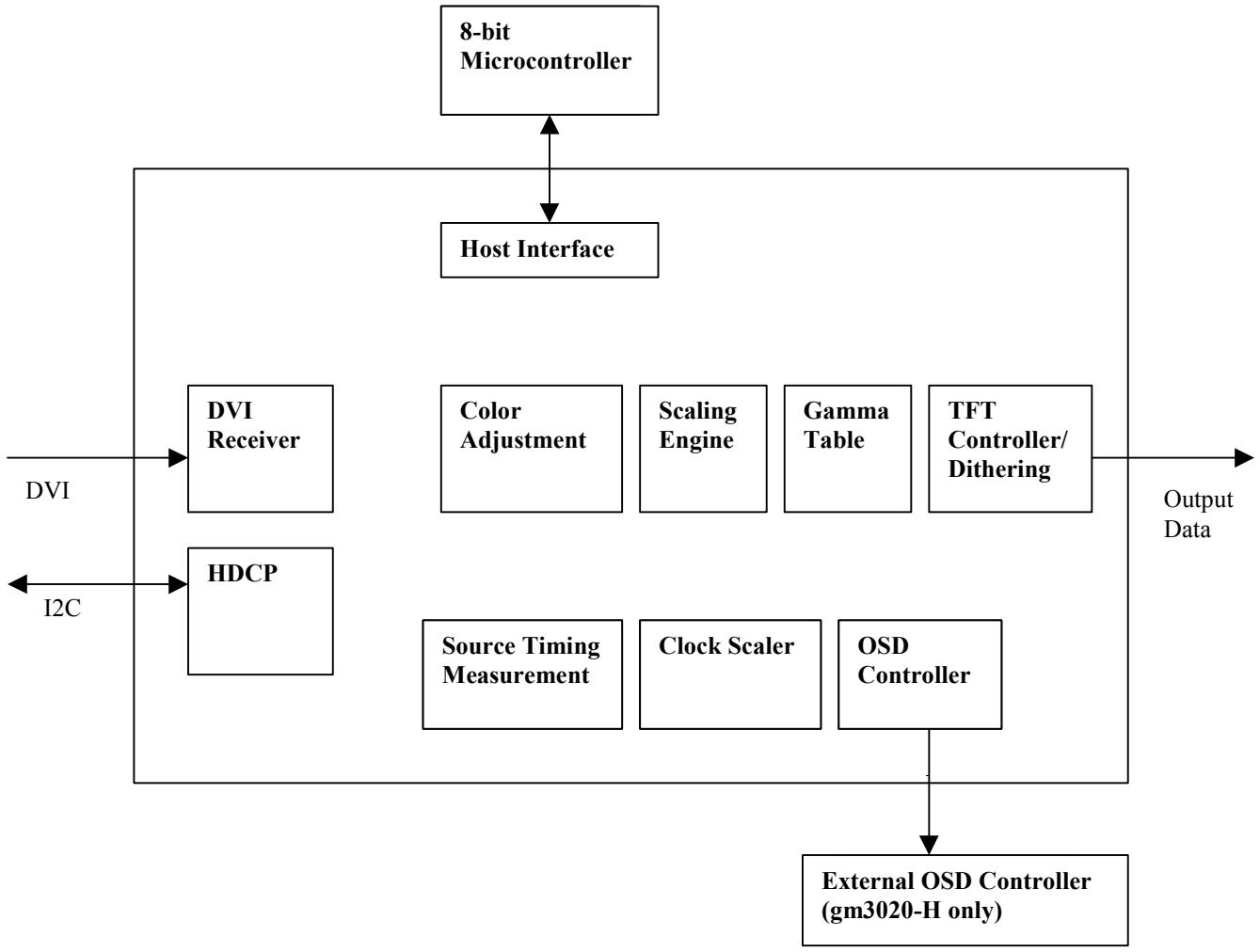
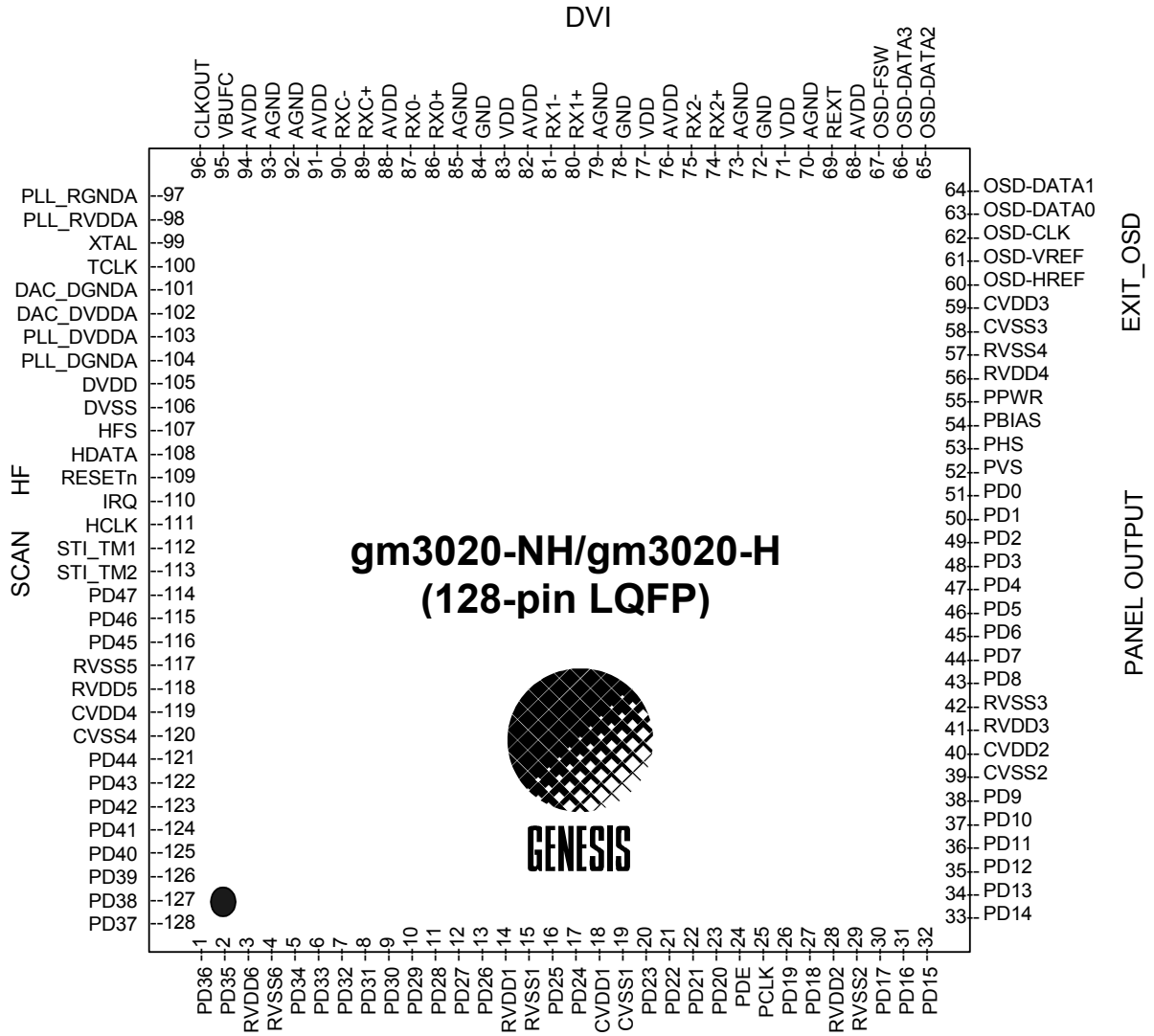


Figure 1: Single-Chip Solution for Low Cost Flat Panel Digital Interface Monitor

3. PINOUT

Figure 2: gm3020-NH/gm3020-H Pinout



3.1 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 1: Ultra-Reliable DVI™ Receiver

Pin No.	Name	In/Out	5V Tolerant Input ?	Description
68	AVDD			Analog VDD for internal biasing circuits. Must be bypassed with 100pF, 1nF and 10uF capacitors in parallel to pin 70.
69	REXT	In		External termination resistor. A 1% 1K ohm resistor should be connected from this pin to pin 68.
70	AGND			Analog GND for internal biasing circuits. Must be connected directly to the ground plane.
71	VDD			VDD for DVI input pair 0 logic circuits. Must be bypassed with 100pF, 1nF and 10uF capacitor to pin 72.
72	GND			GND for DVI input pair 0 logic circuits. Must be connected directly to the ground plane.
73	AGND			Analog GND for DVI input pair 0 input buffer. Must be connected directly to the analog ground plane.
74	RX2+	In		DVI input pair 2
75	RX2-	In		DVI input pair 2
76	AVDD			Analog VDD for DVI input pair 0 input buffer. Must be bypassed with 100pF capacitor to pin 73.
77	VDD			VDD for DVI input pair 1 logic circuits. Must be bypassed with100pF, 1nF and 10uF capacitor to pin 78.
78	GND			GND for DVI input pair 1 input buffer. Must be connected directly to the analog ground plane.
79	AGND			Analog GND for DVI input pair 1 input buffer. Must be connected directly to the analog ground plane.
80	RX1+	In		DVI input pair 1
81	RX1-	In		DVI input pair 1
82	AVDD			Analog VDD for DVI input pair 1 input buffer. Must be bypassed with 100pF capacitor to pin 79.
83	VDD			VDD for DVI input pair 2 logic circuits. Must
84	GND			GND for DVI input pair 2 logic circuits. Must be connected directly to the ground plane.
85	AGND			Analog GND for DVI input pair 2 input buffer. Must be connected directly to the analog ground plane.
86	RX0+	In		DVI input pair 0
87	RX0-	In		DVI input pair 0
88	AVDD			Analog VDD for DVI input pair 2 input buffer. Must be bypassed with 100pF capacitor to pin 85.
89	RXC+	In		DVI input clock pair
90	RXC-	In		DVI input clock pair
91	AVDD			Analog VDD for DVI input clock pair input buffer. Must be bypassed with 100pF capacitor to pin 92.
92	AGND			Analog GND for DVI input clock pair input buffer. Must be connected directly to the analog ground plane.

Pin No.	Name	In/Out	5V Tolerant Input ?	Description
93	AGND			Analog GND for the DVI receiver internal PLL. Must be connected directly to the analog ground plane.
94	AVDD			Analog VDD for the DVI receiver internal PLL. Must be bypassed with a capacitor to pin 93.
95	VBUFC	Out		For internal test purposes only.
96	CLKOUT	Out		For internal test purposes only.

Table 2: Host Interface (HIF), External On-Screen Display (EOSD), and General-Purpose I/O Bus (GPIO)

Pin No.	Name	In/Out	5V Tolerant Input	Description
107	HFS	In	5V tolerant	Active-high Host Frame Sync. Marks the beginning of the host interface data packet. This pin has an internal pull-down resistor..
108	HDATA	In/Out	5V tolerant /4mA	Host serial interface data signal input/output.
109	RESETn	In	5V tolerant	Resets the chip when low for at least 100 ns. Active low input.
110	IRQ	Out	4 mA	Interrupt request output.
111	HCLK	In	5V tolerant	Host Interface clock signal input.
60	OSD-HREF	Out	4 mA	HREF output for external OSD controller. *Note: This pin is a no-connect in gm3020-NH*
	Serial Data 1	In/Out	5V tolerant /4 mA	Used for HDCP and encrypted secret key storage. To be pulled up externally to +5V.
61	OSD-VREF	Out	4 mA	VREF output for external OSD controller.
	Serial Clock 1	In/Out	5V tolerant /4 mA	Used for HDCP and encrypted secret key storage. To be pulled up externally to +5V.
62	OSD-CLK	Out	4 mA	Clock output for external OSD controller
	GPIO bit 0	In/Out	5V tolerant /4 mA	General purpose I/O bus bit 0
63	OSD-DATA0	In	5V tolerant	Data input bit 0 from external OSD controller.
	GPIO bit 1	In/Out	5V tolerant /4 mA	General purpose I/O bus bit 1
64	OSD-DATA1	In	5V tolerant	Data input bit 1 from external OSD controller.
	GPIO bit 2	In/Out	5V tolerant /4 mA	General purpose I/O bus bit 2 When externally pulled down to ground, the internal oscillator is used; otherwise an external oscillator must be used.

65	OSD-DATA2	In	5V tolerant	Data input bit 2 from external OSD controller
	GPIO bit 3 PWM0	In/Out	5V tolerant /4 mA	General purpose I/O bus bit 3. This pin can also be configured as PWM output 0 for backlight brightness control. Its frequency is programmable, while its duty cycle is fixed at 50%.
66	OSD-DATA3	In	5V tolerant	Data input bit 3 from external OSD controller.
	GPIO bit 4 PWM1	In/Out	5V tolerant /4 mA	General purpose I/O bus bit 4; this pin is internally pulled up. This pin can also be configured as PWM output 1 for backlight brightness control. Its frequency is programmable, while its duty cycle is also programmable in 32 steps.
67	OSD-FSW	In	5V tolerant	External OSD window display enable. Displays data from external OSD controller when high.
	GPIO bit 5	In/Out	5V tolerant /4 mA	General purpose I/O bus bit 5; this pin is internally pulled up.

Table 3: Clock Recovery and Time Base Conversion

Pin No.	Name	In/Out	5V Tolerant Input	Description
97	PLL_RGNDA			Analog ground for the Reference PLL. Must be directly connected to the analog ground plane.
98	PLL_RVDDA			Analog power for the Reference PLL. Must be bypassed with a 0.1 uF capacitor to pin 97.
99	XTAL	Out		Output for external crystal. When external oscillator is used, this pin may be left open.
100	TCLK	In	5V tolerant	Reference clock (TCLK) input from external 50 MHz crystal oscillator.
101	DAC_DGNDA			Analog ground for Destination DDS DAC. Must be directly connected to the analog ground plane.
102	DAC_DVDDA			Analog power for Destination DDS DAC. Must be bypassed with a 0.1 uF capacitor to pin 101 (DAC_DGNDA)
103	PLL_DVDDA			Analog power for the Destination DDS PLL. Must be bypassed with a 0.1 uF capacitor to pin 104 (PLL_DGNDA)
104	PLL_DGNDA			Analog ground for Destination DDS PLL. Must be directly connected to the analog ground plane.
105	DVDD			Digital power for Destination DDS logic circuits. Must be bypassed with a 0.1 uF capacitor to pin 106 (DVSS)
106	DVSS			Digital ground for Destination DDS logic circuits. Must be directly connected to the ground plane.

Table 4: TFT Panel Interface

NOTE: Drive current of the panel output pins are programmable

Pin No.	Name	In/ Out	Output Drive Current @ 10pF	Description	TFT (one pixel/clock)			TFT (two pixels/clock)	
					8 bit	6 bit	4 bit	8 bit	6 bit
114	PD47	Out	2mA~20mA	Panel data output 47				OB7	OB5
115	PD46	Out	2mA~20mA	Panel data output 46				OB6	OB4
116	PD45	Out	2mA~20mA	Panel data output 45				OB5	OB3
121	PD44		2mA~20mA	Panel data output 44				OB4	OB2
122	PD43	Out	2mA~20mA	Panel data output 43				OB3	OB1
123	PD42	Out	2mA~20mA	Panel data output 42				OB2	OB0
124	PD41	Out	2mA~20mA	Panel data output 41				OB1	
125	PD40	Out	2mA~20mA	Panel data output 40				OB0	
126	PD39	Out	2mA~20mA	Panel data output 39				OG7	OG5
127	PD38	Out	2mA~20mA	Panel data output 38				OG6	OG4
128	PD37	Out	2mA~20mA	Panel data output 37				OG5	OG3
1	PD36	Out	2mA~20mA	Panel data output 36				OG4	OG2
2	PD35	Out	2mA~20mA	Panel data output 35				OG3	OG1
5	PD34	Out	2mA~20mA	Panel data output 34				OG2	OG0
6	PD33	Out	2mA~20mA	Panel data output 33				OG1	
7	PD32	Out	2mA~20mA	Panel data output 32				OG0	
8	PD31	Out	2mA~20mA	Panel data output 31				OR7	OR5
9	PD30	Out	2mA~20mA	Panel data output 30				OR6	OR4
10	PD29	Out	2mA~20mA	Panel data output 29				OR5	OR3
11	PD28	Out	2mA~20mA	Panel data output 28				OR4	OR2
12	PD27	Out	2mA~20mA	Panel data output 27				OR3	OR1
13	PD26	Out	2mA~20mA	Panel data output 26				OR2	OR0
16	PD25	Out	2mA~20mA	Panel data output 25				OR1	
17	PD24	Out	2mA~20mA	Panel data output 24				OR0	
20	PD23	Out	2mA~20mA	Panel data output 23	B7	B5	B3	EB7	EB5
21	PD22	Out	2mA~20mA	Panel data output 22	B6	B4	B2	EB6	EB4
22	PD21	Out	2mA~20mA	Panel data output 21	B5	B3	B1	EB5	EB3
23	PD20	Out	2mA~20mA	Panel data output 20	B4	B2	B0	EB4	EB2
26	PD19	Out	2mA~20mA	Panel data output 19	B3	B1		EB3	EB1
27	PD18	Out	2mA~20mA	Panel data output 18	B2	B0		EB2	EB0
30	PD17	Out	2mA~20mA	Panel data output 17	B1			EB1	
31	PD16	Out	2mA~20mA	Panel data output 16	B0			EB0	
32	PD15	Out	2mA~20mA	Panel data output 15	G7	G5	G3	EG7	EG5
33	PD14	Out	2mA~20mA	Panel data output 14	G6	G4	G2	EG6	EG4
34	PD13	Out	2mA~20mA	Panel data output 13	G5	G3	G1	EG5	EG3
35	PD12	Out	2mA~20mA	Panel data output 12	G4	G2	G0	EG4	EG2
36	PD11	Out	2mA~20mA	Panel data output 11	G3	G1		EG3	EG1
37	PD10	Out	2mA~20mA	Panel data output 10	G2	G0		EG2	EG0
38	PD 9	Out	2mA~20mA	Panel data output 9	G1			EG1	
43	PD 8	Out	2mA~20mA	Panel data output 8	G0			EG0	
44	PD 7	Out	2mA~20mA	Panel data output 7	R7	R5	R3	ER7	ER5
45	PD 6	Out	2mA~20mA	Panel data output 6	R6	R4	R2	ER6	ER4
46	PD 5	Out	2mA~20mA	Panel data output 5	R5	R3	R1	ER5	ER3
47	PD 4	Out	2mA~20mA	Panel data output 4	R4	R2	R0	ER4	ER2

NOTE: Drive current of the panel output pins are programmable

Pin No.	Name	In/ Out	Output Drive Current @ 10pF	Description	TFT (one pixel/clock)			TFT (two pixels/clock)	
					8 bit	6 bit	4 bit	8 bit	6 bit
48	PD 3	Out	2mA~20mA	Panel data output 3	R3	R1		ER3	ER1
49	PD2	Out	2mA~20mA	Panel data output 2	R2	R0		ER2	ER0
50	PD1	Out	2mA~20mA	Panel data output 1	R1			ER1	
51	PD0	Out	2mA~20mA	Panel data output 0	R0			ER0	
24	PDE	Out	2mA~20Ma	Panel Display Enable signal, active when flat panel data is valid.					
53	PHS	Out	2mA~20mA	This output provides the panel line clock signal.					
52	PVS	Out	2mA~20mA	This output provide the panel frame start signal.					
25	PCLK	Out	2mA~20mA	This output drives the flat panel shift clock.					
55	PPWR	Out	8 mA	This output controls the power to a flat panel.					
54	PBIAS	Out	8 mA	This output turns on/off the panel bias power or controls panel backlight.					

Table 5: Pin-Scan Test Pins

Pin No.	Name	In/Out	5V Tolerant Input?	Description
112	STI_TM1	In	5V tolerant	Internal test pin.
113	STI_TM2	In	5V tolerant	Internal test pin.

Table 6: Power and Ground Pins

Pin No.	Name	Description
14	RVDD1	Pad Ring VDD. Bypass with a 0.1 uF capacitor to RVSS pins.
28	RVDD2	Pad Ring VDD. Bypass with a 0.1 uF capacitor to RVSS pins.
41	RVDD3	Pad Ring VDD. Bypass with a 0.1 uF capacitor to RVSS pins.
56	RVDD4	Pad Ring VDD. Bypass with a 0.1 uF capacitor to RVSS pins.
118	RVDD5	Pad Ring VDD. Bypass with a 0.1 uF capacitor to RVSS pins.
3	RVDD6	Pad Ring VDD. Bypass with a 0.1 uF capacitor to RVSS pins.
15	RVSS1	Pad Ring VSS. Connect directly to ground plane.
29	RVSS2	Pad Ring VSS. Connect directly to ground plane.
42	RVSS3	Pad Ring VSS. Connect directly to ground plane.
57	RVSS4	Pad Ring VSS. Connect directly to ground plane.
117	RVSS5	Pad Ring VSS. Connect directly to ground plane.
4	RVSS6	Pad Ring VSS. Connect directly to ground plane.
18	CVDD1	Core VDD. Bypass with a 0.1 uF capacitor to CVSS pins.
40	CVDD2	Core VDD. Bypass with a 0.1 uF capacitor to CVSS pins.
59	CVDD3	Core VDD. Bypass with a 0.1 uF capacitor to CVSS pins.
119	CVDD4	Core VDD. Bypass with a 0.1 uF capacitor to CVSS pins.
19	CVSS1	Core VSS. Connect directly to ground plane.
39	CVSS2	Core VSS. Connect directly to ground plane.
58	CVSS3	Core VSS. Connect directly to ground plane.
120	CVSS4	Core VSS. Connect directly to ground plane.

4. OPERATING MODES

The Source Clock (SCLK) and the Destination Clock (DCLK) are defined as follows:

- The Source Clock is the pixel clock encoded in the DVI channel. It is the pixel clock of data coming from the source.
- The Destination Clock is the timing clock for panel data at the one pixel per clock rate. The actual clock to the panel (PCLK) may be one-half that frequency for double-pixel panel data formats. When its frequency differs from that of the Source Clock, the Destination Clock is generated by the Clock Generation Block.

There are six display modes: Native, Slow DCLK, Expansion, Downscaling, Source Stand Alone, and Destination Stand Alone.

Each mode is unique in terms of:

- Input video resolution vs. panel resolution
- Source Clock frequency / Panel Clock frequency ratio
- Source Hsync frequency / Panel Hsync frequency ratio
- Data source (video input, panel background color, on-chip pattern generator).

4.1 Native Mode

Destination clock frequency = Source clock frequency

Panel Hsync frequency = Input Hsync frequency

Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution and the input data clock frequency is within the panel clock frequency specification of a panel being used.

4.2 Slow DCLK Mode

Destination clock frequency < Source clock frequency

Panel Hsync frequency = Input Hsync frequency

Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution, but the input data clock frequency exceeds the panel clock frequency specification of a panel being used. The panel clock is scaled to the Source clock, and the internal data buffers are used to spread the timing of the input data by making use of the large blanking period to extend the panel horizontal display time.

4.3 Expansion Mode

Destination clock frequency > Source clock frequency

Panel Hsync frequency > Input Hsync frequency

Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is less than the panel resolution. The panel clock (at a higher frequency than the source clock) is scaled and locked to the source clock. The input data is expanded.

4.4 Downscaling Mode

Destination clock frequency > Source clock frequency

Panel Hsync frequency < Input Hsync frequency

Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is greater than the panel resolution, and is used to provide enough of a display to enable the user to recover to a supported resolution. The input clock is operated at a frequency less than that of the input pixel rate (under-sampled horizontally) and the expander function is used to drop input lines. Expansion interpolation is not provided and must be off.

4.5 Source Stand Alone Mode

Destination clock = SCLK

Panel Hsync frequency = SCLK frequency / (Source Htotal register value)

Panel Vsync frequency = SCLK frequency / (Source Htotal register value * Source Vtotal register value)

This mode is used to display the Pattern Generator data. This mode may be useful for testing an LCD panel on the manufacturing line (color temperature calibration, etc.).

4.6 Destination Stand Alone Mode

Destination clock = DCLK in open loop (not locked)

Panel Hsync frequency = DCLK frequency / (Destination Htotal register value)

Panel Vsync frequency = DCLK frequency / (Destination Htotal register value * Destination Vtotal register value)

This mode is used when the input is changing or not available. The OSD may still be used as in all other display modes, and stable panel timing signals are produced. This mode may be automatically set when the gm3020-NH/gm3020-H detects input timing changes that could cause out-of-spec operation of the panel. This mode can also be used with the internal static patterns for manufacturing line burn-in testing.

4.7 Input Video Mode Support

The gm3020-NH/gm3020-H can support various standard VGA / VESA / Macintosh display modes, depending on the LCD panel specifications. By default, all data input is expanded to full-panel screen resolution. ModeCALC.EXE, an application running under DOS / Microsoft Windows, is available from Genesis Microchip. ModeCALC.EXE calculates and displays the mode supported based on user-supplied panel parameters.

5. FUNCTIONAL BLOCK DESCRIPTION

The figure below shows a high-level block diagram of the gm3020-NH/gm3020-H chip.

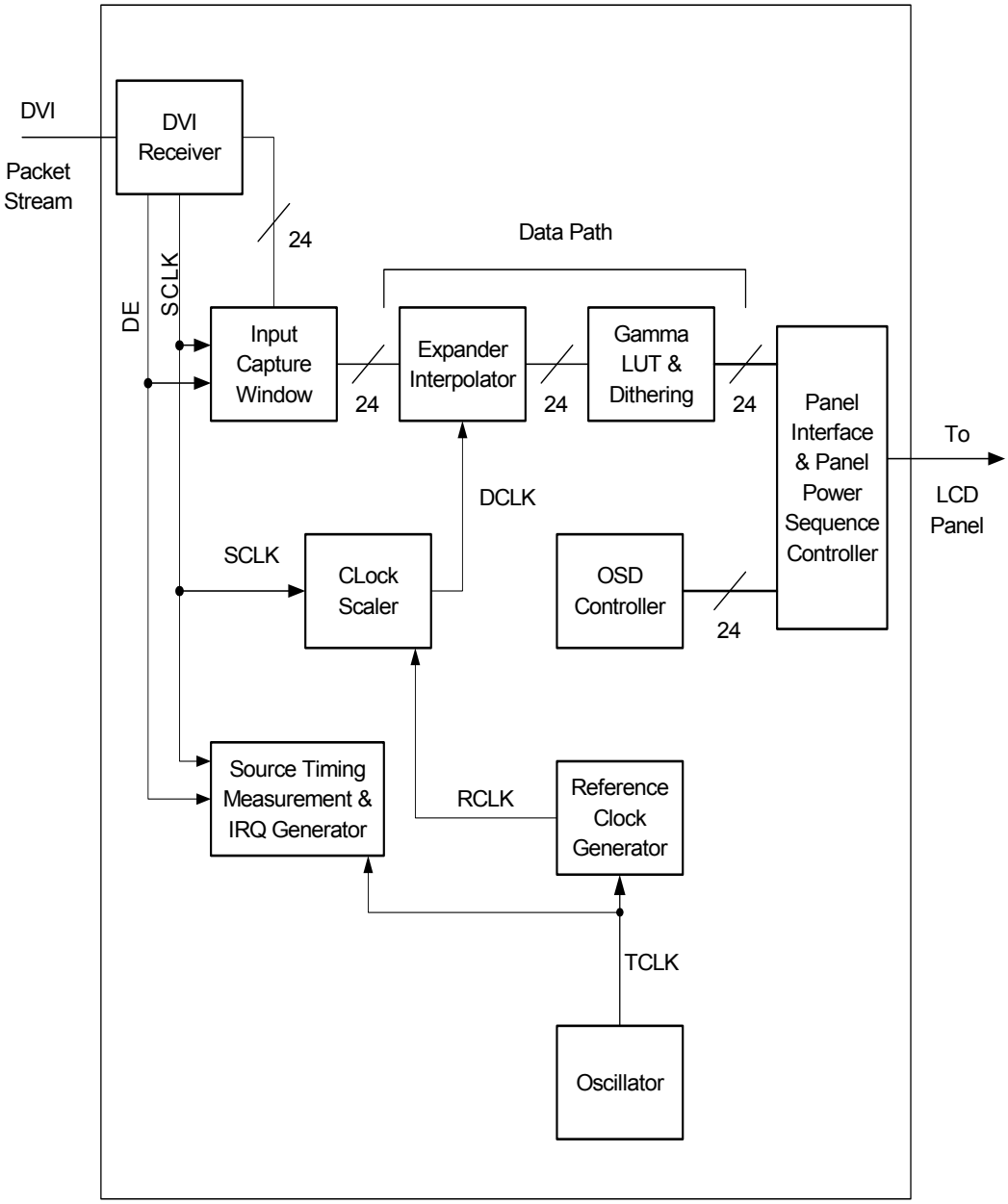


Figure 3: gm3020-NH/gm3020-H Block Diagram

5.1 Ultra-Reliable DVI™ Receiver Block

The Ultra-Reliable DVI™ receiver block of the gm3020-NH/gm3020-H is compliant with DVI 1.0 specifications. It supports an input clock frequency ranging from 20 MHz - 112 MHz. The typical input clock frequency used would be up to 79MHz (XGA 75Hz).

The DE PLL re-generates an internal DE (data-enable) signal from the input DE to ensure that periodic occurrences of a DVI 1.0-induced glitch do not cause the firmware to generate unwanted timing change events.

Table 7 summarizes the characteristics of the four Receiver Pair inputs:

Table 7: Receiver Characteristics

	MIN	TYP	MAX	NOTE
DC Characteristics				
Differential Input Voltage	150mV		1200mV	
Input Common Mode Voltage	AVDD–300mV		AVDD-37mV	
Behavior when Transmitter Disable	AVDD-10mV		AVDD+10mV	
AC Characteristics				
Input clock frequency	20 MHz		112 MHz	
Input differential sensitivity (Peak-to-peak)	150mV			
Max differential input (peak-to-peak)			1560 mV	
Allowable Intra-Pair skew at Receiver			360 ps	Input clock = 112 MHz
Allowable Inter-Pair skew at Receiver			5.4 ns	Input clock = 112 MHz
Worst case differential input clock jitter tolerance			270 ps	Input clock = 112 MHz

Through register programming, the receiver unit may be placed in three states:

- **Active:** The receiver block is fully on and running.
- **Standby:** Only the RXC channel remains active. Data and other control signals do not get decoded.
- **Off:** The receiver block is powered down.

Input clock frequency (or loss of the input clock) may be detected in active mode or in standby mode. The input DE status is detected only in active mode.

The CTL3:0 signals from the DVI channel can be output from pins by programming the EXT_OSD_MUX_CONTROL register.

The internal static pattern can be displayed only if a source clock is present. The source clock may be supplied through pin pair RXC± of the DVI link, or the test bus. (Configured through register 0xF0.)

5.2 Input Capture/Timing Measurement Blocks

Decoded input data and timing signals are sent from the Ultra-Reliable DVI™ receiver block to the input capture block and to the input timing measurement block. Among the input timing signals, Hsync input and Vsync input from the DVI receiver block are ignored. Only the DE input is used. The Hsync and Vsync signals are synthesized from the DE input and sent to the input capture/timing measurement blocks.

5.2.1. Input Capture Block

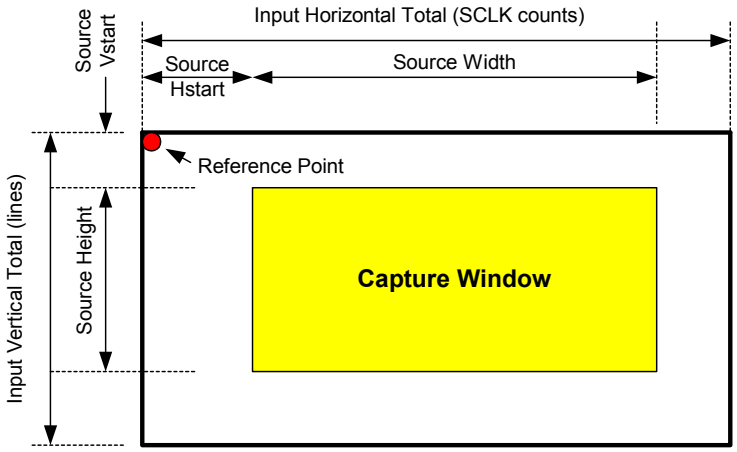


Figure 4 below shows how the window is defined. In the horizontal direction, it is defined in SCLK (input clock from the receiver block) counts and in the vertical direction, in line counts.

All parameters in Figure 4 beginning with "Source" are programmed into the gm3020-NH/gm3020-H registers. Note that horizontal / vertical totals are solely determined by the video input. In other words, the horizontal / vertical counters are cleared by the synthesized Hsync/Vsync signals. Hence, they have the prefix "Input" instead of "Source."

The reference points are as follows:

The first pixel of a line: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.

The first line of a frame: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

Note that above Hsync/Vsync signals are synthesized from the DE input from the receiver block.

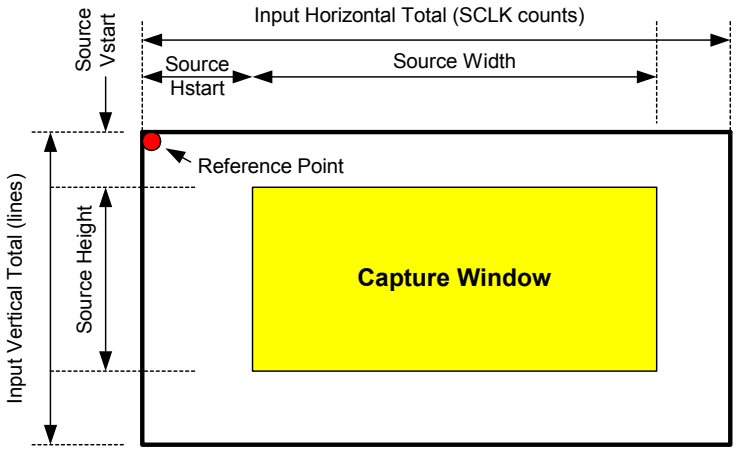


Figure 4: Capture Window

5.2.2. Input Timing Measurement Block

The input timing measurement block consists of the source timing measurement (STM) block and interrupt request (IRQ) controller.

Input timing parameters are measured by the STM block and stored in the registers. Some input conditions will generate an IRQ to an external microcontroller. The IRQ-generating conditions are programmable.

5.2.2.1. Source timing measurement (STM) block

The table below lists all the parameters that may be read in the source timing measurement (STM) registers of gm3020-NH/gm3020-H.

Table 8: Input Timing Parameters Measured by the STM Block

Parameter	Unit	Updated at:
Unstable vertical timing Current v-period different from the last one	N/A	Every frame (This flag can be disabled.)
Unstable horizontal timing (Current h-period different from the last one)	N/A	Every line (This flag can be disabled.)
Unstable SCLK	N/A	Every 256 TCLK periods (This flag can be disabled.)
Unstable DE(Current DE width/height different from the last one)	N/A	Every line horizontally, Every frame vertically
Synthesized Hsync missing	N/A	Every 4096 TCLK periods

Parameter	Unit	Updated at:
Synthesized Vsync missing	N/A	Every 80 ms
Horizontal Period (period between two synthesized Hsync)	SCLKs	Every Frame
Horizontal Display Start (DE rising edge)	SCLKs	Every Frame
Horizontal Display End (DE falling edge)	SCLKs	Every Frame
Vertical Period (period between two synthesized Vsync)	Lines	Every Frame
Vertical Display Start (First DE of a frame)	Lines	Every Frame
Vertical Display End (Last DE of a frame)	Lines	Every Frame

5.2.2.2. IRQ controller

Some input timing conditions can cause the gm3020-NH/gm3020-H chip to generate an IRQ. The IRQ-generation conditions are programmable as follows:

Table 9: IRQ-Generation Condition

IRQ Event	Remark
Timing Event	Each leading edge of synthesized Vsync input
Timing Change	Any of the following timing changes: 1. Unstable SCLK (SCLK delta threshold is programmable) 2. Unstable horizontal timing 3. Unstable vertical timing 4. Loss of synthesized Hsync or Vsync 5. Loss of SCLK

Reading the IRQ status flags will not affect the STM registers.

Note that if a new IRQ event occurs while the IRQ status register is being read, the IRQ signal will become inactive for a minimum of one TCLK period and before being re-activated. The polarity of the IRQ signal is programmable.

The gm3020-NH/gm3020-H may be programmed to automatically switch to the Destination Standalone operation upon unstable input timing detection without intervention by the firmware.

5.3 Clock Scaling Block

The clock scaling block of the gm3020-NH/gm3020-H chip scales the input clock from the Ultra-Reliable DVI™ receiver block (SCLK) to the output clock (DCLK). The data path, OSD controller, and the panel interface run in synchronization with DCLK.

The clock scaling is performed so that the output frame period is equal to the input frame period.

Input frame period = SCLK period * input horizontal total * input vertical total

Output frame period = DCLK period * output horizontal total * output vertical total

Thus, the ratio of SCLK period to DCLK period is:

SCLK period/DCLK period = output horz. total * output vert. total / (input horz. total * input vert. total)

The following block diagram shows how the gm3020-NH/gm3020-H generates the DCLK from SCLK and TCLK input. The TCLK input comes from an external oscillator.

5.4 Data Path

The gm3020-NH/gm3020-H data path is shown in the following diagram:

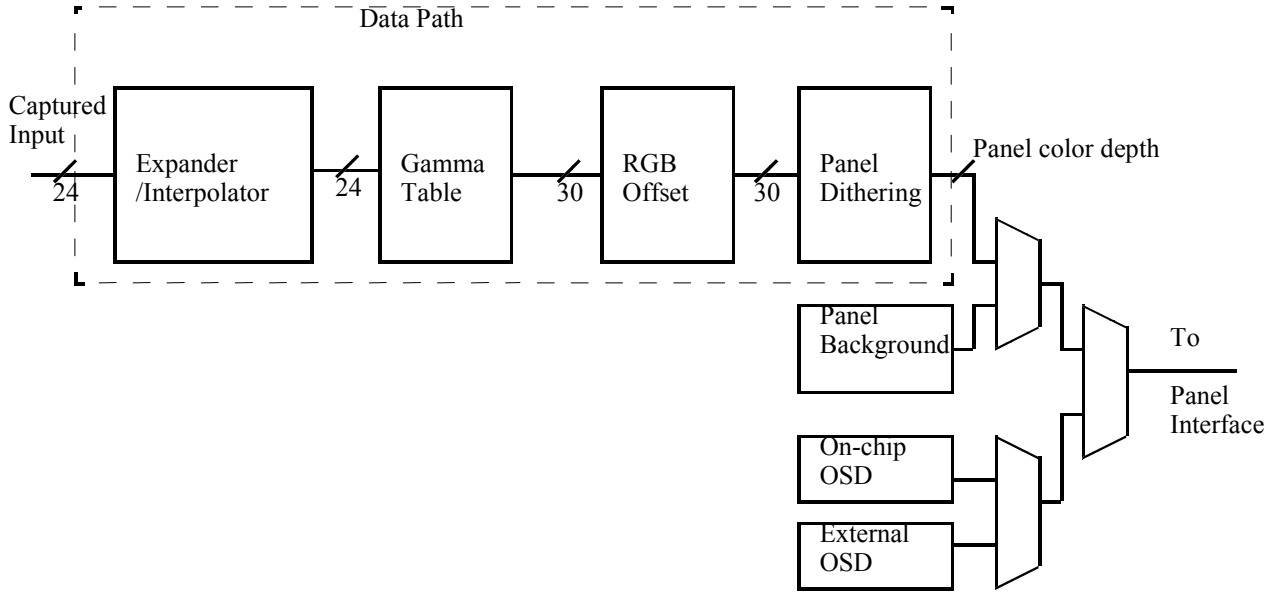


Figure 6: Data Path

5.5 Gamma Table

This Gamma Lookup Table takes the 8-bit R, G, and B data from the DVI receiver block and produces a 10-bit output. This table can be programmed to adjust color temperature/contrast or to reduce the difference of color characteristics of various LCD TFT panels.

5.5.1. Expander Interpolator

For the best display quality when the source resolution is less than the panel resolution, the gm3020-NH/gm3020-H provides an advanced data interpolator. The calculation finds the best output value for the horizontally and vertically expanded output data. The expander block takes in the 8-bit output from the input capture block and produces an 8-bit output. The vertical and horizontal expansion amounts are independently programmable.

5.5.2. RGB Offset

The RGB offsets provide a simple shift (positive or negative) for each of the three color channels. This may be used as a simple brightness adjustment within a limited range. The data is clamped to zero for negative offsets, and clamped to FFh for positive offsets. This adjustment is much faster than recalculating the gamma table, and may be used with in OSD user controls to provide a quick brightness adjust. An offset range of plus 127 to minus 127 is available.

Because the gamma table output is 10 bits per channel, two 0's are appended as the least significant bits of these 8-bit RGB offsets to produce 10-bit output for each channel.

5.5.3. Panel Data Dither

For TFT panels that have fewer than eight bits for each R, G, B input, the gm3020-NH/gm3020-H provides a dither pattern to more smoothly shade colors on 4 and 6 bit panels. The dithering logic is identical to that of the gmZAN1 or gmZ4.

5.5.4. Panel Background Color

This provides a solid background color for a border around any partial expansion display data, or for the Destination Stand Alone Mode. The background color is most often set to black.

5.6 Panel Interface

The gm3020-NH/gm3020-H chip interfaces directly with all of today's commonly used TFT LCD flat panels with 640x480, 800x600 and 1024x768 resolutions. The resolution and the aspect ratio are NOT limited to specific values.

All aspects of the gm3020-NH/gm3020-H panel interface are programmable. For horizontal parameters, Horizontal Display Enable Start, Horizontal Display Enable End, Horizontal Sync Start and Horizontal Sync End are programmable. Vertical Display Enable Start, Vertical Display Enable End, Vertical Sync Start and Vertical Sync Start are also fully programmable.

In order to maximize panel data setup and hold time, the panel clock (PCLK) output skew is programmable. In addition, the current drive strength of the panel interface pins are programmable.

For panel backlight brightness control, there are two PWM outputs available (as part of the GPIO bus). One PWM output has a fixed 50% duty cycle, while the second PWM output has programmable duty cycle.

The following sections describe these functions in detail.

5.6.1. TFT Panel Interface Timing Specification

The TFT panel interface timing parameters are listed in the table below. Refer to the timing diagrams in Figure 7 (one pixel per clock) and Figure 8 for the timing parameter definitions.

Table 10: gm3020-NH/gm3020-H TFT Panel Interface Timing

Note: [ ] figures are for two pixels/clock mode

Signal Name			Min	Typical	Max	Unit [*1]
PVS	Period	t1	0		2048	Lines
				16.67	-	ms
	Frequency			60	-	Hz
	Front porch	t2	0		2048	lines
	Back porch	t3	0		2048	lines
	Pulse width	t4	0		2048	lines
	PdispE	t5	0	Panel height	2048	lines
	Disp. Start From VS	t6	0		2048	lines
	PVS set-up to PHS	t18	1		2048	pclk
	PVS hold from PHS	t19	1		2048	pclk

PHS	Period	t7	0		2048 [1024]	pclk
	Front porch	t8	0		2048	pclk
	Back porch	t9	0		2048	pclk
	Pulse width	t10	0		2048	pclk
	PdispE	t11	0	Panel width	2048 [1024]	pclk
	Disp. Start from HS	t12	0		2048	pclk
PCLK [*4]	Frequency	t13			112 [56]	MHz
	Clock (H) [*2]	t14	DCLK/2-3 [DCLK – 3]		DCLK/2 - 2 [DCLK - 2]	ns
	Clock (L) [*2]	t15	DCLK/2-3 [DCLK – 3]		DCLK/2 - 2 [DCLK - 2]	ns
	Type			One pels/clock [two pels/clock]	-	
Data	Set up [*3]	t16	DCLK/2 - 5 [DCLK – 5]		DCLK/2 - 2 [DCLK - 2]	
	Hold [*3]	t17	DCLK/2 - 5 [DCLK – 5]		DCLK/2 - 2 [DCLK - 2]	
	Width		12 bits [24 bits]	18 bits [36 bits]	24 bits [48 bits]	Bits/pixel

NOTES:

1: The pclk is the panel shift clock.

2: The DCLK (Destination Clock) period. is equal to:
- pclk period in one pixel/clock mode,
- twice the pclk period in two pixels/clock mode.

The drive current of the panel interface signals is programmable as shown in Table 12. Output current is programmable from 2 mA to 20 mA in increments of 2 mA. Drive strength should be programmed to match the load presented by the cable and input of the panel.

3: The same setup/hold time specification to the pclk also applies to the PHS and the PDE signals. The setup time (t16) and the hold time (t17) listed in this table are for the case in which no clock-to-data skew is added: The PVS/PHS/PDE/ PData signals are asserted on the rising edge of the PCLK.

Note that the polarity of the PCLK and its skew are programmable. Clock to Data skew can be adjusted in sixteen 800-ps increments. In combination with the Pclk polarity inversion, the clock-to-data phase can be adjusted in total of 31 steps.

4: The polarity of the PCLK is programmable.

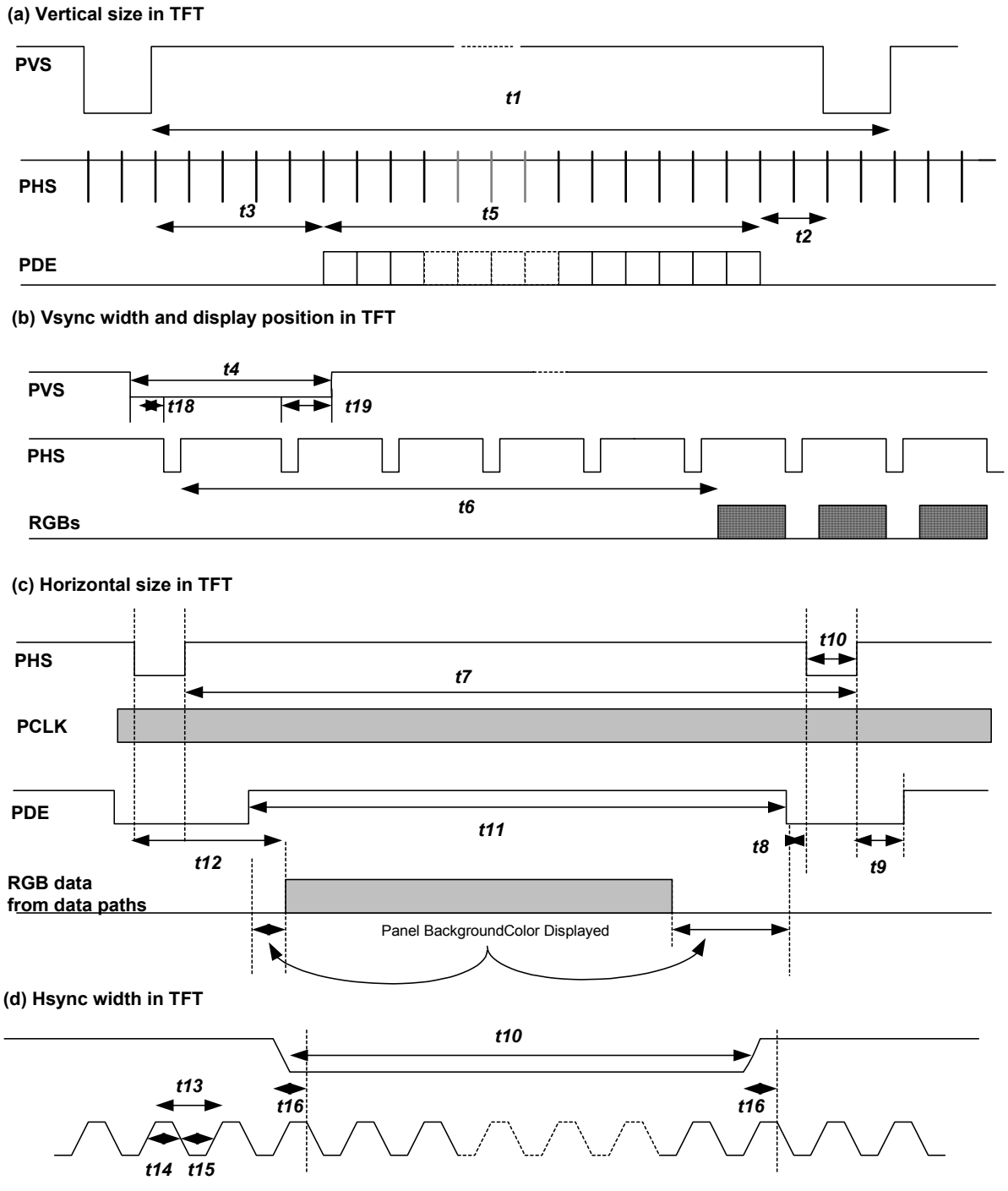
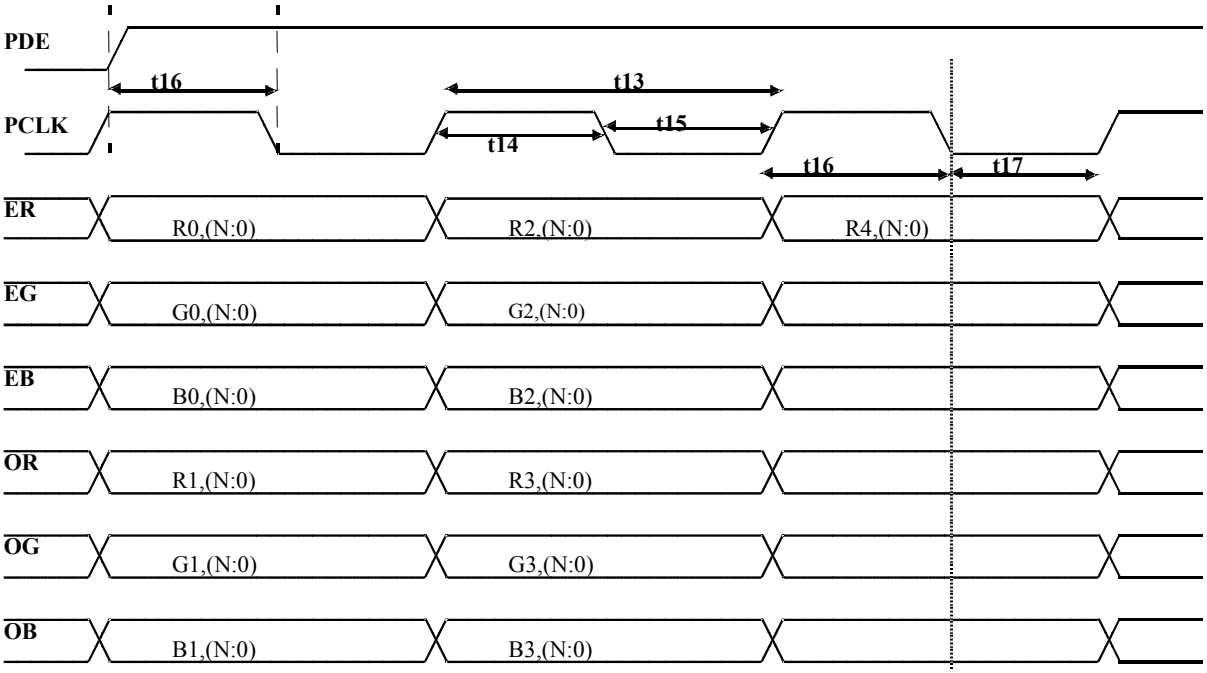


Figure 7: TFT Panel Interface Timing (one pixel per clock)

(a) Two pixel per clock mode in TFT



(b) One pixel per clock mode in TFT

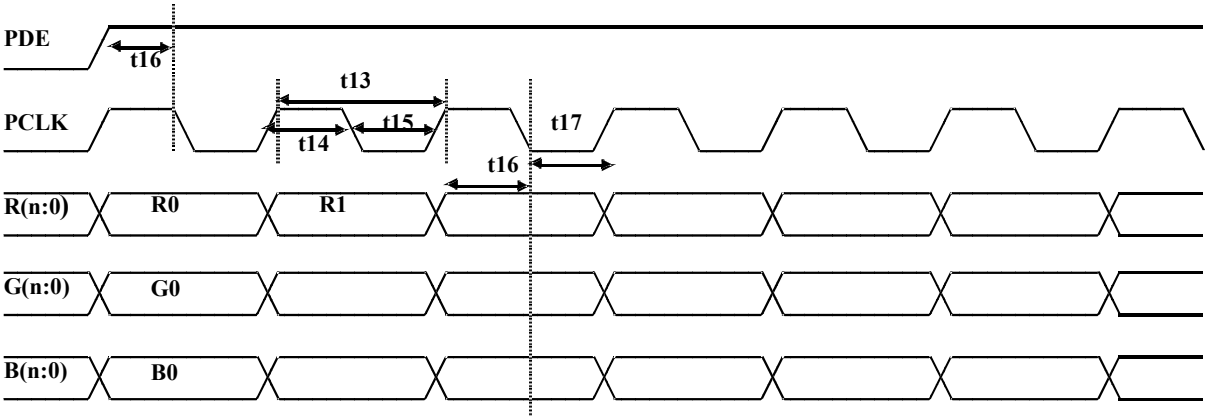


Figure 8: TFT Panel Interface Data Latch Timing

5.6.2. TFT LCD Power Sequencer

LCD panels require logic power, panel bias power, and control signals to be sequenced in a specific order. Otherwise, a severe damage may occur and disable the panel permanently. The gm3020-NH/gm3020-H has a built-in power sequencer, which should prevent this kind of damage.

The Power Sequencer controls the power up/down sequences for LCD panels within the four states described below. Also see the timing diagram in Table 11.

State 0 (Power Off)

The PBIAS signal and the PPWR signal are low (inactive). The panel controls and data are forced low. This state is both the beginning and final state in power sequence.

State 1 (Power On)

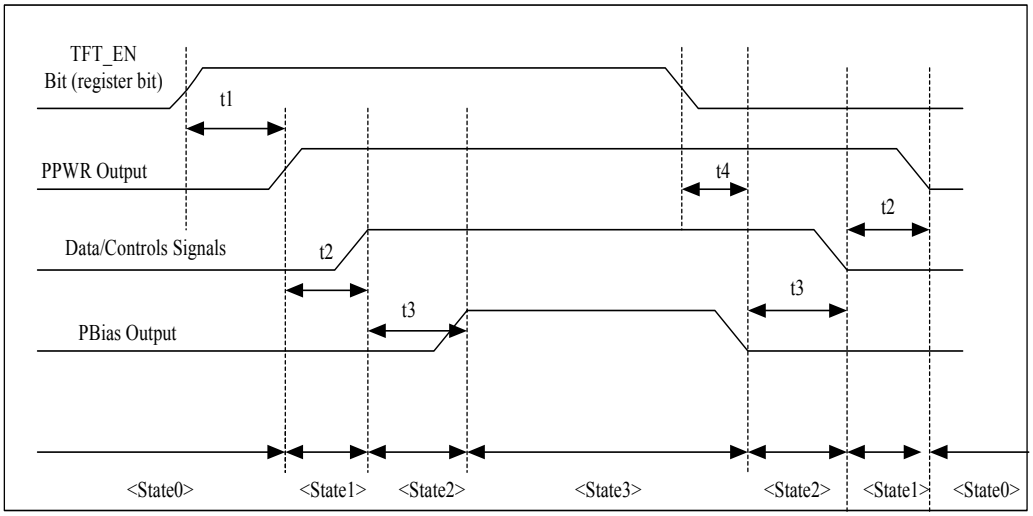
Intermediate step 1. The PPWR is high (active), the PBIAS is low (inactive), and the panel interface is forced low (inactive).

State 2 (Panel Drive Enabled)

Intermediate step 2. The PPWR is high (active), the PBIAS is low (inactive), and the panel control and data signals are active.

State 3 (Panel Fully Active)

Final step in power up sequence with PPWR and PBIAS high (active), and the panel interface active. gm3020-NH/gm3020-H power manager is kept in this state until the internal TFT_Enable signal is disabled and State 2 is entered.



The power sequence state can be read from a gm3020-NH/gm3020-H status register.

All of the four timing parameters (t1 ~ t4) in Table 11 are independently programmable from one step to eight steps in length.

One-step length is TCLK * $\mathbf{2}^{\mathbf{19}}$ or about 10 ms when TCLK is 50 MHz.

Table 11: Panel Power Sequence Timing Definition

Timing Symbol	Description
t1	TFT_EN bit set to 1 PPWR active
t2	PPWR active to Signals active (power up) or Signals inactive to PPWR inactive (power down)
t3	Signals active to PBIAS active (power up) or PBIAS inactive to Signals inactive (power down)
t4	TFT_EN bit cleared to 0 to PBIAS inactive

5.6.3. Panel Interface Drive Strength

The gm3020-NH/gm3020-H has programmable output pads for the TFT panel interface. Three groups of panel interface pads (panel clock, data, and control) are independently controlled by programming registers.

Table 12: Panel Interface Pad Drive Strength

Value (4 bits)	Drive Strength
0	Outputs are in tri-state condition
1	2 mA
2	4 mA
3, 4	6 mA
5, 8	8 mA
6, 9	10 mA
7, 10	12 mA
11, 12	14 mA
13	16 mA
14	18 mA
15	20 mA

5.7 Host Interface

The host interface uses a serial protocol consisting of four signals as described in this section.

5.7.1. Host interface pin connection

Table 13: gm3020-NH/gm3020-H Host Interface

Signal Name	Description
HFS	Host Frame Sync. that enable the serial communication when driven high by the microcontroller. The gm3020-NH/gm3020-H chip has an internal pull-down resistor on chip. Thus, the default state of this signal is low.
HCLK	Serial clock driven by the microcontroller in the write operation. May be connected to an external pull-up resistor.
HDATA	Address is sent by the microcontroller to the gm3020-NH/gm3020-H. Data is driven: by the microcontroller in the write operation. by the gm3020-NH/gm3020-H in the read operation.
IRQ	IRQ pin driven by the gm3020-NH/gm3020-H chip. The polarity is programmable.
RESETn	Sets the chip to a known state when pulled low.

The gm3020-NH/gm3020-H has an on-chip pull-down resistor in the HFS input pad. The signal stays low until driven high by the microcontroller.

RESETn must be low for at least 100 ns after the CVDD has become stable (between +3.15V and +3.45V) to reset the chip to a known state.

5.7.2. gm3020-NH/gm3020-H Serial Communication Protocol

During serial communication between the microcontroller and the gm3020-NH/gm3020-H, the microcontroller always acts as an initiator while the gm3020-NH/gm3020-H is always the target. The following timing diagram describes the protocol of the serial channel

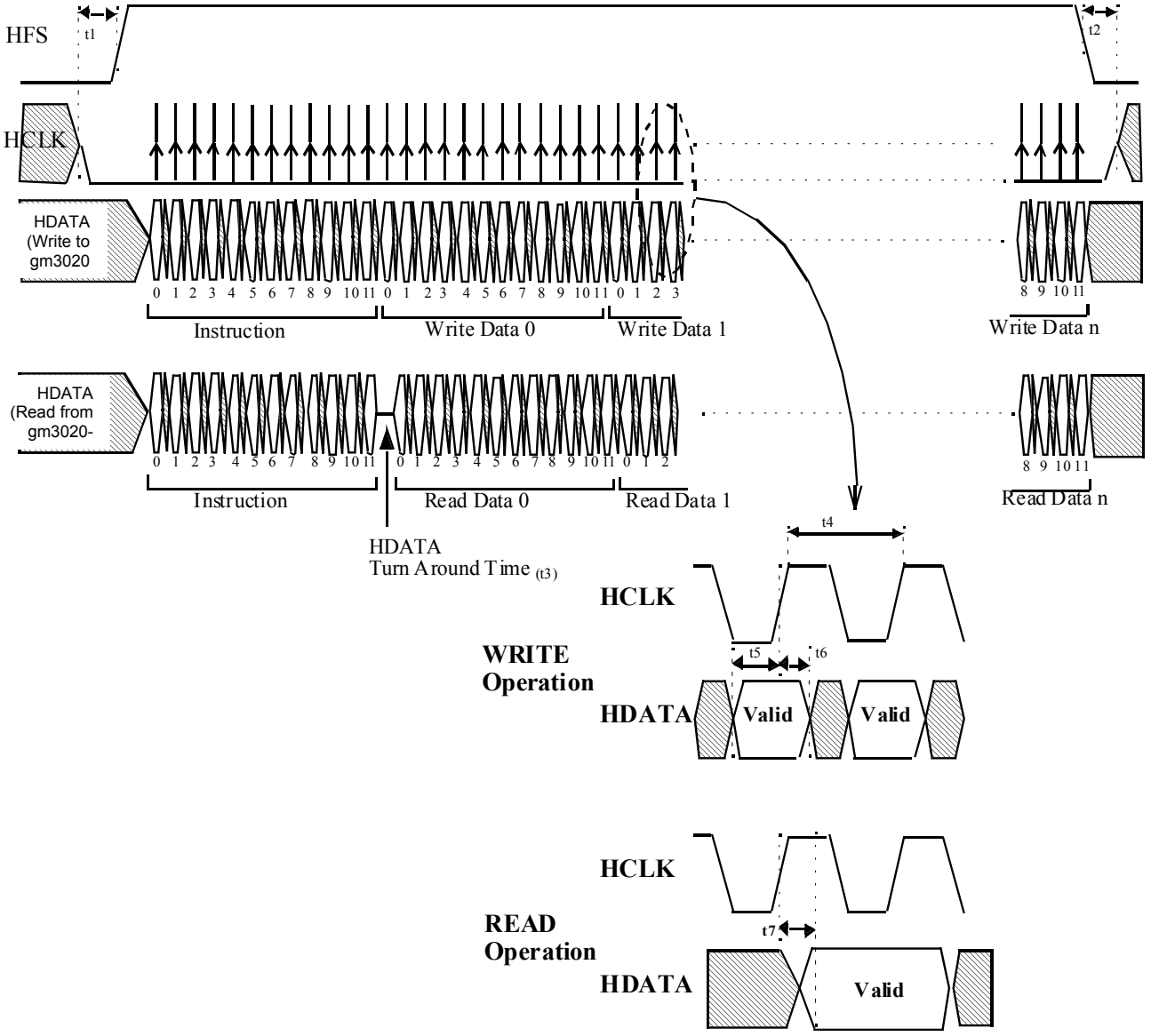


Figure 9: Serial Communication Timing Diagram

Table 14 summarizes the serial channel specification of the gm3020-NH/gm3020-H. Refer to Figure 9 for the timing parameter definitions.

Table 14: gm3020-NH/gm3020-H Serial Channel Specification

Parameter	Min.	Typ.	Max.
Word size (Instruction and Data)	----	12 bits	----
HCLK low to HFS high (t1)	100 ns		
HFS low to HCLK inactive (t2)	100 ns		
HDATA Write to Read Turnaround Time (t3)	1 HCLK cycle		1 HCLK cycle
HCLK cycle (t4)	100 ns		
Data in setup time (t5)	25 ns		
Data in hold time (t6)	25 ns		
Data out valid (t7)	5 ns		10 ns

The microcontroller (Initiator) issues an instruction lasting 12 HCLKs. After the last bit of the command is transferred to the gm3020-NH/gm3020-H on the 12th clock, the microcontroller must stop driving data before the next rising edge of HCLK, at which point the gm3020-NH/gm3020-H will start driving data if it is a read operation. At the 13th rising edge of HCLK, the gm3020-NH/gm3020-H will begin driving data.

The data order for address, read data or write data is:

- D11 on the first clock

- D0 on the twelfth clock

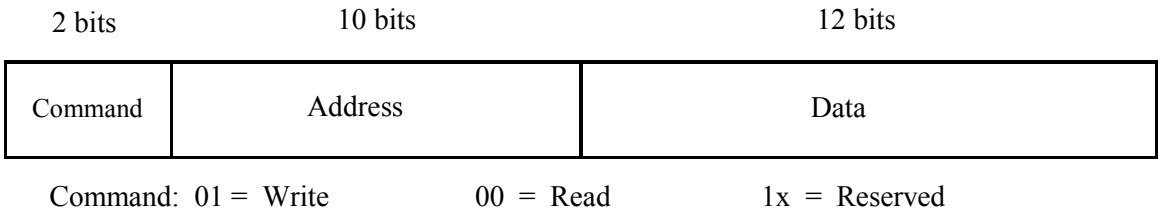


Figure 10: Serial Host Interface Data Transfer Format

5.8 OSD (On-Screen Display) Control

The gm3020-NH/gm3020-H chip has a built-in OSD (On-Screen Display) controller with an integrated block of font ROM. The built-in OSD controller can display an OSD window of up to 32 x 16 characters.

The gm3020-H also supports an external OSD controller as an option for monitor vendors to maintain a familiar user interface.

Regardless of whether the built-in OSD or an external OSD is enabled, the window size is not affected by the expansion operation.

5.8.1. On-Chip OSD

Features of the gm3020-NH/gm3020-H's on-chip OSD controller include: character blinking, OSD window shadowing, OSD window bordering and background transparency. In addition, the OSD window can be pixel or line doubled independently.

There are 256 built-in ROM fonts. The size of each font is 12 pixels x 16 lines.

The on-chip, 512-byte OSD SRAM is used as a display buffer. This display buffer is contiguously accessed through the 0x100-0x1ff register range of the gm3020-NH/gm3020-H. One bit in the OSD_Control register selects one of two segments accessed through the 0x100-0x1ff window.

Table 15: On-chip Character Code

Blinking Enable	Foreground/ Background Colors	Font Select
Bit 10 0 = Disable 1 = Enable	Bit 9 – Bit 8 00 = F/Bcolor 0 01 = F/Bcolor 1 10 = F/Bcolor 2 11 = F/Bcolor 3	Bit 7 – B 0 Selects a font from 256-font ROM

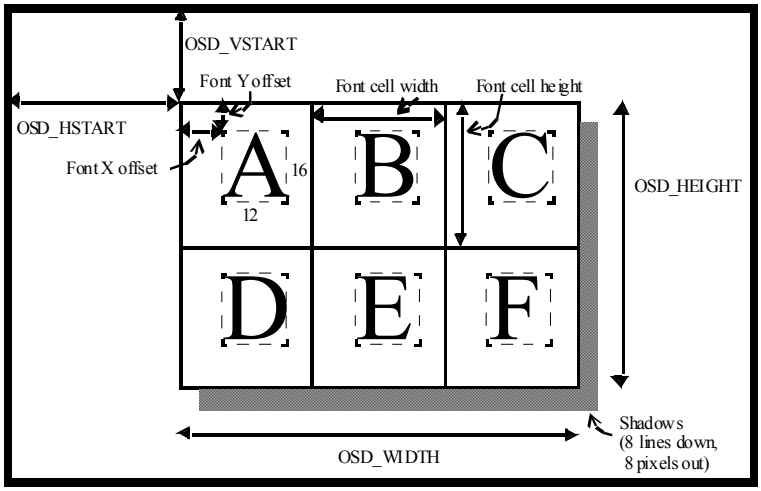
The blink rate is based on either a 32 or 64 frame cycle and the duty cycle may be selected as 25/75, 50/50 or 75/25.

The on-chip OSD colors are controlled by the foreground or background color selected. The foreground and background colors are stored in registers. Each location contains 12 bits that define the upper 4 bits of each 8 bit Red, Green and Blue color component. If any of the upper 4 RGB bits are set to 1, then the corresponding lower four RGB bits are all set to 1, otherwise the lower four RGB bits are set to 0.

Table 16: On-chip OSD Color Control

Register Index	Color Selected
0xBA	Foreground 0<R7:4><G7:4><B7:4> (Bits 11:8 = R7:4, Bits 7:4 = G7:4, Bits 3:0 = B7:4)
0xBB	Foreground 1<R7:4><G7:4><B7:4>
0xBC	Foreground 2<R7:4><G7:4><B7:4>
0xBD	Foreground 3<R7:4><G7:4><B7:4>
0xBE	Background 0<R7:4><G7:4><B7:4>
0xBF	Background 1<R7:4><G7:4><B7:4>
0xC0	Background 2<R7:4><G7:4><B7:4>
0xC1	Background 3<R7:4><G7:4><B7:4>

Foreground / background colors may be independently made transparent via register 0xB9 bits7:0.



OSD_HSTART: Starting pixel number 0-2047

OSD_VSTART: Starting line number 0-2047

Font X offset: Location of left pixel of font inside char cell 0-63

Font Y offset: Location of top line of font inside char cell 0-63

Font Cell Width: Cell width in pixels 3-66

Font Cell Height: Cell height in lines 2-65

OSD_Width: OSD Window Width in char cells 1-64

OSD_Height: OSD Window Height in char cells 1-64

Figure 11: On-Chip OSD Window Location

When the OSD window shadow is enabled, a shadow region the same size as the OSD, but shifted down and to the right by eight pixels/lines is shown. Data on the panel is at half intensity in the shadow region. OSD foreground and background colors will always appear on top of the shadow region but the transparent background color will be 'lost' in the shadow since it is also half intensity.

When the OSD window border is enabled, a 1, 2, 4 or 8 pixel/line wide border is drawn around the OSD window. In this case, the OSD vertical and horizontal start positions include the thickness of the border and the actual start of the character display is offset from the start position by the thickness of the border. If the OSD window border is enabled, the OSD window shadow must be disabled. Only one may be selected at a time.

If the Cell Height or Cell Width is larger than the 12 x 16 font, the extra pixels and lines in each cell will display as the background color of that cell's character code. If the Cell Height or Cell Width is smaller than the 12 x 16 font, the cell will clip the right most pixels and the bottom lines of the font.

Following page:

Figure 12: gm3020-NH/gm3020-H On-chip Fonts in ROM

Index	Font	Index	Font	Index	Font	Index	Font	Index	Font	Index	Font
00		2C	,	58	X	84	ま	B0	垂	DC	
01		2D	−	59	Y	85	る	B1	直	DD	
02		2E	.	5A	Z	86	ん	B2	曲	DE	
03		2F	/	5B	の	87	ぞ	B3	像	DF	
04		30	0	5C	他	88	ア	B4	入	E0	
05		31	1	5D	回	89	オ	B5	力	E1	
06		32	2	5E		8A	ワ	B6	信	E2	
07		33	3	5F	⊕	8B	コ	B7	号	E3	
08		34	4	60	⊖	8C	サ	B8	輝	E4	
09		35	5	61	a	8D	シ	B9	音	E5	
0A		36	6	62	b	8E	ス	BA	言	E6	
0B		37	7	63	c	8F	セ	BB	語	E7	
0C		38	8	64	d	90	タ	BC	日	E8	
0D		39	9	65	e	91	テ	BD	本	E9	
0E		3A	:	66	f	92	ト	BE	表	EA	
0F		3B	●	67	g	93	ナ	BF	示	EB	
10		3C	<	68	h	94	フ	C0	無	EC	
11		3D	=	69	i	95	マ	C1	質	ED	
12		3E	>	6A	j	96	ラ	C2	グ	EE	
13		3F	?	6B	k	97	リ	C3	ル	EF	
14		40	O	6C	l	98	ロ	C4	ᴿᴳ	F0	
15		41	A	6D	m	99	ン	C5	ᵍʸ	F1	
16		42	B	6E	n	9A	ェ	C6	⊕	F2	
17		43	C	6F	o	9B	ッ	C7	ノ	F3	
18		44	D	70	p	9C	ョ	C8	匚	F4	
19		45	E	71	q	9D	ガ	C9	刁	F5	
1A		46	F	72	r	9E	ジ	CA		F6	
1B		47	G	73	s	9F	ズ	CB		F7	
1C		48	H	74	t	A0	デ	CC		F8	
1D		49	I	75	u	A1	プ	CD		F9	
1E		4A	J	76	v	A2	ポ	CE	保	FA	
1F		4B	K	77	w	A3	明	CF	存	FB	
20		4C	L	78	x	A4	色	D0	力	FC	
21	™	4D	M	79	y	A5	調	D1	一	FD	
22	"	4E	N	7A	z	A6	整	D2		FE	
23		4F	O	7B	←	A7	赤	D3		FF	Æ
24		50	P	7C	↓	A8	緑	D4	選		
25	%	51	Q	7D	→	A9	青	D5	量		
26	&	52	R	7E	↑	AA	温	D6	択		
27	'	53	S	7F	⚠	AB	度	D7			
28	(	54	T	80	き	AC	位	D8			
29	)	55	U	81	さ	AD	置	D9			
2A	®	56	V	82	し	AE	水	DA			
2B	+	57	W	83	せ	AF	平	DB			

5.8.2. External OSD Support (gm3020-H only)

The gm3020-H supports an external OSD controller for monitor vendors who wish to maintain a specific user interface, or its look and feel. Only those OSD controllers that are developed for a flat-panel monitor application and have a pixel-clock input pin are supported.

An external OSD controller is connected to the gm3020-H chip as shown in Table 17.

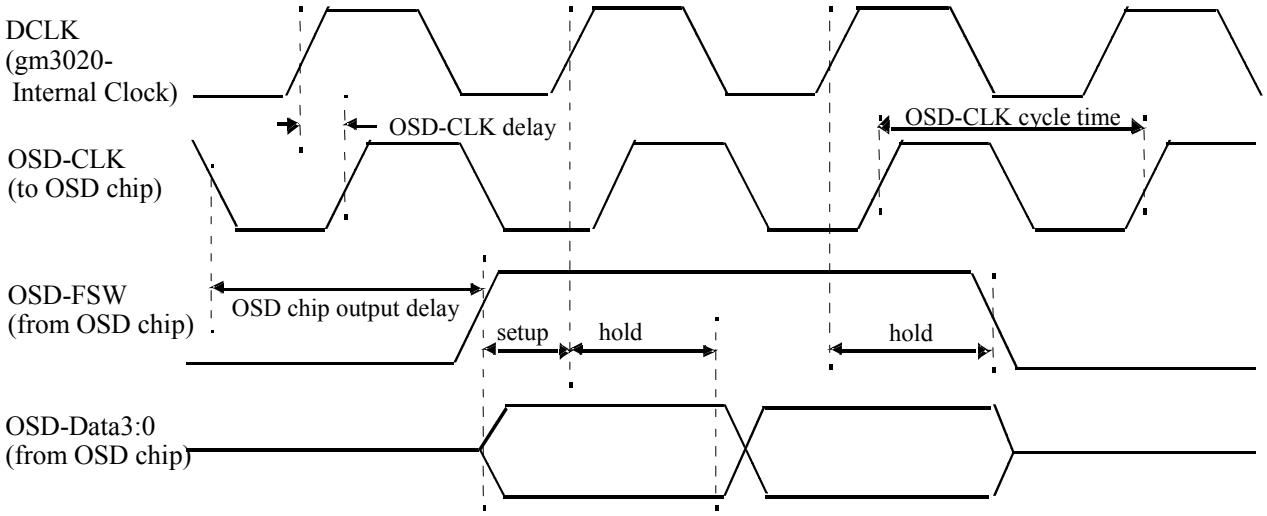
Table 17: Pin Connection Between the gm3020-H and an External OSD controller

Pin Name (in/out)	External OSD Controller Pin (in/out)	Polarity	Position
OSD-HREF (output)	Hsync (input)	Programmable	Relative to left edge of panel. Leading edge of PDE.
OSD-VREF (output)	Vsync (input)	Programmable	Relative to top edge of panel. Leading edge of first PDE after vertical blanking period.
OSD-CLK (output)	Pixel Clock (input)		
OSD-FSW (input)	OSD Window Indicator (output)	Programmable	Horizontal: M OSD-CLK cycles after the HREF for N pixels. Vertical: M' HREF pulses after the VREF for N' lines. (M, N, M', N' programmed to external OSD chip)
OSD-DATA [3:0] (inputs)	Intensity, R, G, and B (outputs)		

The four-bit data from an external OSD controller becomes one of the 16 entries to the OSD look-up table (LUT), which is 12 bits wide and contains the upper four bits (D7:4) of each color component. The lower four bits are determined as follows to make a full 8 bit color value:

D [7:4]	D [3:0]
0000b	0000b
If any bit = 1	1111b

The eight pins of the external OSD interface can be configured as general purpose I/O pins or CTL3:0 output pins.



OSD-CLK delay = 3 ns default. Additional 0 ~ 12 ns delay can be added.

OSD-FSW/OSD-DATA setup/hold time = 1.5 ns min.

OSD-CLK cycle time = DCLK cycle time = 110 MHz max.

Figure 13: External OSD Interface Data Latch Timing

When the external OSD controller interface is enabled, the data from the OSD LUT is displayed on a TFT panel in place of the captured input data, whenever the OSD-FSW signal is active.

The OSD-CLK output to an external OSD controller chip is derived from the DCLK (destination clock) whose clock frequency is the same as the panel clock frequency (or twice the panel clock frequency on a two-pixels-per-clock panel). The maximum frequency is 112 MHz. The OSD-CLK can be divided down by a factor of two or four from DCLK, which doubles or quadruples each OSD pixel on the display.

Both the OSD Data and OSD-FSW signals are latched by the gm3020-H on the rising edge of DCLK. To maximize the setup/ hold time for the OSD-Data and OSD-FSW signal, an internal programmable delay of up to 12 ns in sixteen 800 ps increments is available.

To maximize OSD-HREF setup/hold time to the external OSD controller chip, an internal programmable delay is available to delay OSD-HREF up to 12 ns in sixteen 800 ps increments.

Table 18: External OSD Interface Timing Parameters

Parameter	Minimum	Typical	Maximum
OSD-CLK Frequency			112 MHz
OSD-FSW/OSD-DATA setup time	1.5 ns		
OSD-FSW/OSD-DATA hold time	1.5 ns		
OSD-CLK delay from DCLK		0 ~ 12 ns, programmable in 16 800-ps increments	
OSD-HREF delay from DCLK		0 ~ 12 ns, programmable in 800-ps increments	
OSD-CLK/DCLK ratio		1/4x, 1/2x, 1x, programmable	

The external-OSD window position is referenced to the edge of the OSD-HREF and OSD-VREF. The horizontal start position is defined in terms of OSD-CLK pulse counts. The vertical position is defined in terms of OSD-HREF pulse counts. These values are programmed into an external OSD controller chip.

5.9 On-chip TCLK Oscillator

The gm3020-NH/gm3020-H on-chip TCLK oscillator circuitry is a custom designed circuit to support the use of an external oscillator or a crystal resonator to generate a reference frequency source for the gm3020-NH/gm3020-H device. When used with an external crystal resonator, the oscillator circuit was designed to provide a very low jitter and very low harmonic clock to the internal circuitry of the gm3020-NH/gm3020-H. The on-chip oscillator circuit also minimizes the overdrive of the crystal, which reduces the aging of the crystal.

The Requirements for the TCLK signal is listed below:

Table 19: TCLK Specifications

Frequency	20 MHz ~ 50 MHz
Jitter	250 ps maximum
Rise Time (10 % to 90 %)	5 ns
Duty Cycle	40 – 60

5.9.1. External Oscillator mode

The first mode of operation of the TCLK circuitry is the external oscillator mode. When the gm3020-NH/gm3020-H is in reset, the state of the OSD-DATA1 (pin 64) is sampled. If the pin is pulled high to Vdd (there is an internal 60K Ohm pull up resistor on this pin) the external oscillator mode is enabled. In this mode the internal oscillator circuit is disabled and the external oscillator signal that is connected to the TCLK (pin 100) is routed to an internal clock buffer as shown in figure 6.

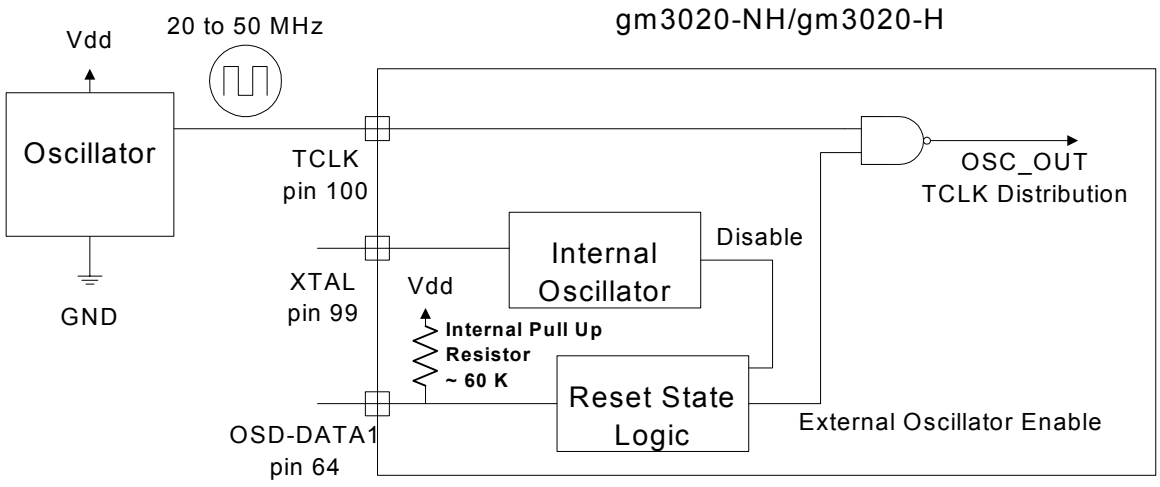


Figure 14: Using an External Oscillator

5.9.2. Internal Oscillator mode

The second mode of operation for the TCLK circuitry is the internal oscillator mode. When the gm3020-NH/gm3020-H is in reset, the state of the pin OSD-DATA1 (pin 64) is sampled. If the pin is pulled low by connecting the pin directly to GND, or by connecting the pin to GND through a pull down resistor, the internal oscillator is enabled. The maximum value of the pull down resistor is 15K Ohm. In this mode an external crystal resonator is connected between the XTAL (pin 99) and the TCLK (pin 100) with the appropriately sized loading capacitors C_{L1} and C_{L2}. The size of C_{L1} and C_{L2} are determined from the crystal manufacture's specification and by compensating for the parasitic capacitance of the gm3020-NH/gm3020-H device and the printed circuit board traces. The loading capacitors are terminated to the Vdda power supply. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to ground.

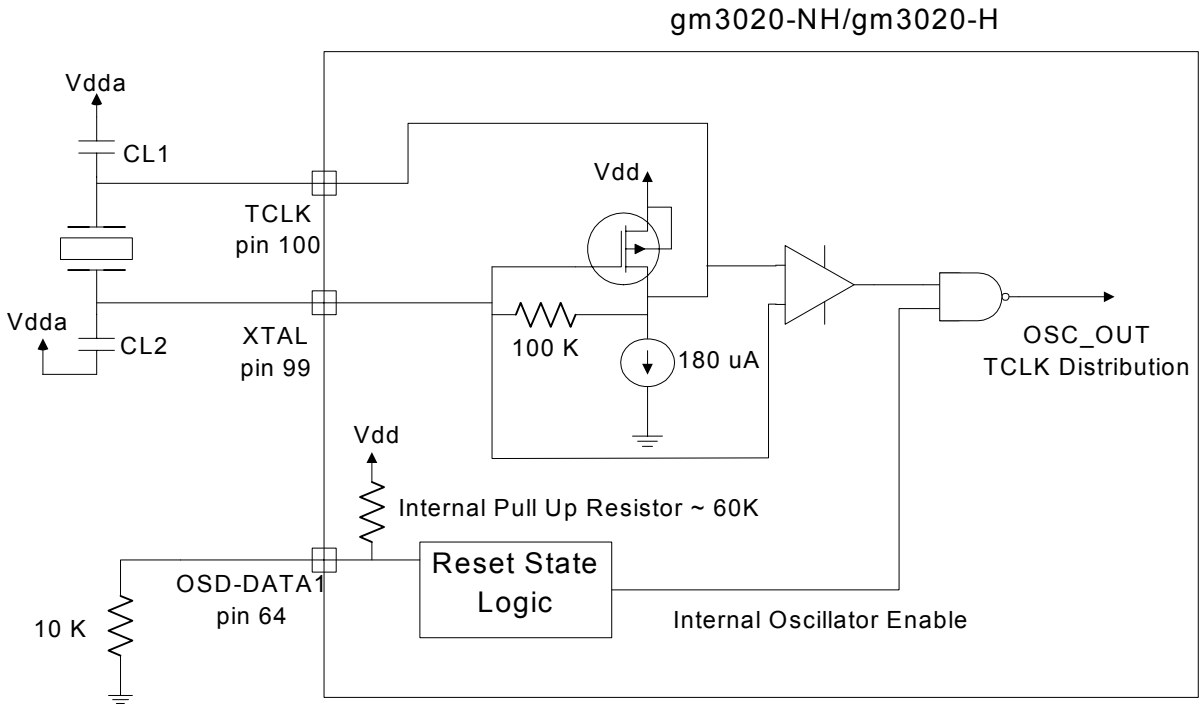


Figure 15: Using an Internal Oscillator

The oscillator circuit is a Pierce Oscillator circuit and a simplified schematic is shown in Figure 7. The output of the oscillator circuit, measured at the TCLK (pin 100), is an approximate sine wave with a bias of about 2 volts above ground (see Figure 8).

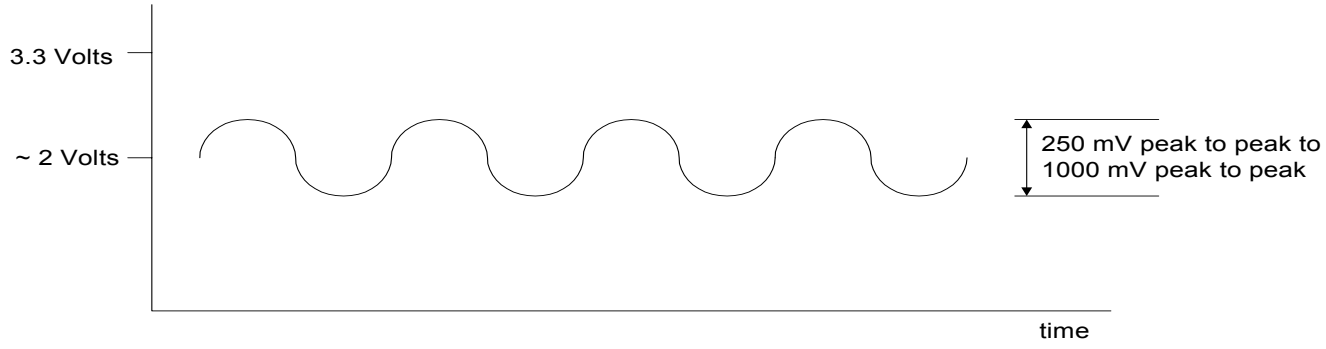


Figure 16: Internal Oscillator output at TCLK

The peak to peak voltage of the output can range from 250 mV to 1000 mV depending on the specific characteristics of the external crystal used and variation in the oscillator characteristics. The output of the oscillator is connected to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50-mV peak to peak to function correctly. The output of the comparator is buffered and then distributed to the gm3020-NH/gm3020-H circuits.

One of the design parameters that must be given some consideration is the value of the loading capacitors used with the crystal.

The loading capacitance (C_{load}) on the external crystal is the combination of C_{L1} and C_{L2} and is calculated by: $C_{load} = ((C_{L1} * C_{L2}) / (C_{L1} + C_{L2})) + C_{shunt}$.

The shunt capacitance C_{shunt} is the effective capacitance between the XTAL and TCLK pins. For the gm3020-NH/gm3020-H this is approximately 9 pF.

C_{L1} and C_{L2} are a parallel combination of the external loading capacitors (C_{ex}), the PCB board capacitance (C_{PCB}), the pin capacitance (C_{pin}), the pad capacitance (C_{pad}), and the ESD protection capacitance (C_{ESD}). The capacitances are symmetrical so that $C_{L1} = C_{L2} = C_{ex} + C_{PCB} + C_{pin} + C_{pad} + C_{ESD}$ The correct value of C_{ex} must be calculated given the value of the parasitics.

(These values need to be verified)

C_{PCB} ~ Layout dependent. Approximately 2 pF to 10 pF

C_{pin} ~ 1.1 pF

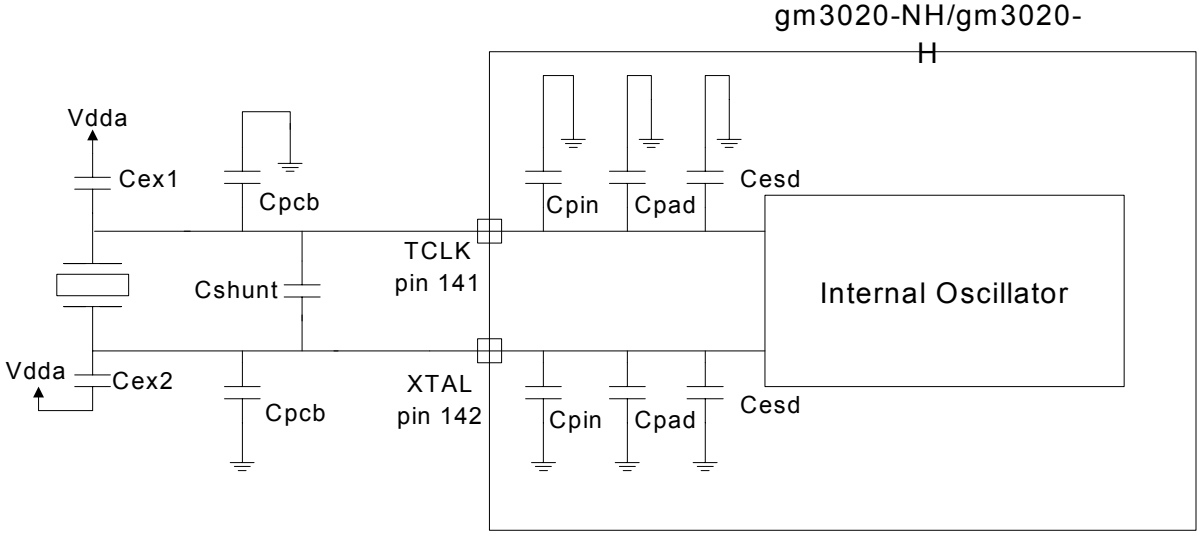
C_{pad} ~ 1 pF

C_{ESD} ~ 5.3 pF

C_{shunt} ~ 9 pF

Some attention must be given to the details of the oscillator circuit when used with an external crystal resonator. The value of C_{load} that is specified by the manufacture should not be exceeded because of potential start up problems with the oscillator. Additionally, the external crystal used should be a parallel resonate cut and the value of the equivalent series resistance must be less then 90 Ohms.

Figure 17: Parasitic Capacitance Sources



CL1 = Cex1 + Cpcb + Cpin + Cpad + Cesd

CL2 = Cex1 + Cpcb + Cpin + Cpad + Cesd

5.10 Power Down Mode

Each functional block of the gm3020-NH/gm3020-H may be independently disabled for power savings, as described in the following table:

Table 20: Disabling Functional Blocks

Functional Block	Disabled:
Ultra-Reliable DVI™ Receiver Block	By setting Index 0x52[1:0] = 01 (The RXC channel block will remain on)
DCLK DDS	By setting Index 0x21[0] = 0
DCLK PLL	By setting Index 0x4D[3] = 0
RCLK PLL	By setting Index 0x4A[2] = 0 Disable after DCLK is disabled
Gamma Table	By setting Index 0x0[6] = 0
Expansion Engine	By setting Index 0x0[0] = 0
Panel Dithering Engine	By setting Index 0x0[8] = 0
Internal OSD	By setting Index 0xB0[0] = 0
External OSD Interface	By setting Index 0xC8[0] = 0
Panel Interface	By setting Index 0x80[0] = 0
Input Capture Block	When SCLK is disabled.
Host Interface	When TCLK is stopped.
Source Timing Measurement	When TCLK is stopped.
Interrupt Request Controller	When TCLK is stopped.

6. ELECTRICAL CHARACTERISTICS

Table 21: Absolute Ratings

Parameter	Minimum	Typical	Maximum	Note
VDD			5. 6 V	(4)
V_{IN}	V_{ss} – 0.5 V		V_{cc} + 0.5 V	(1)
Operating temperature	0 degree C		70 degree C	
Power consumption at XGA output resolutions (measured at VDD=3.3V)	0 Watts		1.75 Watts	
Receiver Differential Mode Signal on any pair	- 3. 3 volts		3 .3 volts	
Receiver Termination Supply Voltage	VDD		VDD	
Receiver Termination Resistance	0 Ohm		Open Circuit	

Table 22: Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Note
VDD	3.15 V	3. 3 V	3. 47 V	(4)
V_{IL} (CMOS inputs)			0. 3 * CVDD	
V_{IH} (CMOS inputs)	0. 7 * CVDD		1 . 1 * CVDD	(1)
V_{OH}	2. 4 V		CVDD	
V_{OL}		0. 2 V	0. 4 V	
Input current	-10 uA		10 uA	

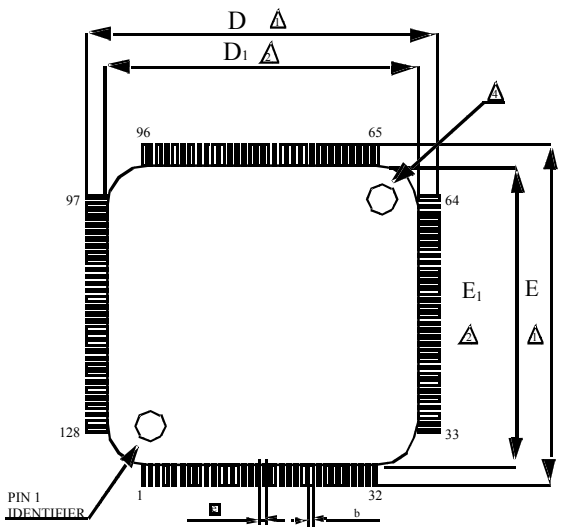
NOTE 1: All input pads except for the Ultra-Reliable DVI™ receiver input pads are 5V-tolerant inputs (except where noted in the pin descriptions).

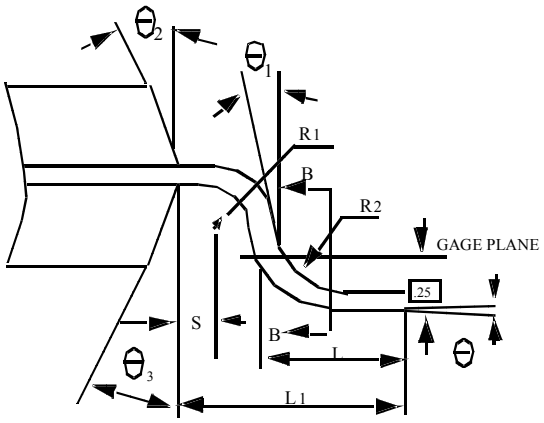
NOTE 2: When the panel interface, external OSD interface, and MFB pins are disabled, the RVDD supply current is 0 mA. The drive current of each panel interface pad can be programmed in the range of 2 mA to 20 mA (@ capacitive loading of 10 pF).

NOTE 3: When all circuits are powered down and TCLK is stopped, CVDD supply current becomes 0 mA.

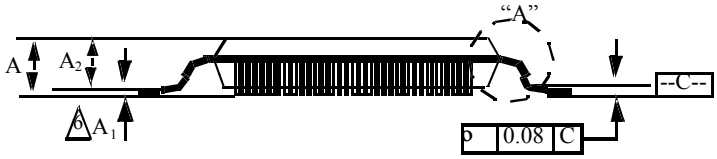
NOTE 4: Includes all VDD pins, analog and digital.

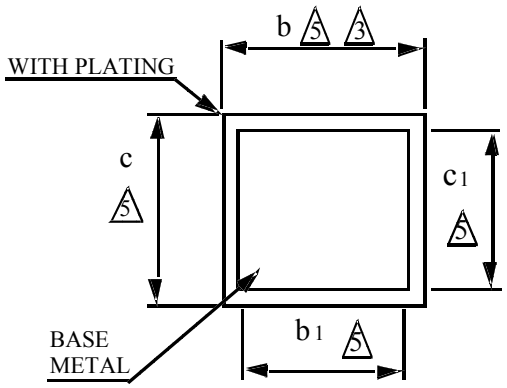
7. MECHANICAL SPECIFICATIONS





DETAIL "A"





SECTION B-B

Symbol	Dimension in mm					
	Min	Nom	Max			
A			1.60			
A_1	0.05					
A_2	1.35	1.40	1.45			
b	0.13	0.18	0.23			
b_1	0.13	0.16	0.19			
c	0.09		0.20			
c_1	0.09		0.16			
D	15.85	16.00	16.15			
D_1	13.90	14.00	14.10			
E	15.85	16.00	16.15			
E_1	13.90	14.00	14.10			
e	0.40 BSC					
L	0.45	0.60	0.75			
L_1	1.00 REF					
R_1	0.08					
R_2	0.08		0.20			
S	0.20					
θ	0°	3.5°	7°			
θ_1	0°					
θ_2	12° TYP					
θ_3	12° TYP					

128 Pin LQFP Package

8. ORDERING INFORMATION

Order Code	Application	Package	Temperature Rating
gm3020-NH	XGA with no external OSD support	128-pin LQFP 14 x 14 (mm)	Commercial 0^0 C to 70^0 C
gm3020-H	XGA with HDCP support & external OSD support	128-pin LQFP 14 x 14 (mm)	Commercial 0^0 C to 70^0 C