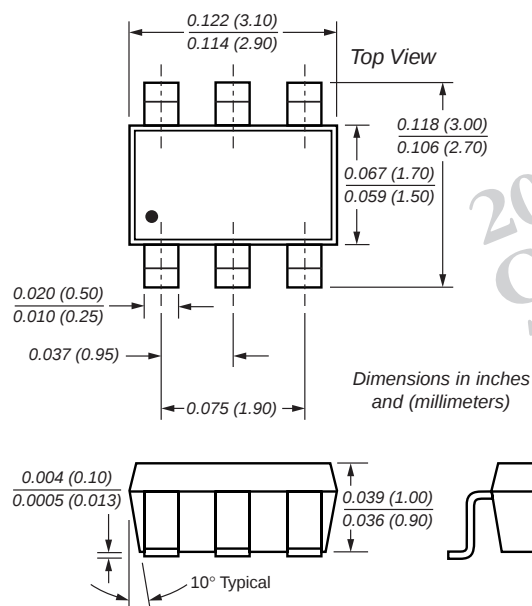


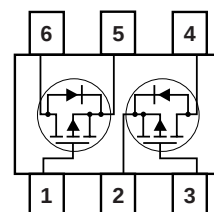


Dual P-Channel Logic Level Enhancement-Mode MOSFET

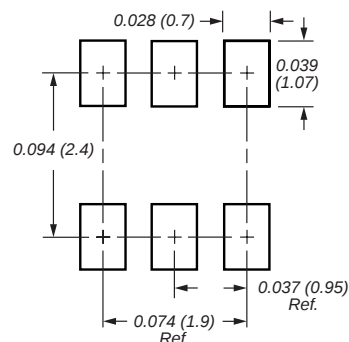
SOT-23-6L

 $V_{DS} - 20V$
 $R_{DS(ON)} 0.135\Omega$
 $I_D - 2.3A$ 

Pin Configuration (Top View)



Mounting Pad Layout



Mechanical Data

Case: SOT-23-6L package**Terminals:** Leads solderable per MIL-STD-750, Method 2026**Marking Code:** M3

Features

- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Popular SOT-23-6L package with copper lead-frame for superior thermal and electrical capabilities
- Compact and low profile
- -1.8V rated

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ⁽²⁾ $T_J = 150^\circ C$	I_D	-2.3	A
$T_A = 25^\circ C$ $T_A = 70^\circ C$		-1.8	
Pulsed Drain Current ⁽¹⁾	I_{DM}	-8	
Maximum Power Dissipation ⁽²⁾	P_D	1.15	W
$T_A = 25^\circ C$ $T_A = 70^\circ C$		0.73	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$
Junction-to-Ambient Thermal Resistance ⁽²⁾	$R_{\theta JA}$	110	$^\circ C/W$

Note: (1) Pulse width limited by maximum junction temperature.(2) Surface mounted on a 1in² 2oz. Cu PCB (FR-4 material)

Electrical Characteristics (T_J = 25°C unless otherwise noted)

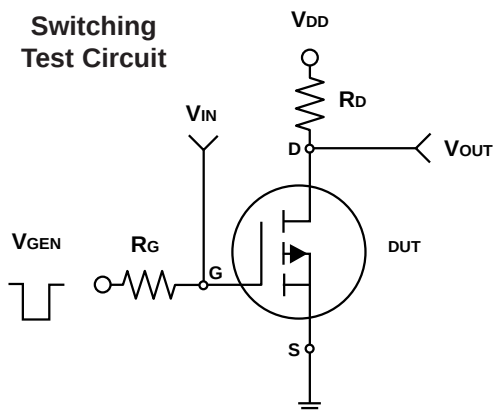
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = −250μA	−20	−	−	V
Breakdown Voltage Temp. Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =−1mA	−	−8.8	−	mV/°C
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = −250μA	−0.45	−	−	V
Gate-Body Leakage	I _{GSS}	V _{GS} = ±8V, V _{DS} = ±0V	−	−	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = −16V, V _{GS} = 0V	−	−	−1	μA
		V _{DS} =−16V, V _{GS} =0V, T _J =85°C	−	−	−10	
On-State Drain Current ⁽¹⁾	I _{D(on)}	V _{DS} ≥ −5V, V _{GS} = −4.5V	−5	−	−	A
Drain-Source On-State Resistance ⁽¹⁾	R _{DS(on)}	V _{GS} = −4.5V, I _D = −2.3A	−	109	135	mΩ
		V _{GS} = −2.5V, I _D = −2.0A	−	146	180	
		V _{GS} = −1.8V, I _D = −1.7A	−	205	250	
Forward Transconductance ⁽¹⁾	g _{fs}	V _{DS} = −5V, I _D = −2.3A	−	5	−	S
Dynamic						
Total Gate Charge ⁽¹⁾	Q _g	V _{DS} = −10V, V _{GS} = −4.5V I _D = −2.3A	−	5.1	7.5	nC
Gate-Source Charge ⁽¹⁾	Q _{gs}		−	1.0	−	
Gate-Drain Charge ⁽¹⁾	Q _{gd}		−	1.2	−	
Turn-On Delay Time ⁽¹⁾	t _{d(on)}	V _{DD} = −8V, R _L = 8Ω I _D ≅ −1A, V _{GEN} = −4.5V R _G = 6Ω	−	7	20	ns
Turn-OnRise Time ⁽¹⁾	t _r		−	45	60	
Turn-Off Delay Time ⁽¹⁾	t _{d(off)}		−	162	200	
Turn-OffFall Time ⁽¹⁾	t _f		−	116	160	
Input Capacitance	C _{iss}	V _{DS} = −10V, V _{GS} = 0V f = 1.0MHz	−	343	−	pF
Output Capacitance	C _{oss}		−	77	−	
Reverse Transfer Capacitance	C _{rss}		−	58	−	
Source-Drain Diode						
Maximum Diode Forward Current	I _S	T _A = 25°C	−	−	−1.3	A
Maximum Pulsed Diode Forward Current ⁽²⁾	I _{SM}	—	−	−	−8	A
Diode Forward Voltage ⁽¹⁾	V _{SD}	V _{GS} = 0V, I _S = −1.05A	−	−0.85	−1.1	V

Notes:

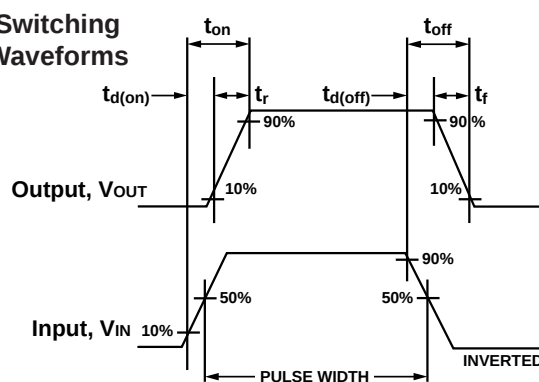
(1) Pulse test; pulse width ≤ 300μs, duty cycle ≤ 2%

(2) Pulse width limited by maximum junction temperature

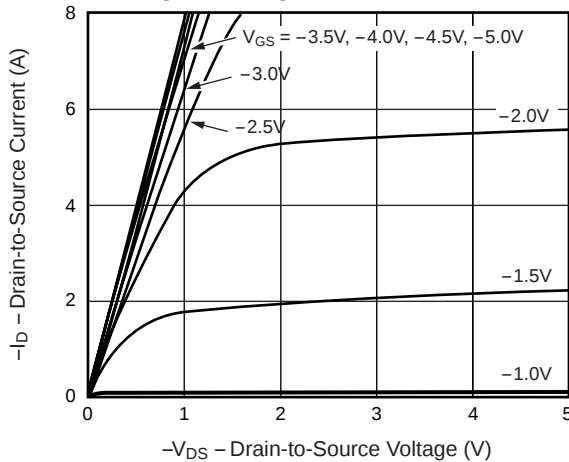
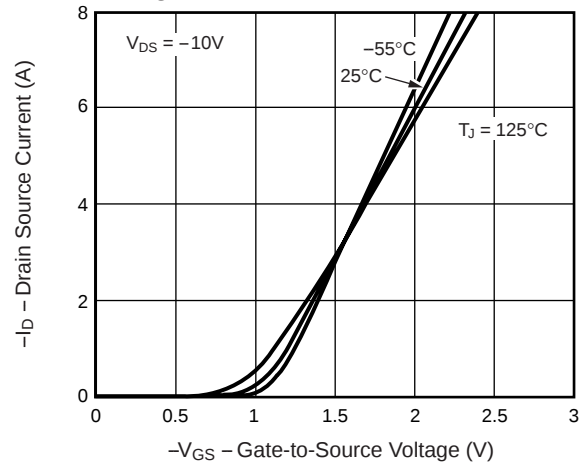
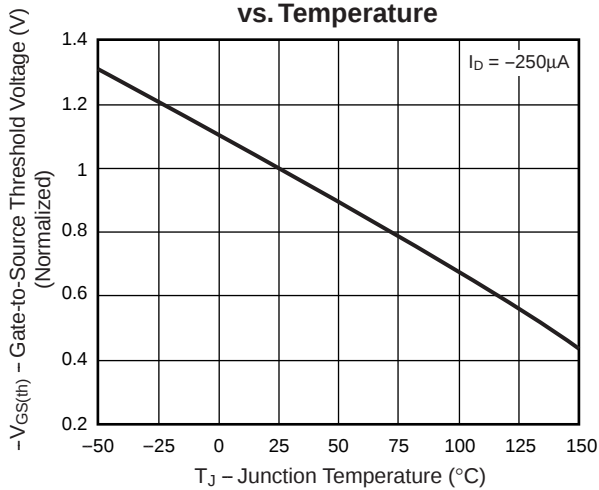
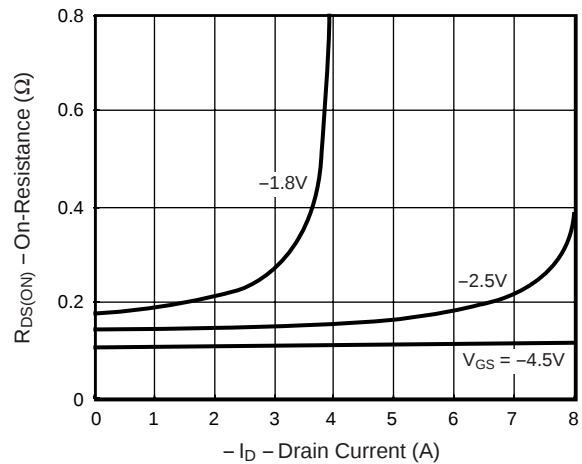
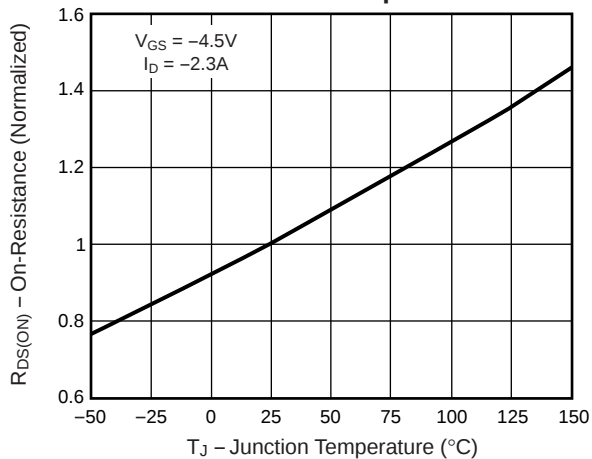
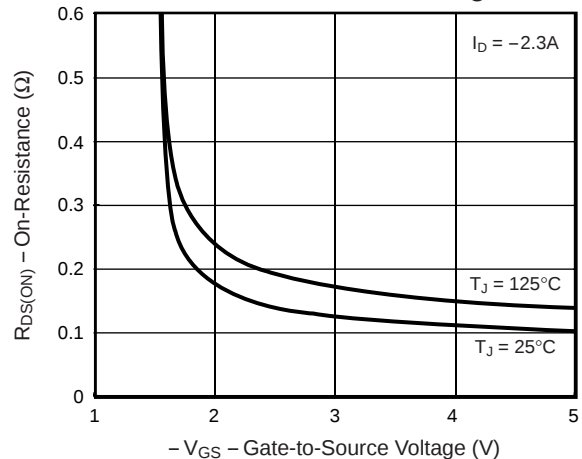
Switching Test Circuit



Switching Waveforms



Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 1 – Output Characteristics

Fig. 2 – Transfer Characteristics

Fig. 3 – Threshold Voltage vs. Temperature

Fig. 4 – On-Resistance vs. Drain Current

Fig. 5 – On-Resistance vs. Junction Temperature

Fig. 6 – On-Resistance vs. Gate-to-Source Voltage


Ratings and Characteristic Curves

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 7 – Gate Charge

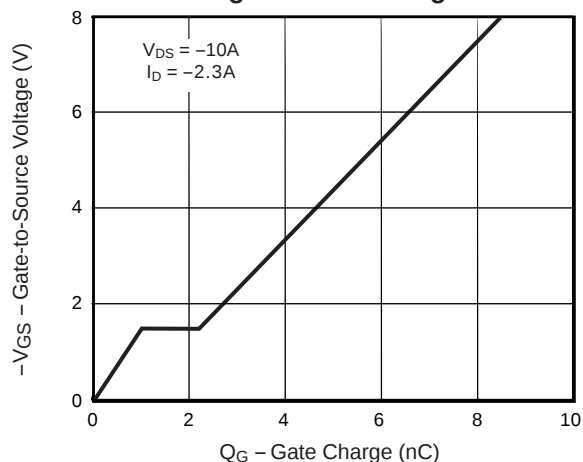


Fig. 8 – Capacitance

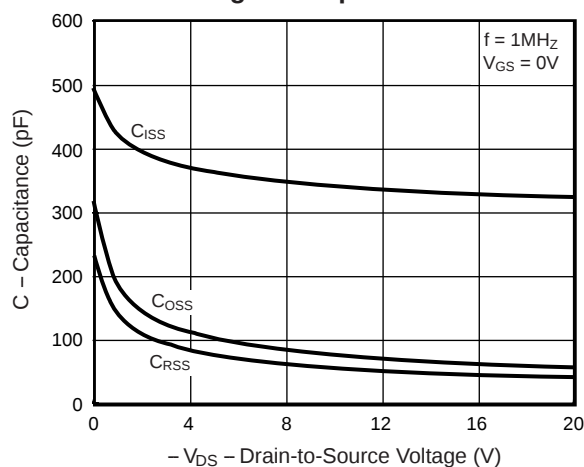


Fig. 9 – Source-Drain Diode
Forward Voltage

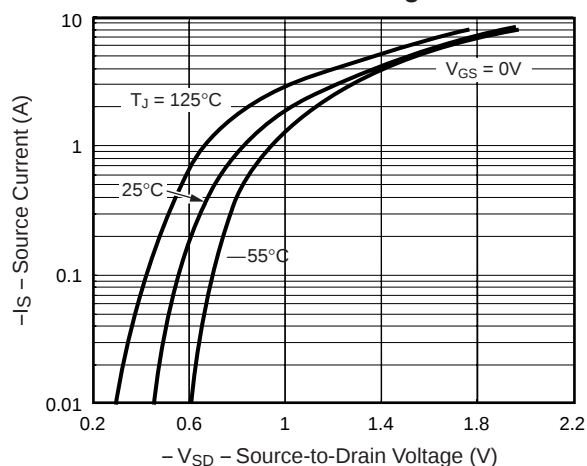


Fig. 10 – Thermal Impedance

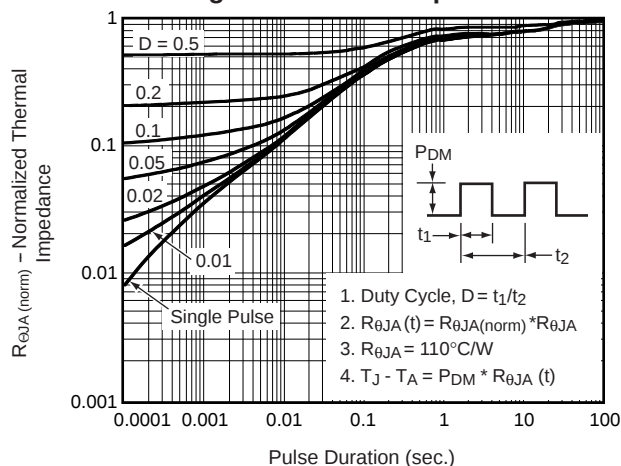


Fig. 11 – Power vs. Pulse Duration

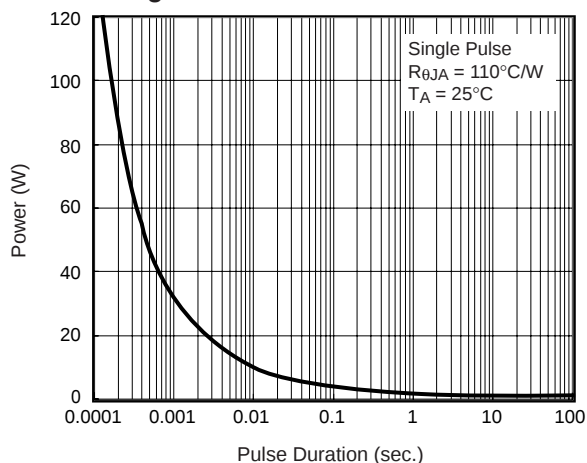


Fig. 12 – Maximum Safe Operating Area

