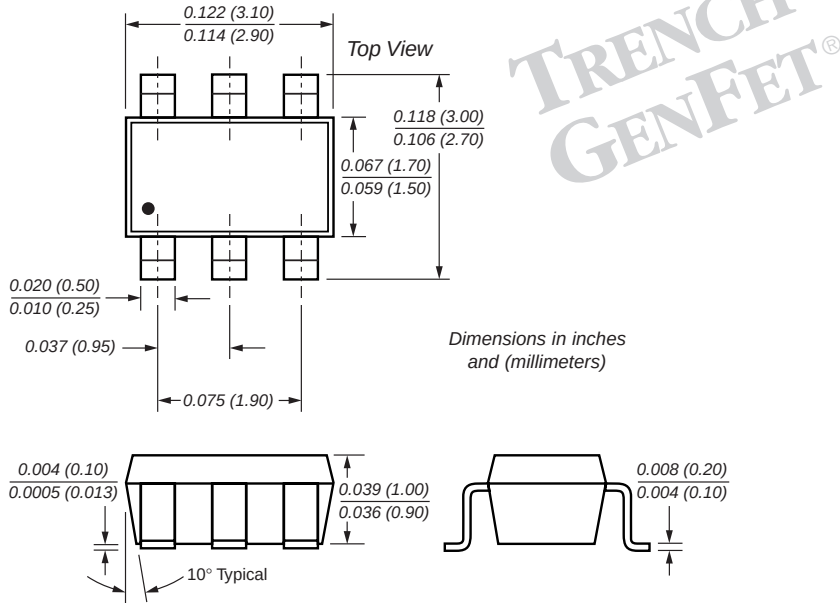




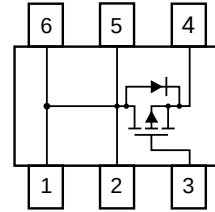
P-Channel Enhancement-Mode MOSFET

 $V_{DS} - 30V$
 $R_{DS(ON)} 75m\Omega$
 $I_D - 3.6A$

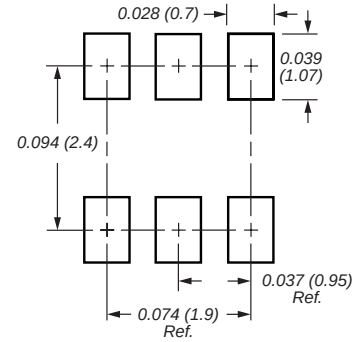
SOT-23-6L



Pin Configuration (Top View)



Mounting Pad Layout



Mechanical Data

Case: SOT-23-6L package**Terminals:** Leads solderable per MIL-STD-750,
Method 2026**Marking Code:** 54

Features

- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Popular SOT-23-6L package with copper lead-frame for superior thermal and electrical capabilities
- Compact and low profile

Maximum Ratings and Thermal Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

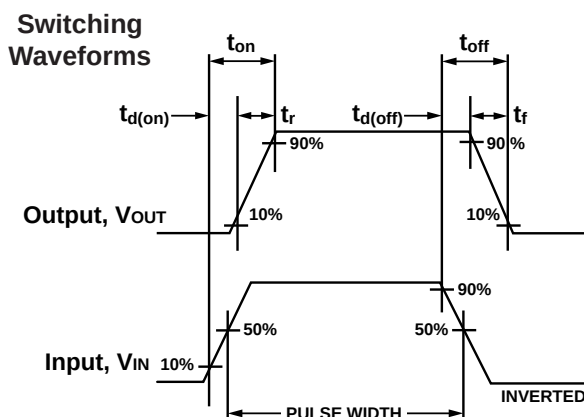
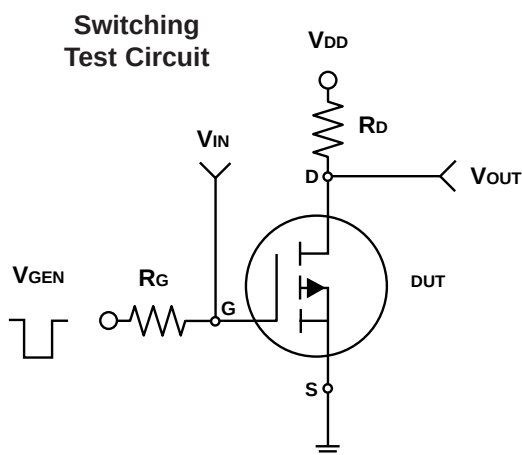
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ⁽²⁾ $T_J = 150^\circ C$	I_D	-3.6	A
$T_A = 25^\circ C$ $T_A = 70^\circ C$		-2.9	
Pulsed Drain Current ⁽¹⁾	I_{DM}	-10	
Power Dissipation ⁽²⁾ $T_J = 150^\circ C$	P_D	2.0	W
$T_A = 25^\circ C$ $T_A = 70^\circ C$		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$
Junction-to-Ambient Thermal Resistance ⁽²⁾	$R_{\theta JA}$	62.5	$^\circ C/W$

Notes: (1) Pulse width limited by maximum junction temperature(2) Surface mounted on FR4 board, $t \leq 5$ sec.

Electrical Characteristics (T_J = 25°C unless otherwise noted)

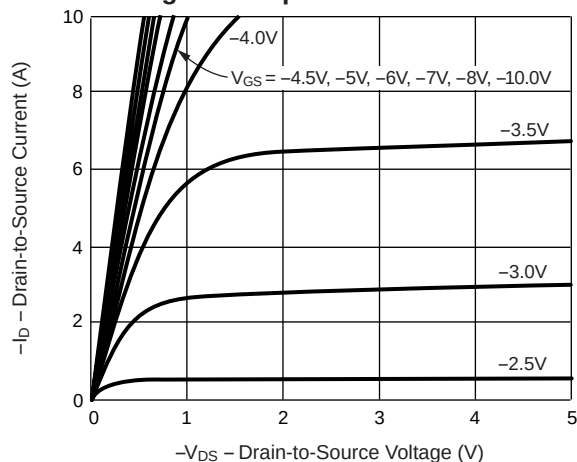
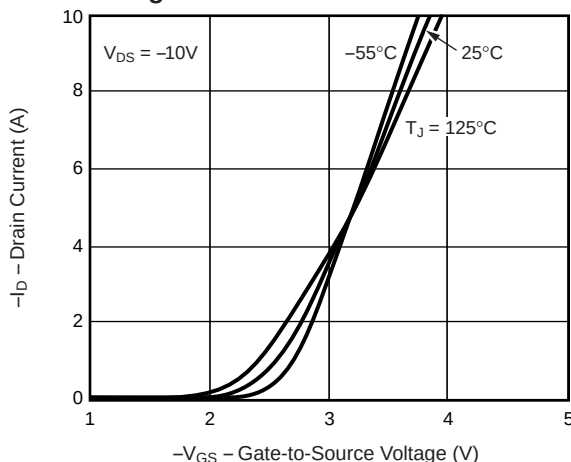
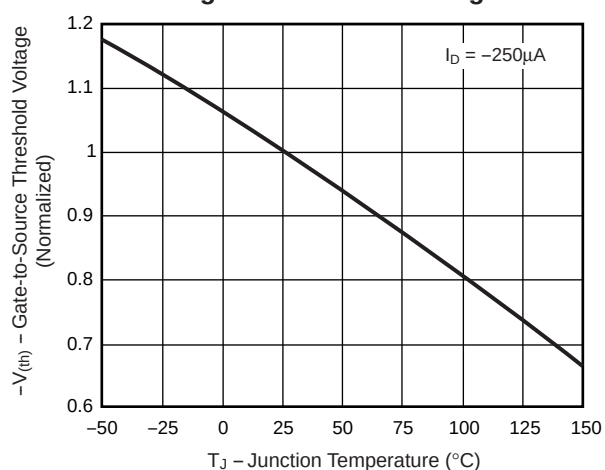
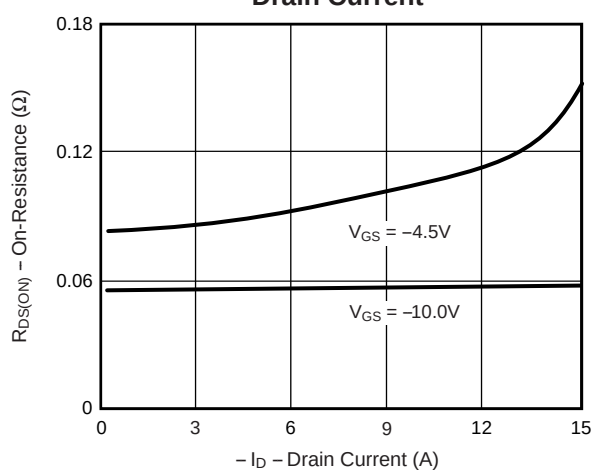
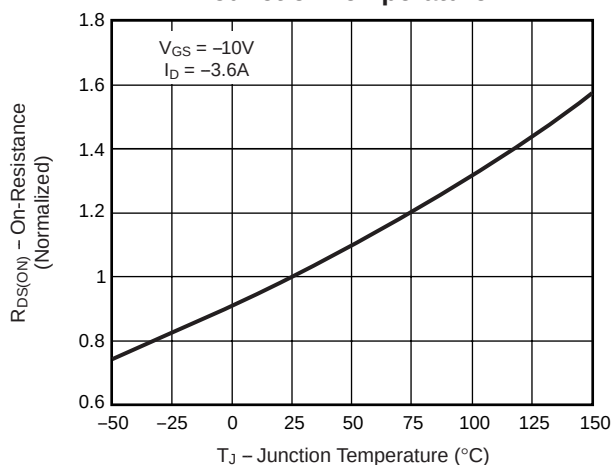
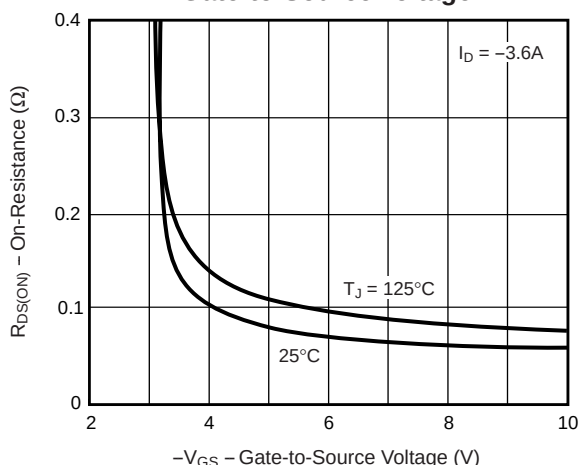
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = −250μA	−30	−	−	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = −250μA	−1	−	−3	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	−	−	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = −24V, V _{GS} = 0V	−	−	−1.0	μA
		V _{DS} =−20V, V _{GS} =0V, T _J =55°C	−	−	−10.0	
On-State Drain Current ⁽¹⁾	I _{D(on)}	V _{DS} = −5V, V _{GS} = −4.5V	−5	−	−	A
Drain-Source On-State Resistance ⁽¹⁾	R _{DS(on)}	V _{GS} = −10V, I _D = −3.6A	−	55	75	mΩ
		T _J = 125°C	−	75	127	
		V _{GS} = −4.5V, I _D = −2.7A	−	86	125	
Forward Transconductance ⁽¹⁾	g _{fs}	V _{DS} = −10V, I _D = −3.6A	−	3	−	S
Dynamic						
Total Gate Charge ⁽¹⁾	Q _g	V _{DS} = −15V, V _{GS} = −10V I _D = −3.6A	−	12.5	15	nC
Gate-Source Charge ⁽¹⁾	Q _{gs}		−	2.0	−	
Gate-Drain Charge ⁽¹⁾	Q _{gd}		−	2.5	−	
Turn-On Delay Time ⁽¹⁾	t _{d(on)}	V _{DD} = −15V I _D ≈ −1A, V _{GEN} = −10V R _G = 6Ω	−	5	18	ns
Rise Time ⁽¹⁾	t _r		−	5.5	14	
Turn-Off Delay Time ⁽¹⁾	t _{d(off)}		−	40	60	
Fall Time ⁽¹⁾	t _f		−	19	29	
Input Capacitance	C _{iss}	V _{DS} = −15V, V _{GS} = 0V f = 1.0MHz	−	670	−	pF
Output Capacitance	C _{oss}		−	125	−	
Reverse Transfer Capacitance	C _{rss}		−	70	−	
Source-Drain Diode						
Maximum Diode Forward Current	I _S	T _A = 25°C	−	−	−1.3	A
Maximum Pulsed Diode Forward Current ⁽²⁾	I _{SM}		−	−	−10	
Diode Forward Voltage ⁽¹⁾	V _{SD}	I _S = −1.3A, V _{GS} = 0V	−	−0.85	−1.2	V
		T _J = 125°C	−	−0.64	−1	

Note: (1) Pulse test, pulse width ≤ 300 μs, duty cycle ≤ 2%
(2) Pulse width limited by maximum junction temperature



Ratings and Characteristic Curves

($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 1 – Output Characteristics

Fig. 2 – Transfer Characteristics

Fig. 3 – Threshold Voltage

Fig. 4 – On-Resistance vs. Drain Current

Fig. 5 – On-Resistance vs. Junction Temperature

Fig. 6 – On-Resistance vs. Gate-to-Source Voltage


Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 7 – Gate Charge

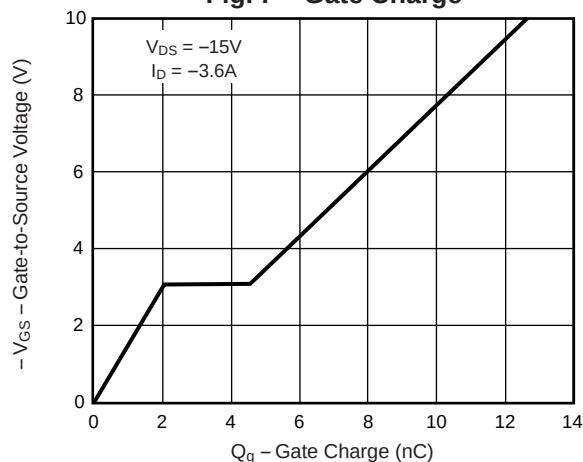


Fig. 8 – Capacitance

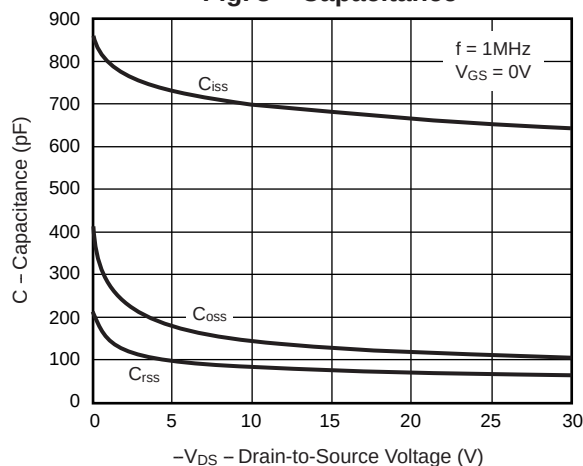


Fig. 9 – Source-Drain Diode Forward Voltage

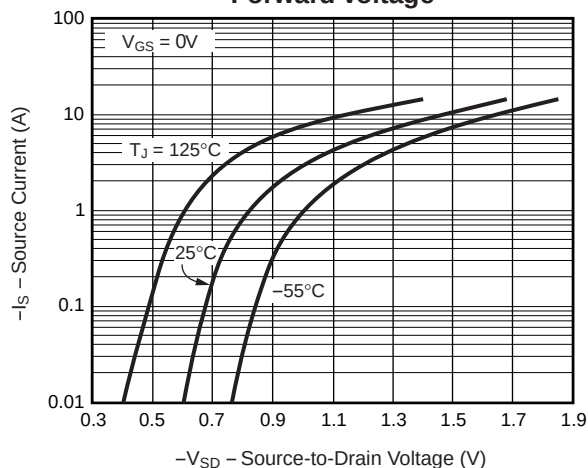


Fig. 10 – Transient Thermal Impedance

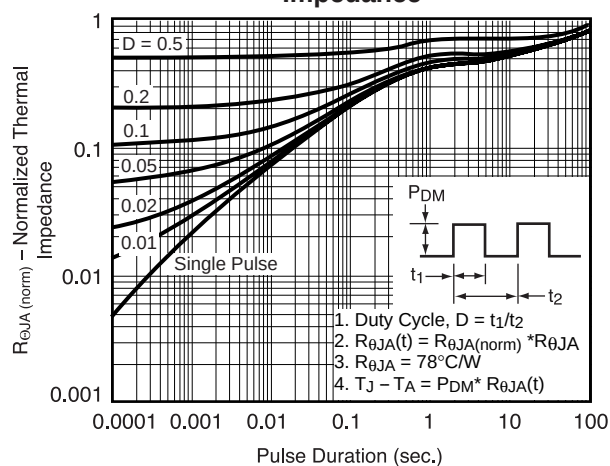


Fig. 11 – Power vs. Pulse Duration

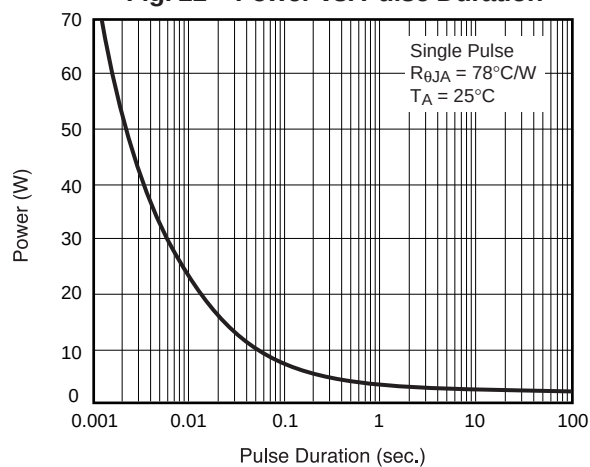


Fig. 12 – Maximum Safe Operating Area

