GLT4160M04

4M X 4 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT

Nov. 2001 (Rev. 2.1)

Features :

- 4,194,304 words by 4 bits organization.
- Fast access time and cycle time
- Low power dissipation.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh.
- 2,048 refresh cycles per 32ms.
- Available in 300 mil 26(24) SOJ and TSOPII.
- 2.5V±0.2V Vcc Power Supply voltage.
- All inputs and Outputs are LVTTL compatible.
- Extended Data-Out (EDO) Page access cycle.
- Self-refresh Capability. (S-Version).

Description :

The GLT4160M04 is a high-performance CMOS dynamic random access memory containing 16,777,216 bits organized in a x4 configuration. The GLT4160M04 offers page cycle access with Extended Data Output. The GLT4160M04 has 11 row- and 11 column-addresses, and accepts 2048-cycle refresh in 32 ms.

The GLT4160M04 provides EDO PAGE MODE operation which allows for fast data access within a row-address defined boundary, up to 2048 x 4 bits with cycle times as short as 25ns.

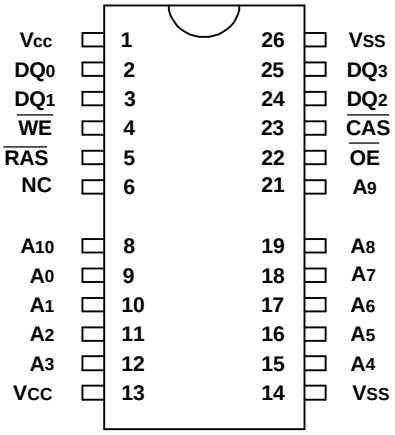
HIGH PERFORMANCE	60	70	80
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns	40 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	25 ns	30 ns	35 ns
Min. Read/Write Cycle Time, (t_{RC})	104 ns	124 ns	144 ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	15 ns	20 ns	20 ns

G-Link Technology
2701 Northwestern Parkway
Santa Clara, CA 95051, U.S.A.

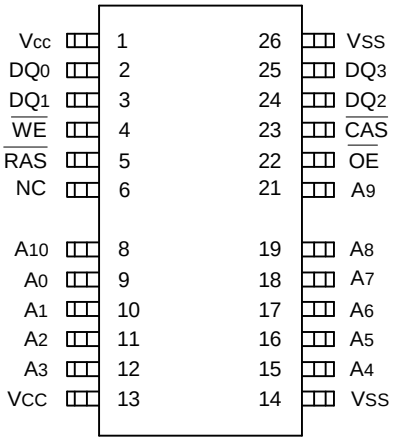
G-Link Technology Corporation,Taiwan
6F, No. 24-2, Industry E. RD. IV, Science Based
Industrial Park, Hsin Chu, Taiwan.

Pin Configuration :

GLT4160M04
300mil 26(24) SOJ



GLT4160M04
300mil 26(24) TSOPII



Pin Descriptions:

Name	Function
A_0 - A_{10}	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
DQ_0 - DQ_3	Data Inputs / Outputs
V_{CC}	+2.5V Power Supply
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
.....0°C to +70°C
For Extended Temperature……..-20°C to 85°C
Storage Temperature(plastic).....-55°C to +150°C
Voltage Relative to V_{SS}.....-0.5V to + 4.6V
Short Circuit Output Current.....20mA
Power Dissipation.....1.0W

*Note: Operation above Absolute Maximum Ratings can aversely affect device reliability.

Capacitance*

T_A=25°C, V_{CC}=2.5V±0.2V, V_{SS}=0V

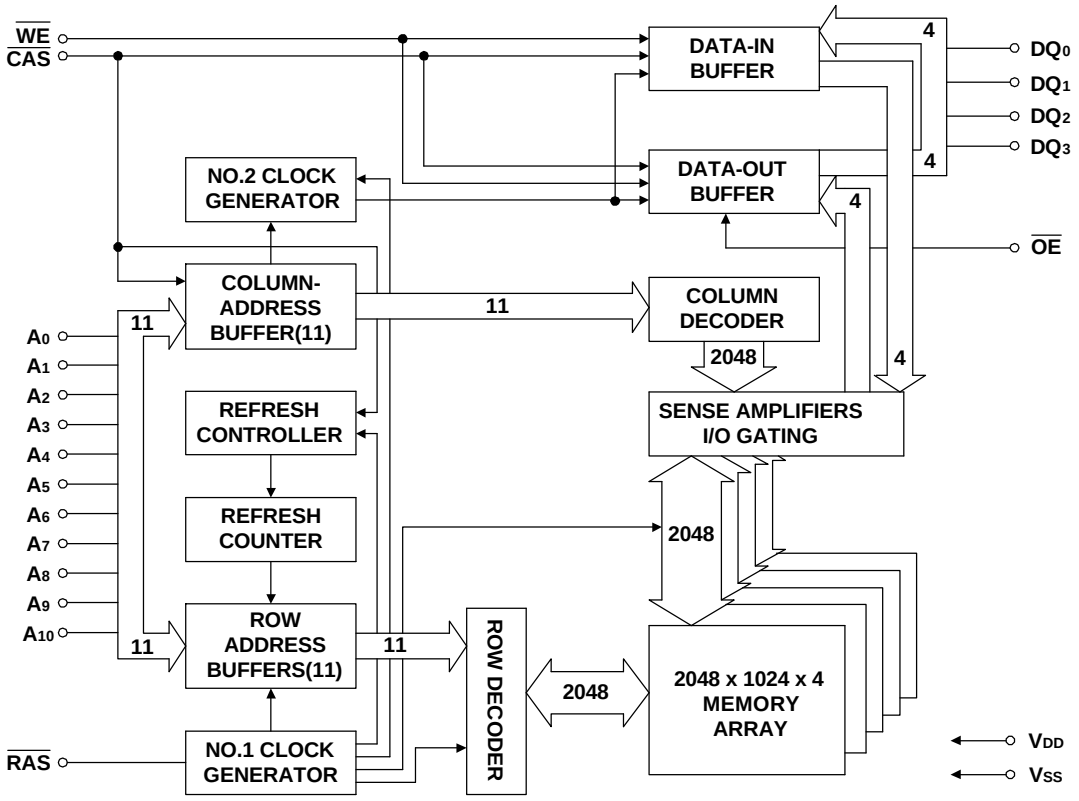
Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	7	pF
C_{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 200µs and then, execute eight $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Truth Table:

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESS		DATA-IN/OUT
						t_R	t_C	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out,Data-In
EDO-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
READ	2nd cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
EARLY-WRITE	2nd cycle	L	H→L	L	X	n/a	COL	Data-In
EDO-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out,Data-In
READ-WRITE	2nd cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out,Data-In
$\overline{RAS}$ -ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, -20°C to 85°C V_{CC}=2.5V±0.2V, V_{SS}=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	0V ≤ V_{IN} ≤ V_{CC}+0.3V (All other pins not under test=0V)		-5		+5	µA	
I_{LO}	Output Leakage Current (for High-Z State)	0V ≤ V_{out} ≤ V_{CC} Output is disabled (Hiz)		-5		+5	µA	
I_{CC1}	Operating Current, Random READ/WRITE	t_{RC} = t_{RC} (min.)	t_{RAC} = 60ns t_{RAC} = 70ns t_{RAC} = 80ns			80 70 60	mA	1,2
I_{CC2}	Standby Current, (TTL)	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥V_{SS}				1	mA	
I_{CC3}	Refresh Current, $\overline{RAS}$ -Only	$\overline{RAS}$ cycling, $\overline{CAS}$ at V_{IH} t_{RC} = t_{RC} (min.)	t_{RAC} = 60ns t_{RAC} = 70ns t_{RAC} = 80ns			80 70 60	mA	2
I_{CC4}	Operating Current, EDO Page Mode	$\overline{RAS}$ at V_{IL}, $\overline{CAS}$ address cycling:t_{PC}=t_{PC}(min.)	t_{RAC} = 60ns t_{RAC} = 70ns t_{RAC} = 80ns			80 70 60	mA	1,2
I_{CC5}	Refresh Current, $\overline{CAS}$ Before $\overline{RAS}$	$\overline{RAS}$, $\overline{CAS}$ address cycling: t_{RC}=t_{RC} (min.)	t_{RAC} = 60ns t_{RAC} = 70ns t_{RAC} = 80ns			80 70 60	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{RAS}$ ≥V_{CC}-0.2V, $\overline{CAS}$ ≥V_{CC}-0.2V, All other inputs V_{SS}				200	µA	1
I_{CC7}	Self refresh Current	$\overline{RAS}$ = $\overline{CAS}$ =0.2V, $\overline{WE}$ = $\overline{OE}$ = A_0~A_{10}=V_{CC}-0.2V or 0.2V DQ_0~DQ_3=V_{CC}-0.2V,0.2V or Open				200	µA	
V_{IL}	Input Low Voltage			-0.3		+0.8	V	3
V_{IH}	Input High Voltage			2.0		V_{CC}+0.3	V	4
V_{OL}	Output Low Voltage	I_{OL} = 2mA				0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -2mA		1.8			V	

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC}(max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions specified ICC(max.) is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
3. Specified V_{IL}(min.) is steady state operation. During transitions V_{IL}(min.) may undershoot to –0.9V for a period not to exceed 10ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC}.
4. Specified V_{IH}(max.) is steady state operation . During transitions V_{IH}(max.) may overshoot to V_{CC}+0.9V for a period not to exceed 10ns. All AC parameters are measured with V_{IL}(min.) ≥ V_{SS} and VIH(max.) ≤ V_{CC} .

AC Characteristics

T_A = 0°C to 70°C , -20°C to 85°C V_{CC} = 2.5 V ± 0.2V, VIH/VIL = 2.0/0.8 V, V_{OH}/V_{OL} = 1.6/0.6V

An initial pause of 200 µs and 8 $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycles are required after power-up.

		60		70		80			
Parameter	**Symbol**	**Min.**	**Max.**	**Min .**	**Max.**	**Min.**	**Max.**	**Unit**	**Notes**
Read or Write Cycle Time	t_{RC}	104		124		144		ns	
Read Modify Write Cycle Time	t_{RWC}	140		170		190		ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10k	70	10k	80	10k	ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	1, 2, 3
Access Time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	1, 5, 10
Access Time from Column Address	t_{AA}		30		35		40	ns	1, 5, 6
$\overline{CAS}$ to Output Low-Z	t_{CLZ}	3		3		3		ns	
$\overline{CAS}$ to Output High-Z	t_{CEZ}	3	15	3	20	3	20	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	45		50		70		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10k	15	10k	20	10k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	20	60	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	15	40	ns	7
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		10		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	10		15		15		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30		35		40		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	45		50		60		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	4
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		0		ns	8, 9
Write Command Hold Time	t_{WCH}	10		15		15		ns	
Write Command Pulse Width	t_{WP}	10		15		15		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15		20		20		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	10		15		20		ns	

AC Characteristics

Parameter	Symbol	60		70		80		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-Up Time	t_{DS}	0		0		0		ns	
Data Hold Time	t_{DH}	10		15		15		ns	
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	45		50		60		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	79		94		99		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	34		44		44		ns	
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	49		59		64		ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay	t_{CPWD}	54		64		69		ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ Before $\overline{RAS}$ counter test cycle)	t_{CPT}	20		25		25		ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		35		40		45	ns	
EDO Page Mode Cycle Time	t_{PC}	25		30		35		ns	
EDO Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	56		71		81		ns	
$\overline{CAS}$ Precharge Time (EDO Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Pulse Width (EDO Page Mode Only)	t_{RASP}	60	100k	70	100k	80	100k	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ precharge	t_{RHCP}	35		40		45		ns	
Access Time from $\overline{OE}$	t_{OEA}		15		20		20	ns	8
$\overline{OE}$ to Data Delay Time	t_{OED}	15		20		20		ns	
$\overline{OE}$ to Output Low-Z	t_{OLZ}	0		0		3		ns	
$\overline{OE}$ to Output High-Z	t_{OEZ}	3	15	3	20	3	20	ns	
$\overline{WE}$ to Data Delay	t_{WED}	15		20		20		ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	15		20		20		ns	
Data Output Hold after $\overline{CAS}$ low	t_{DOH}	5		5		5		ns	
$\overline{RAS}$ to Output High-Z	t_{REZ}	3	15	3	20	3	20	ns	
$\overline{WE}$ to Output High-Z	t_{WEZ}	3	15	3	20	3	20	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	5		5		5		ns	
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5		5		5		ns	
$\overline{OE}$ Precharge Time	t_{OEP}	5		5		5		ns	
$\overline{WE}$ Puts width (EDO mixed read write cycle)	t_{WPE}	5		5		5		ns	
$\overline{CAS}$ Set-Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	t_{CSR}	5		5		5		ns	

Parameter	Symbol	60		70		80		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	t_{CHR}	10		15		15		ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ Before $\overline{RAS}$ refresh)	t_{WRP}	10		10		10		ns	
$\overline{WE}$ to $\overline{RAS}$ hold time ($\overline{CAS}$ Before $\overline{RAS}$ refresh)	t_{WRH}	10		10		10		ns	
Transition Time	t_T	2	50	2	50	2	50	ns	
Refresh Period (2,048 cycles)	t_{REF}		32		32		32	ms	
Refresh Period (S-Version)	t_{REFS}		128		128		128	ms	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ Before $\overline{RAS}$ Self refresh)	t_{RASS}	100		100		100		µs	
$\overline{RAS}$ precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Self refresh)	t_{RPS}	110		130		150		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Self refresh)	t_{CHS}	-50		-50		-50		ns	

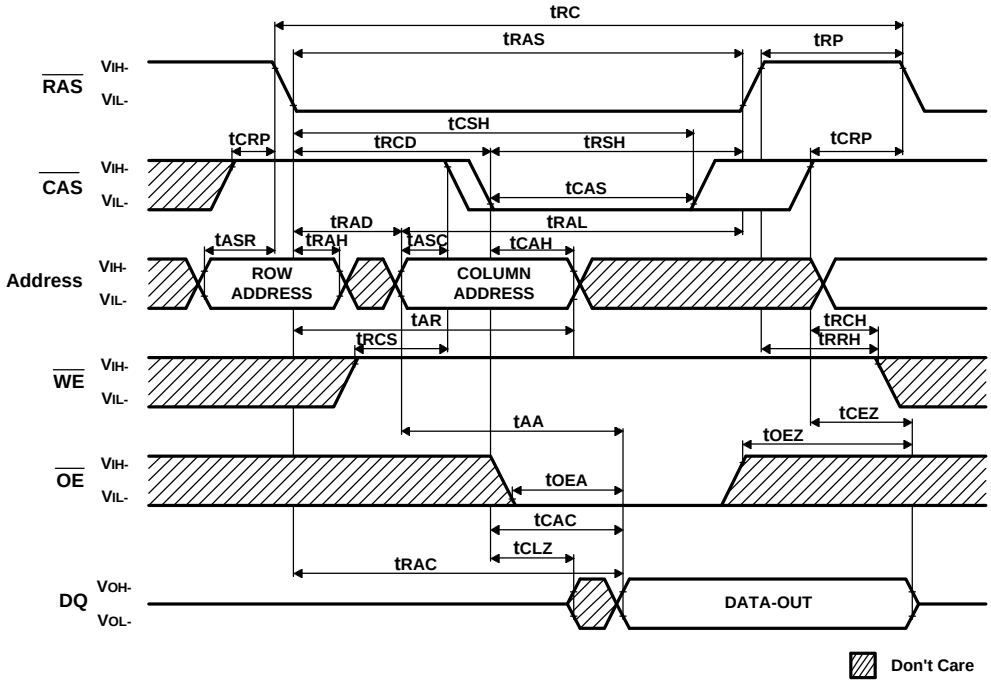
TEST MODE CYCLE

Parameter	Symbol	60		70		80		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Random read or write cycle time	t_{RC}	109		129		149		ns	
Read-modify-write cycle time	t_{RWC}	145		175		195		ns	
Access time from $\overline{RAS}$	t_{RAC}		65		75		85	ns	1,2,3,7
Access time from $\overline{CAS}$	t_{CAC}		20		25		25	ns	1,3,7
Access time from column address	t_{AA}		35		40		45	ns	1,2,7
$\overline{RAS}$ pulse width	t_{RAS}	65	10k	75	10k	85	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10k	20	10k	25	10k	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	50		55		75		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35		40		45		ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	39		49		49		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	84		99		104		ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	54		64		69		ns	8
$\overline{CAS}$ Precharge to $\overline{WE}$ delay time	t_{CPWD}	59		69		74		ns	8
EDO Page Mode cycle time	t_{PC}	30		35		40		ns	
EDO page mode read-modify-write cycle time	t_{PRWC}	61		76		86		ns	
$\overline{RAS}$ Pulse width (EDO page cycle)	t_{RASP}	65	100k	75	100k	85	100k	ns	
Access time form $\overline{CAS}$ precharge	t_{CPA}		40		45		50	ns	1
$\overline{OE}$ access time	t_{OEA}		20		25		25	ns	
$\overline{OE}$ to data delay	t_{OED}	20		25		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	20		25		25		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	

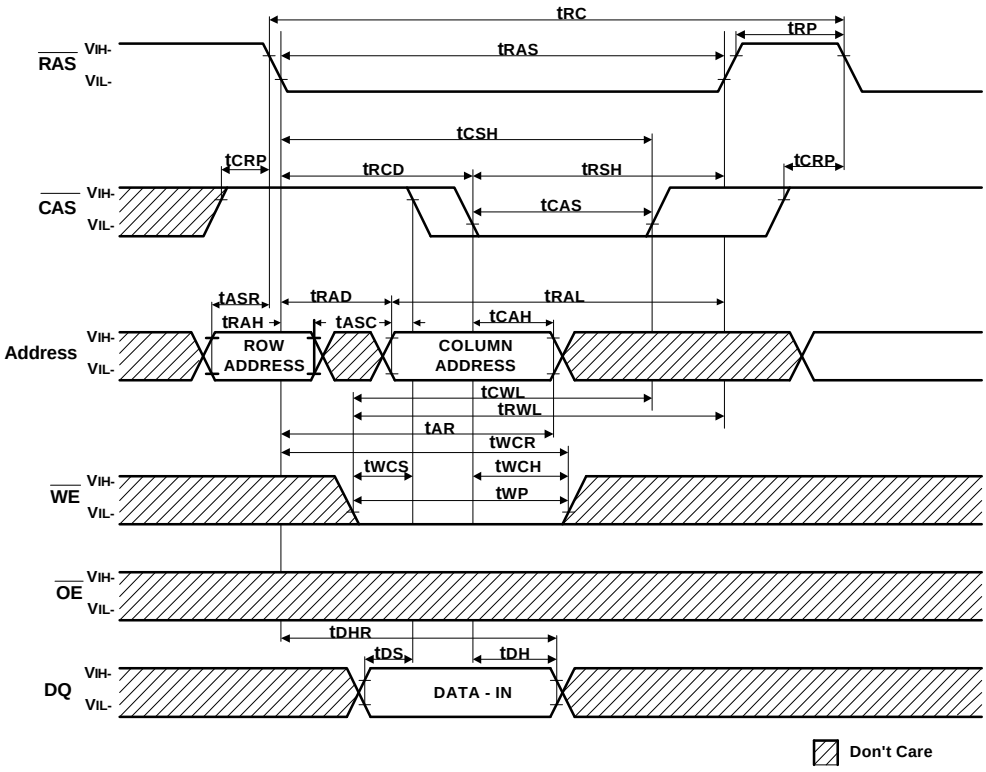
Notes:

1. Measure with a load equivalent to one TTL input and 100 pF.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), access time will be t_{AA} dominant.
3. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RCD} (max.), access time will be controlled by t_{CAC}.
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{AA}, t_{CAC} and t_{CPA}.
6. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
7. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
8. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
11. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 2 ns.

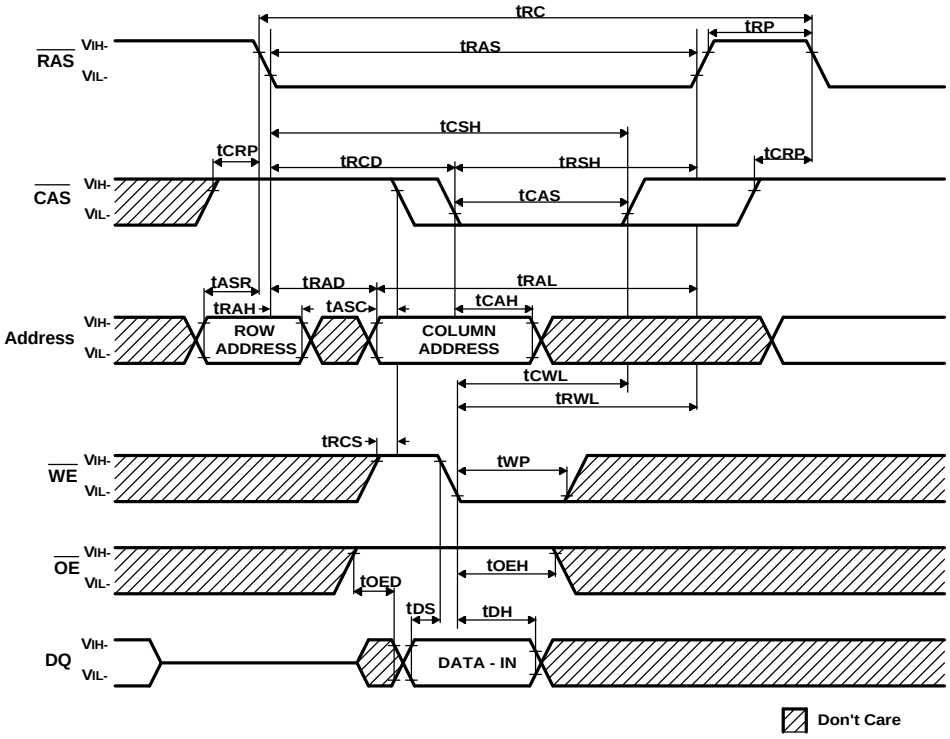
Read Cycle



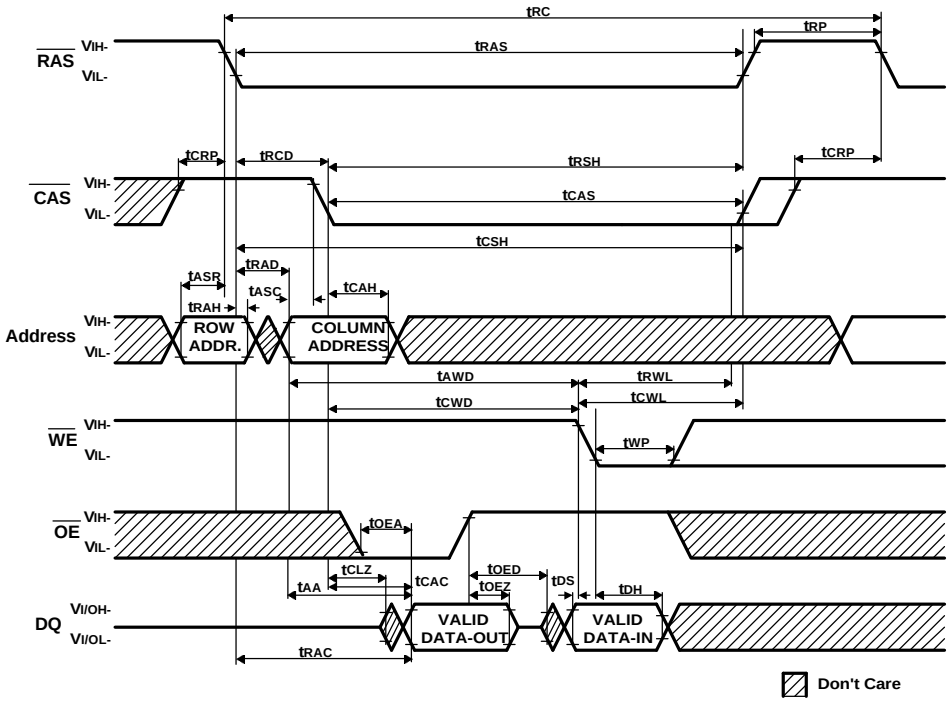
Early Write Cycle NOTE : D_{OUT} = OPEN



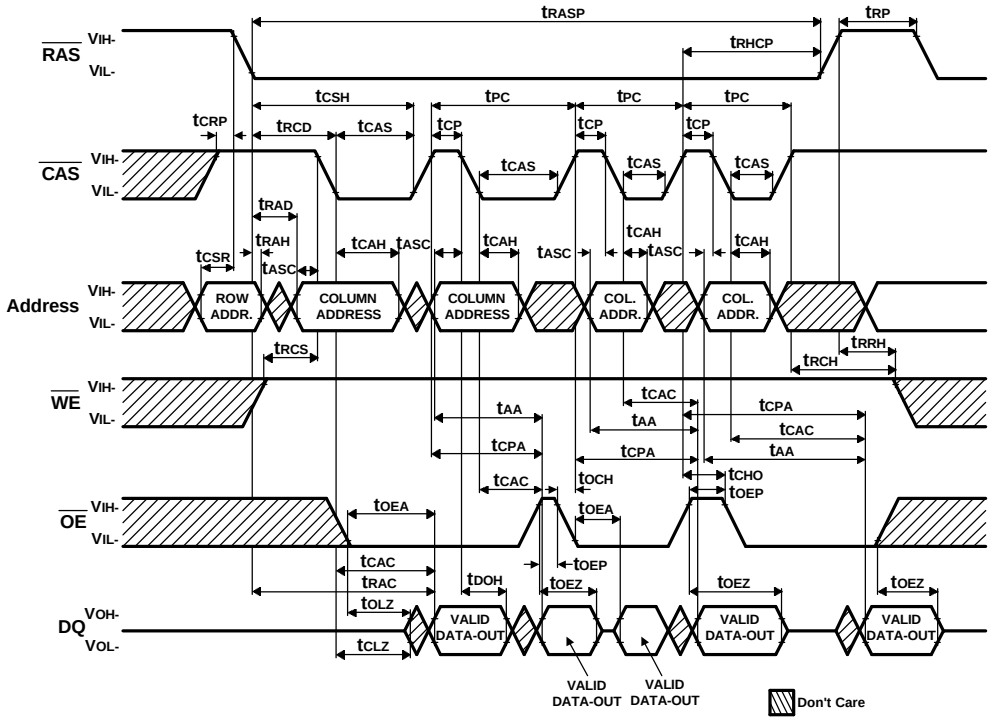
$\overline{OE}$ Controlled Write Cycle NOTE : D_{OUT} = OPEN



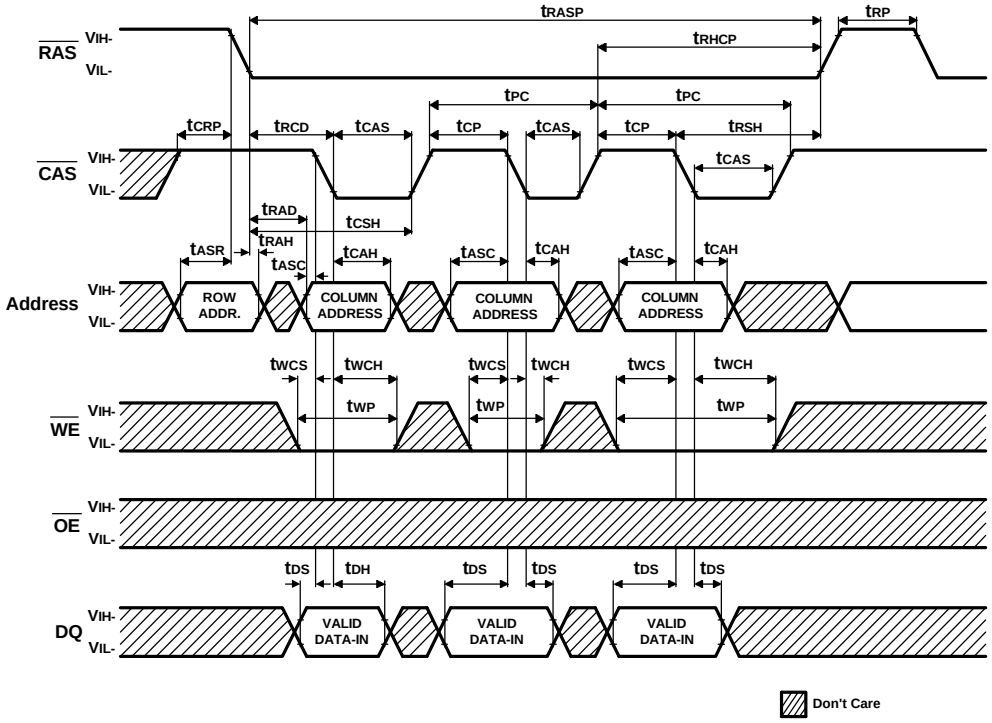
Read - Modify - Write Cycle



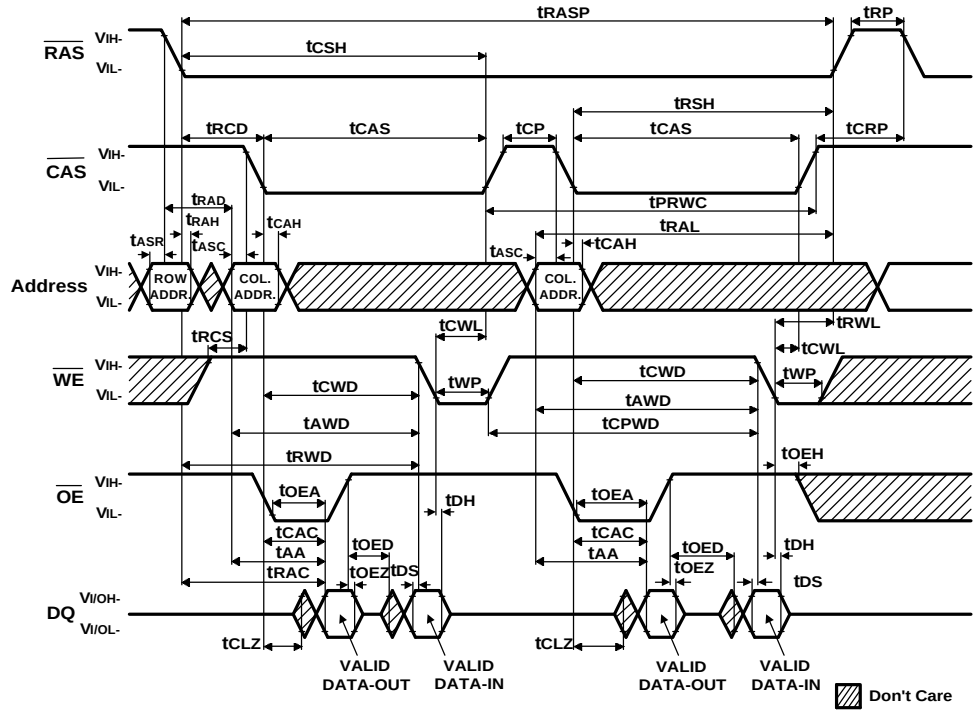
EDO Page Mode Read Cycle NOTE : D_{OUT} = OPEN



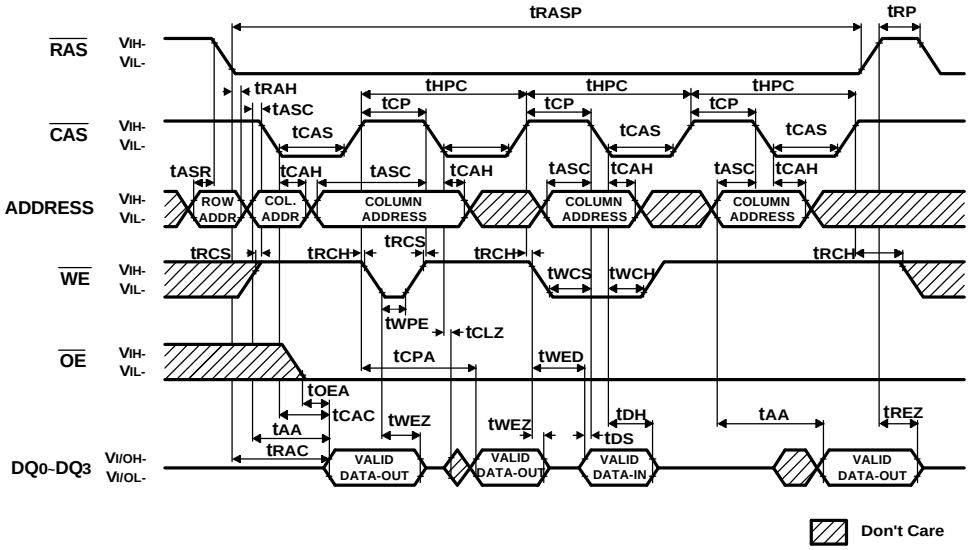
EDO Page Mode Early Write Cycle NOTE : D_{OUT} = OPEN



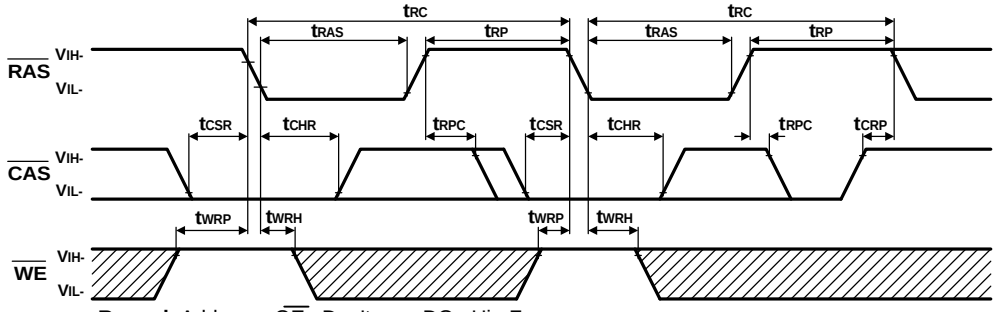
EDO Page Mode Read - Modify - Write Cycle NOTE : D_{OUT} = OPEN



EDO Page Read And Write Mixed Ccycle

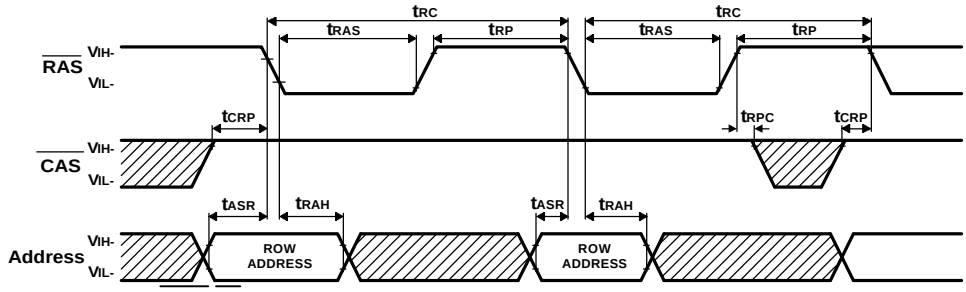


$\overline{CAS}$ - Before - $\overline{RAS}$ Refresh Cycle



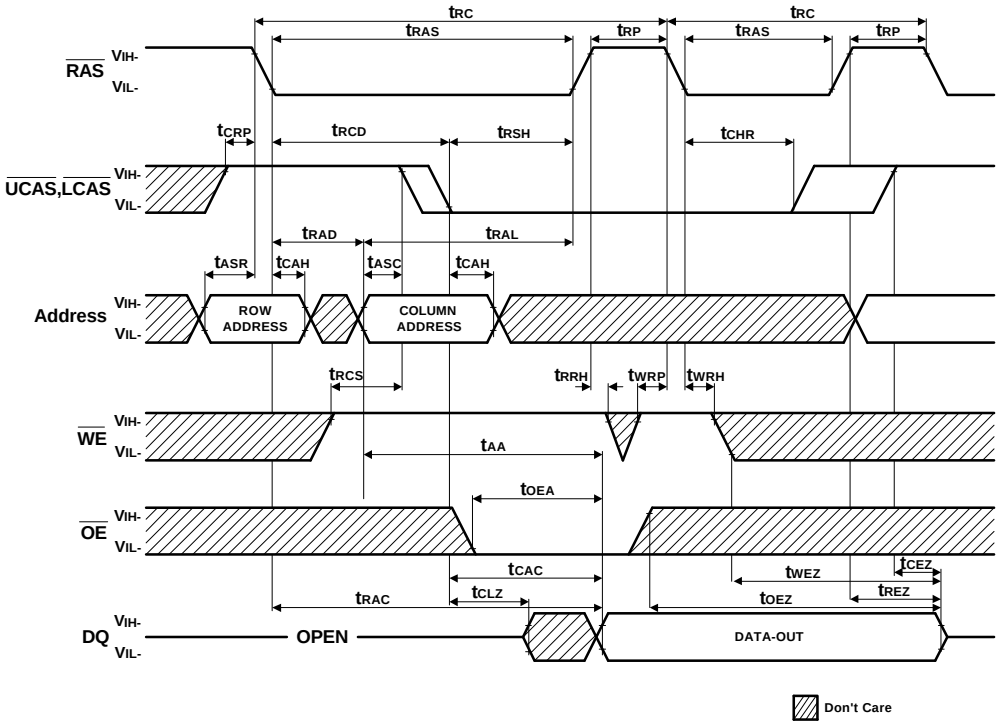
Remark Address, $\overline{OE}$: Don't care DQ : Hi - Z

$\overline{RAS}$-Only Refresh Cycle

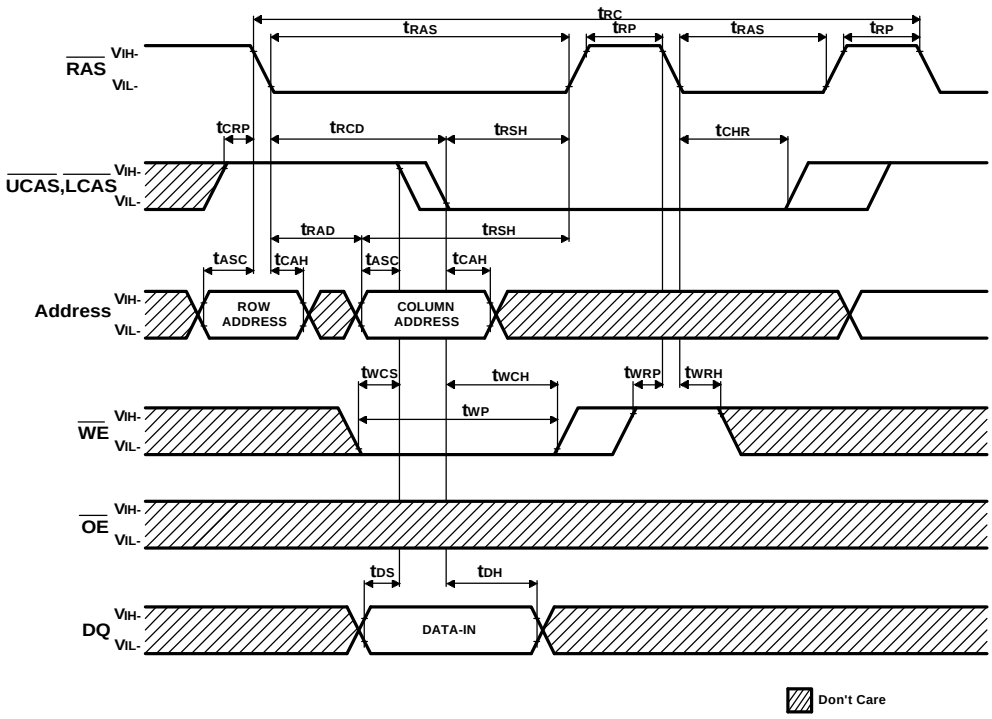


Remark $\overline{WE}$, $\overline{OE}$: Don't care DQ : Hi - Z

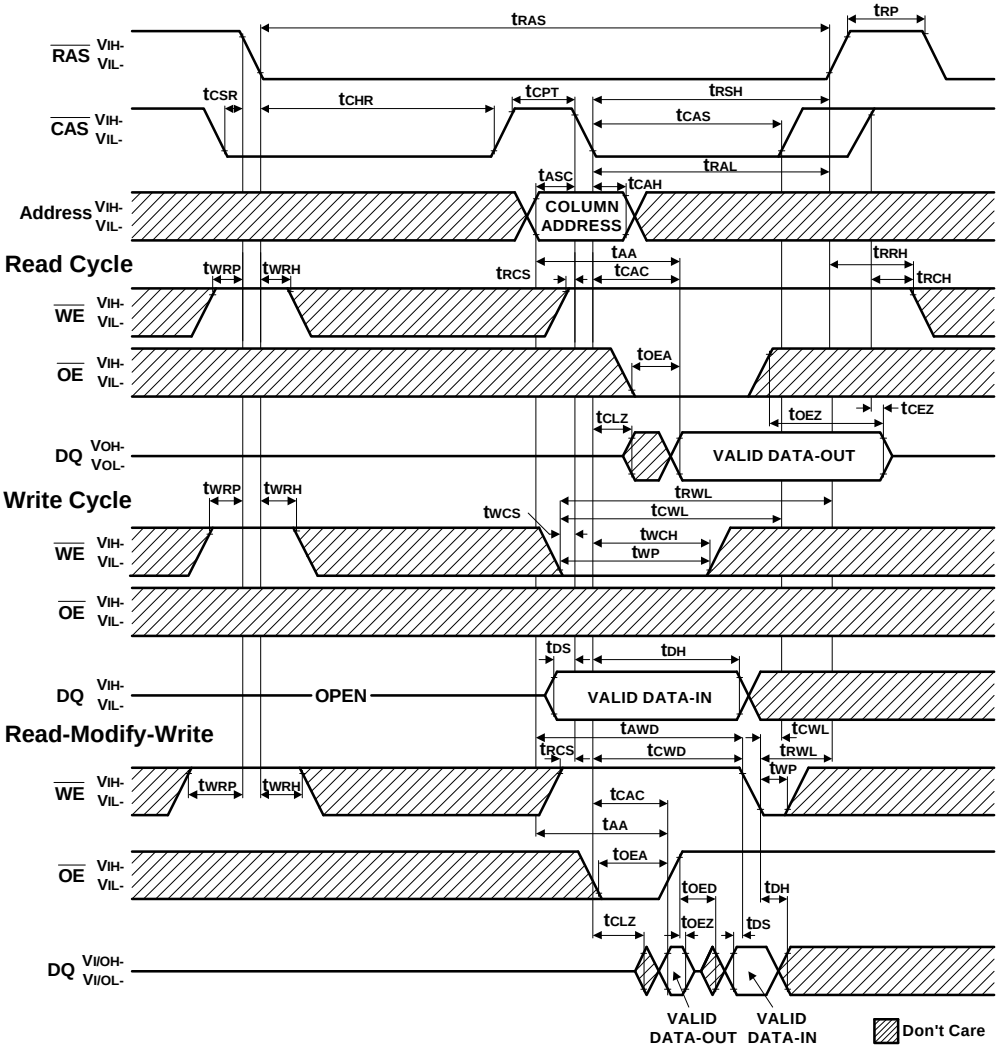
Hidden Refresh Cycle (Read)



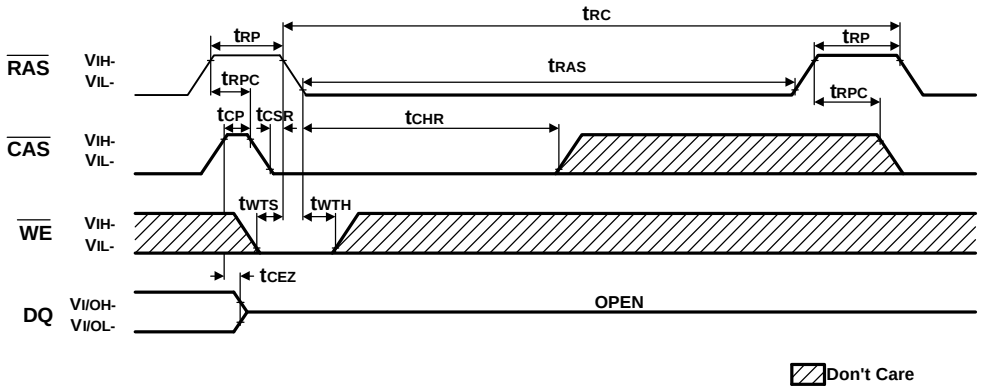
Hidden Refresh Cycle (Write) NOTE : D_{OUT} = OPEN



CAS-Before RAS Refresh Counter Test Cycle



Test Mode In Cycle



Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the x 16-bit organization during test mode. Don't care about the input levels of the $\overline{CAS}$ input A0, A1 .

(1) Setting the mode

Executing the test mode cycle ($\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) sets the test mode.

(2) Write / read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell be checked.

Output = "1" Normal write (all memory cells)
Output = "0" Abnormal write

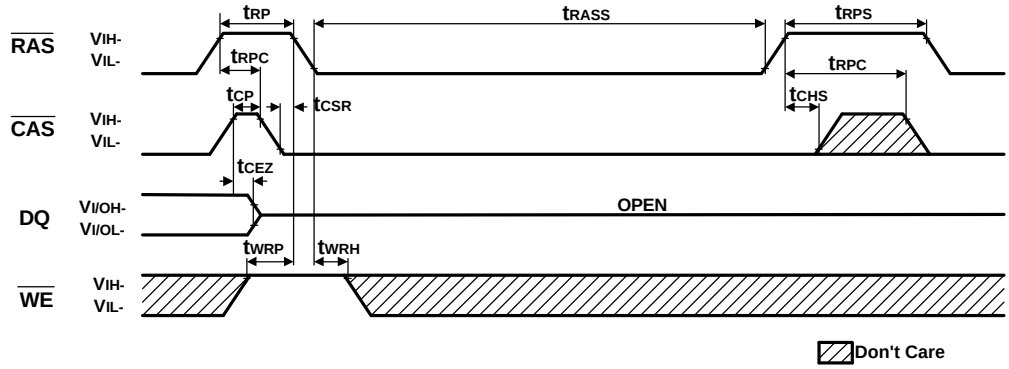
(3) Refresh

Refresh in the test mode must be performed with the $\overline{RAS}$ / $\overline{CAS}$ cycle or with the $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. The $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle use the same counter as the $\overline{CAS}$ before $\overline{RAS}$ refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

$\overline{CAS}$-Before-$\overline{RAS}$ Self Refresh Cycle

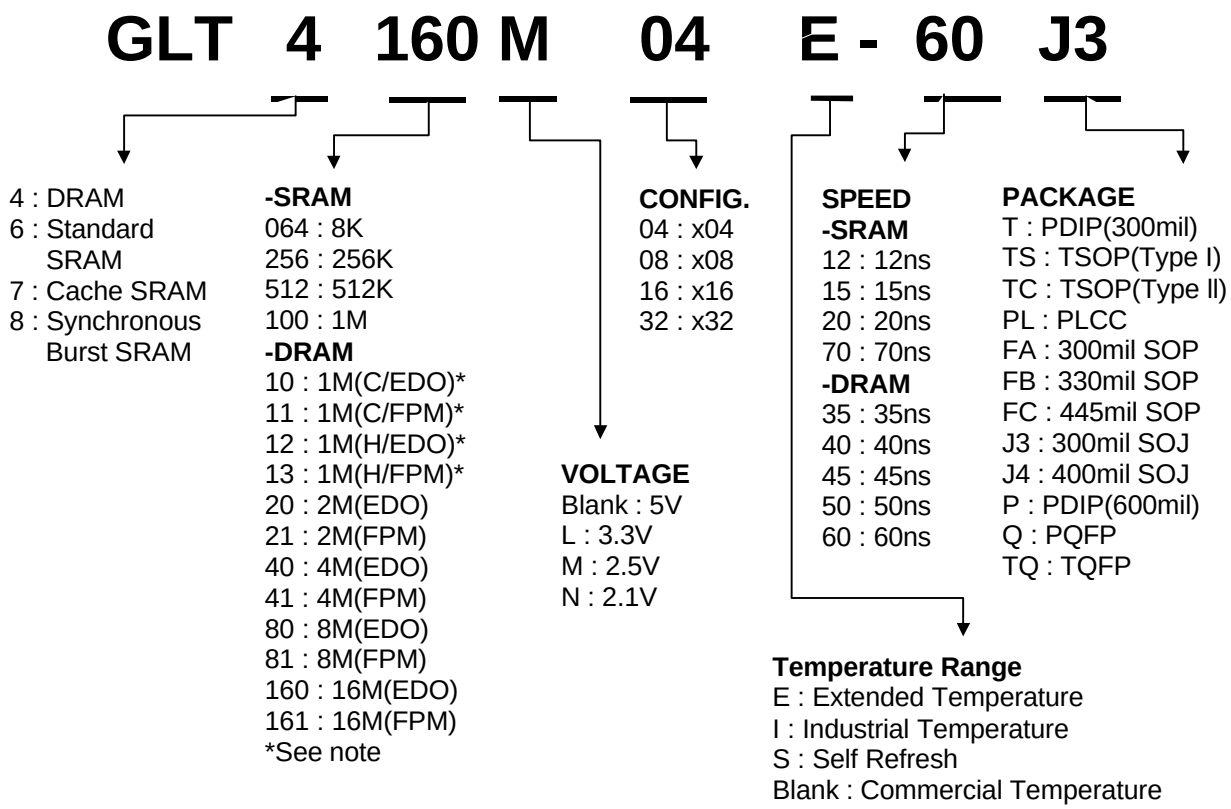


NOTE : $\overline{OE}$, Address = Don't Care

Ordering Information

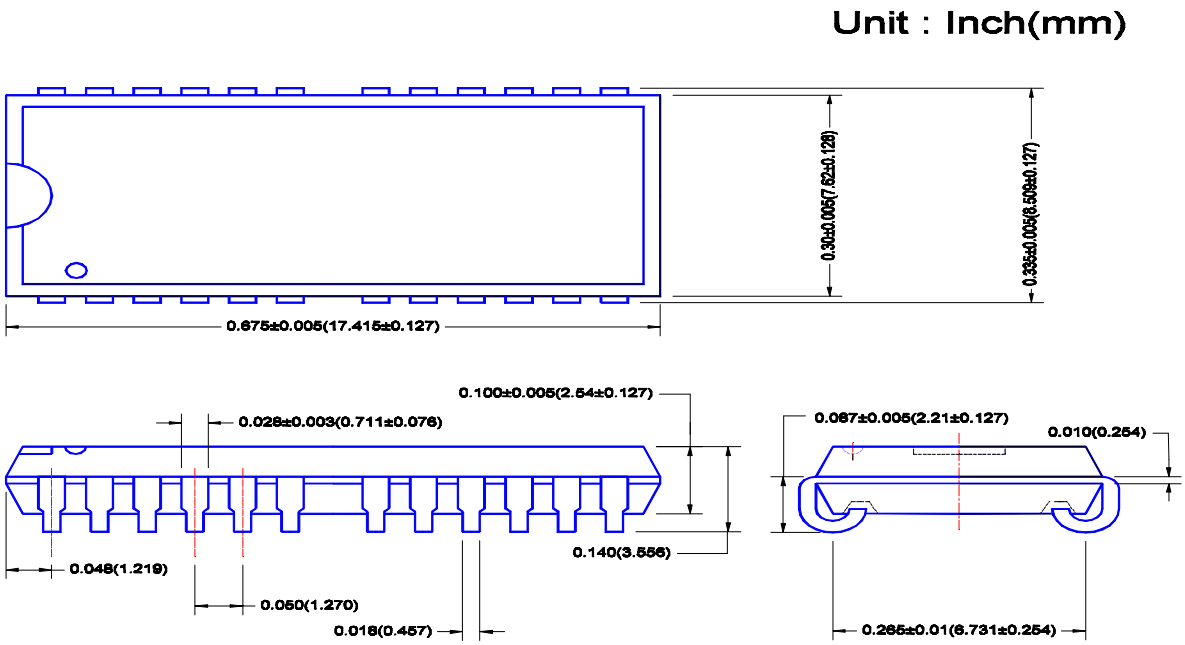
Part Number	SPEED	POWER	FEATURE	TEMPERATURE	PACKAGE
GLT4160M04-60J3	60ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160M04-70J3	70ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160M04-80J3	80ns	Normal	EDO	Commercial	SOJ 300mil 26(24)L
GLT4160M04E-60J3	60ns	Normal	EDO	Extended	SOJ 300mil 26(24)L
GLT4160M04E-70J3	70ns	Normal	EDO	Extended	SOJ 300mil 26(24)L
GLT4160M04E-80J3	80ns	Normal	EDO	Extended	SOJ 300mil 26(24)L
GLT4160M04S-60J3	60ns	Normal	EDO	Self Refresh	SOJ 300mil 26(24)L
GLT4160M04S-70J3	70ns	Normal	EDO	Self Refresh	SOJ 300mil 26(24)L
GLT4160M04S-80J3	80ns	Normal	EDO	Self Refresh	SOJ 300mil 26(24)L
GLT4160M04-60TC	60ns	Normal	EDO	Commercial	TSOPII 300mil 26(24)L
GLT4160M04-70TC	70ns	Normal	EDO	Commercial	TSOPII 300mil 26(24)L
GLT4160M04-80TC	80ns	Normal	EDO	Commercial	TSOPII 300mil 26(24)L
GLT4160M04E-60TC	60ns	Normal	EDO	Extended	TSOPII 300mil 26(24)L
GLT4160M04E-70TC	70ns	Normal	EDO	Extended	TSOPII 300mil 26(24)L
GLT4160M04E-80TC	80ns	Normal	EDO	Extended	TSOPII 300mil 26(24)L
GLT4160M04S-60J3	60ns	Normal	EDO	Self Refresh	TSOPII 300mil 26(24)L
GLT4160M04S-70J3	70ns	Normal	EDO	Self Refresh	TSOPII 300mil 26(24)L
GLT4160M04S-80J3	80ns	Normal	EDO	Self Refresh	TSOPII 300mil 26(24)L

Parts Numbers (Top Mark) Definition :



Package Information

300mil 24/26 Lead Thin Small Outline Package SOJ



300mil 24/26 Lead Thin Small Outline Package (TSOP) TYPE II