G-LINK Technology

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GLT41316

64K x 16 CMOS Dynamic RAM with Fast Page Mode

Features

- 65,536 words by 16 bits organization
- Fast access time and cycle time
- Dual $\overline{WE}$ Input
- Low power dissipation
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh and Test Mode Capability
- 256 refresh cycles per 4 ms
- Available in 40-Pin 400 mil SOJ and 40/44-Pin TSOPII
- Single 5.0 V ±10% Power Supply
- All inputs and Outputs are TTL compatible
- Fast Page Mode operation

General Description

The GLT41316 is a 65,536 x 16 bit high-performance CMOS dynamic random access memory. The GLT41316 offers Fast Page Mode and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{WE}$ pins. The GLT41316 has symmetric address and accepts 256-cycle refresh in 4 ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 256x16 bits, within a page, with cycle times as short as 21ns.

The GLT41316 is best suited for graphics, and DSP applications requiring high performance memories.

Functional Block Diagram

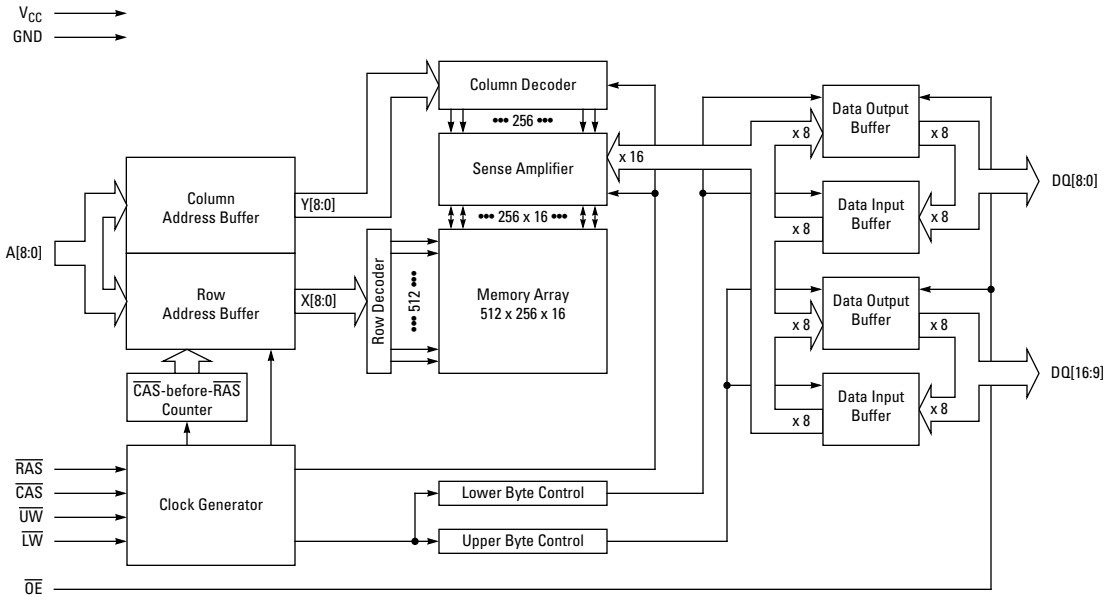


Figure 1. GLT41316 64K x 16 CMOS

Signal Descriptions

Name	Function
A[7:0]	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read / Upper Byte Write Enable
$\overline{LW}$	Read / Lower Byte Write Enable
$\overline{OE}$	Output Enable
DQ[15:0]	Data Inputs / Outputs
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{UW}$	$\overline{LW}$	$\overline{OE}$	Address	DQs	Notes
Standby		H	H → X	X	X	X		High-Z	
Read: Word		L	L	H	H	L	ROW/COL	Data Out	
Write: Word (Early Write)		L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)		L	L	H	L	X	ROW/COL	Lower Byte, Data-In Upper Byte, High-Z	
Write: Upper Byte (Early)		L	L	L	H	X	ROW/COL	Lower Byte, High-Z Upper Byte, Data-In	
Read Write		L	L	H → L	H → L	L → H	ROW/COL	Data-Out, Data-In	[1] [2]
Fast-Page-Mode Read	1st Cycle	L	H → L	H	H	L	ROW/COL	Data-Out	[1]
	2nd Cycle	L	H → L	H	H	L	COL	Data-Out	
Fast-Page- Mode Write	1st Cycle	L	H → L	L	L	X	ROW/COL	Data-In	
	2nd Cycle	L	H → L	L	L	X	COL	Data-In	
Fast-Page-Mode Read-Write	1st Cycle	L	H → L	H → L	H → L	L → H	ROW/COL	Data-Out, Data-In	
	2nd Cycle	L	H → L	H → L	H → L	L → H	COL	Data-Out, Data-In	
Hidden Refresh	Read	L → H → L	L	H	L	L	ROW/COL	Data-Out	
	Write	L → H → L	L	L	L	X	ROW/COL	Data-In	[2] [3]
$\overline{RAS}$-Only Refresh		L	H	X	X	X	ROW	High-Z	
CBR Refresh		H → L	L	X	X	X		High-Z	

1. These READ cycles are always WORD READ cycles.
2. These WRITE cycles may also be BYTE READ cycles (either $\overline{UW}$ or $\overline{LW}$ active)
3. EARLY WRITE only.

Electrical Specifications

Absolute Maximum Ratings [1] [2] [3] [4]

Parameter	Rating	Unit
Operating Temperature, T_A (ambient)	-0 to +70	°C
Storage Temperature (plastic)	-55 to +125	°C
Voltage Relative to V_{SS}	-1.0 to + 7.0	V
Short Circuit Output Current	50	mA
Power Dissipation	1.0	W

1. Operation above Absolute Maximum Ratings can adversely affect device reliability.
2. $\overline{WE}$ means $\overline{UW}$ and $\overline{LW}$.
3. All voltages are referenced to GND.
4. After power up, wait more than 100 ms and then, execute eight $\overline{CAS}$-before- $\overline{RAS}$ or $\overline{RAS}$-only refresh cycles as dummy cycles to initialize internal circuit.

Capacitance [1] (T_A = 25°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Symbol	Parameter	Max	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$	7	pF
C_{OUT}	Data Input/Output	7	pF

1. Capacitance is sampled and not 100% tested

DC Characteristics (T_A = 0°C to 70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified) [1] [2]

			-35		-40		-45		-50			
Symbol	Parameter	Test Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	0 V ≤ V_{IN} ≤ 5.5 V (All other pins not under test = 0 V)	-10	+10	-10	+10	-10	+10	-10	+10	µA	
I_{LO}	Output Leakage Current (for High-Z State)	0 V ≤ V_{OUT} ≤ 5.5 V Output is disabled (Hi-Z)	-10	+10	-10	+10	-10	+10	-10	+10	µA	
I_{CC1}	Operating Current, Random READ/WRITE	t_{RC} = t_{RC} (min)		170		160		150		140	mA	[1] [2]
I_{CC2}	Standby Current (TTL)	$\overline{RAS}$, $\overline{CAS}$, at V_{IH} other inputs ≥ V_{SS}		2		2		2		2	mA	
I_{CC3}	Refresh Current, $\overline{RAS}$ -Only	RAS cycling, $\overline{CAS}$ at V_{IH} t_{RC} = t_{RC} (min)		170		160		150		140	mA	[2]
I_{CC4}	Operating Current, EDO Page Mode	$\overline{RAS}$ at V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} (min)		170		160		150		140	mA	[1] [2]
I_{CC5}	Refresh Current, $\overline{CAS}$ Before $\overline{RAS}$	$\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} (min)		170		160		150		140	mA	[1]
I_{CC6}	Standby Current (CMOS)	$\overline{RAS}$ ≥ V_{CC} -0.2 V, $\overline{CAS}$ ≥ V_{CC} -0.2V, All other inputs ≥ V_{SS}		1		1		1		1	mA	
V_{IL}	Input Low Voltage		-1	+0.8	-1	+0.8	-1	+0.8	-1	+0.8	V	[3]
V_{IH}	Input High Voltage		2.4	V_{CC}+1	2.4	V_{CC}+1	2.4	V_{CC}+1	2.4	V_{CC}+1	V	[3]
V_{OL}	Output Low Voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4		0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4		2.4		2.4		2.4		V	

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC} (max) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions specified. I_{CC} (max) is measured with a maximum of one transition per address cycle in random Read/Write and Fast Page Mode.
3. Specified V_{IL} (min) is steady state operation. During transitions, V_{IL} (min) may undershoot to -1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{CC}.

AC Characteristics ($0°C \le T_A \le 70°C$) (V_{CC} = 5.0 V ±10%, V_{IH}/V_{IL} = 2.4 V/0.8 V, V_{OH}/V_{OL} = 2.4 V/0.4 V) [1] [2]

Symbol	Parameter	-35		-40		-45		-50		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Read/Write Cycle Time	70	-	75	-	80	-	90	-	ns	
t_{RWC}	Read Modify Write Cycle Time	99	-	105	-	110	-	121	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	35	-	40	-	45	-	50	ns	[3] [4]
t_{CAC}	Access Time from $\overline{CAS}$	-	11	-	12	-	12	-	13	ns	[3] [4]
t_{AA}	Access Time from Column Address	-	18	-	20	-	22	-	25	ns	[3] [4]
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	0	-	ns	[3]
t_{OFF}	Output Buffer Turn-off Delay from $\overline{CAS}$	3	8	3	8	3	8	3	8	ns	[5]
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	[2]
t_{RP}	$\overline{RAS}$ Precharge Time	25	-	25	-	25	-	30	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	35	100K	40	100K	45	100K	50	100K	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	12	-	12	-	13	-	14	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	36	-	40	-	46	-	51	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	12	10000	12	10000	13	10000	14	10000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	17	24	18	28	18	33	19	37	ns	[4]
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	12	17	13	20	13	23	14	25	ns	[4]
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	5	-	ns	[6]
t_{ASR}	Row Address Setup Time	0	-	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	7	-	8	-	8	-	9	-	ns	
t_{ASC}	Column Address Setup Time	0	-	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	6	-	6	-	6	-	7	-	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	30	-	34	-	39	-	44	-	ns	
t_{RAL}	Column Address Lead Time Referenced to $\overline{RAS}$	18	-	20	-	23	-	25	-	ns	
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	0	-	ns	
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	0	-	ns	[7]
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	0	-	ns	[7]
t_{WCH}	$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	6	-	6	-	6	-	7	-	ns	[8]
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	30	-	34	-	39	-	44	-	ns	[9]
t_{WP}	$\overline{WE}$ Pulse Width	6	-	6	-	6	-	7	-	ns	[8]
t_{RWL}	$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	11	-	12	-	12	-	13	-	ns	
t_{CWL}	$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	11	-	12	-	12	-	13	-	ns	
t_{DS}	Data-In Setup Time	0	-	0	-	0	-	0	-	ns	[10]
t_{DH}	Data-In Hold Time	7	-	8	-	8	-	9	-	ns	[10]
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	31	-	36	-	41	-	46	-	ns	[11]
t_{REF}	Refresh Time (256 cycles)	-	4	-	4	-	4	-	4	ms	
t_{WCS}	$\overline{WE}$ Setup Time	0	-	0	-	0	-	0	-	ns	[9]
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	58	-	63	-	68	-	73	-	ns	[9]
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	29	-	30	-	30	-	31	-	ns	[9]
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	36	-	38	-	40	-	43	-	ns	[9]
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	-	5	-	5	-	5	-	ns	

AC Characteristics ($0°C \le T_A \le 70°C$) (V_{CC} = 5.0 V ±10%, V_{IH}/V_{IL} = 2.4 V/0.8 V, V_{OH}/V_{OL} = 2.4 V/0.4 V) [1] [2]

Symbol	Parameter	-35		-40		-45		-50		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	-	10	-	10	-	10	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time (CBR Counter Test Cycle)	20	-	20	-	20	-	20	-	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	21	-	23	-	25	-	30	ns	[3]
t_{PC}	Fast Page Mode Read/Write Cycle Time	21	-	23	-	25	-	30	-	ns	
t_{PRWC}	Fast Page Mode Read Modify Write Cycle Time	60	-	63	-	65	-	71	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	6	-	7	-	7	-	8	-	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	35	100K	40	100K	45	100K	50	100K	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	25	-	25	-	30	-	30	-	ns	
t_{OEA}	Access Time from $\overline{OE}$	-	11	-	12	-	12	-	13	ns	
t_{OED}	$\overline{OE}$ to Delay Time	8	-	8	-	8	-	8	-	ns	
t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	3	8	3	8	3	8	3	8	ns	[5]
t_{OEH}	$\overline{OE}$ Hold Time	6	-	7	-	7	-	7	-	ns	
t_{WHR}	$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	15	-	15	-	15	-	15	-	ns	

1. An initial pause of 100µs is required after power-up followed by any 8 $\overline{RAS}$-only Refresh or $\overline{CAS}$-before-$\overline{RAS}$ Refresh cycles to initialize the internal circuit.
2. $V_{IH\ (min)}$ and $V_{IL\ (min)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH\ (min)}$ and $V_{IL\ (max)}$, AC measurements assume T_T = 5 ns.
3. Measured with an equivalent to 2 TTL loads and 100 pF.
4. For read cycles, the access time is defined as follows:

Input Conditions	Access Time
$t_{RAD} \le t_{RAD\ (max)}$ and $t_{RCD} \le t_{RCD\ (max)}$	$t_{RAC\ (max)}$
$t_{RAD\ (max)} < t_{RAD}$ and $t_{RCD} \le t_{RCD\ (max)}$	$t_{AA\ (max)}$
$t_{RCD\ (max)} < t_{RCD}$	$t_{CAC\ (max)}$

   $t_{RAD\ (max)}$ and $t_{RCD\ (max)}$ indicate the points which the access time changes and are not the limits of operation.
5. $t_{OFF\ (max)}$ and $t_{OEZ\ (max)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
6. $t_{CRP\ (min)}$ requirement should be applicable for $\overline{RAS}$, $\overline{CAS}$ cycle preceded by any cycles.
7. Either $t_{RCH\ (min)}$ or $t_{RRH\ (min)}$ must be satisfied for a read cycle.
8. $t_{WP\ (min)}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH\ (min)}$ should be satisfied.
9. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \ge t_{WCS\ (min)}$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \ge t_{CWD\ (min)}$, $t_{RWD} \ge t_{RWD\ (min)}$ and $t_{AWD} \ge t_{AWD\ (min)}$, then the cycle is a Read-Modify-Write Cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
10. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.
11. t_{AR}, t_{WCR}, and t_{DHR} are referenced to $t_{RAD\ (max)}$.

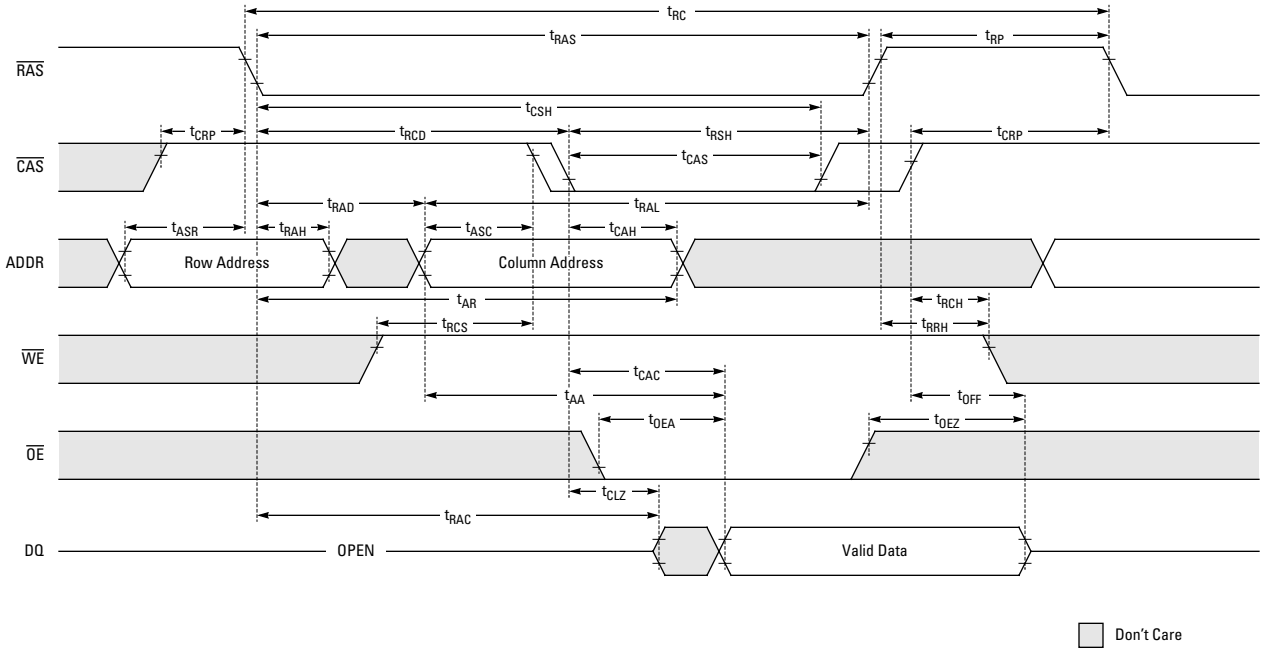


Figure 2. Read Cycle

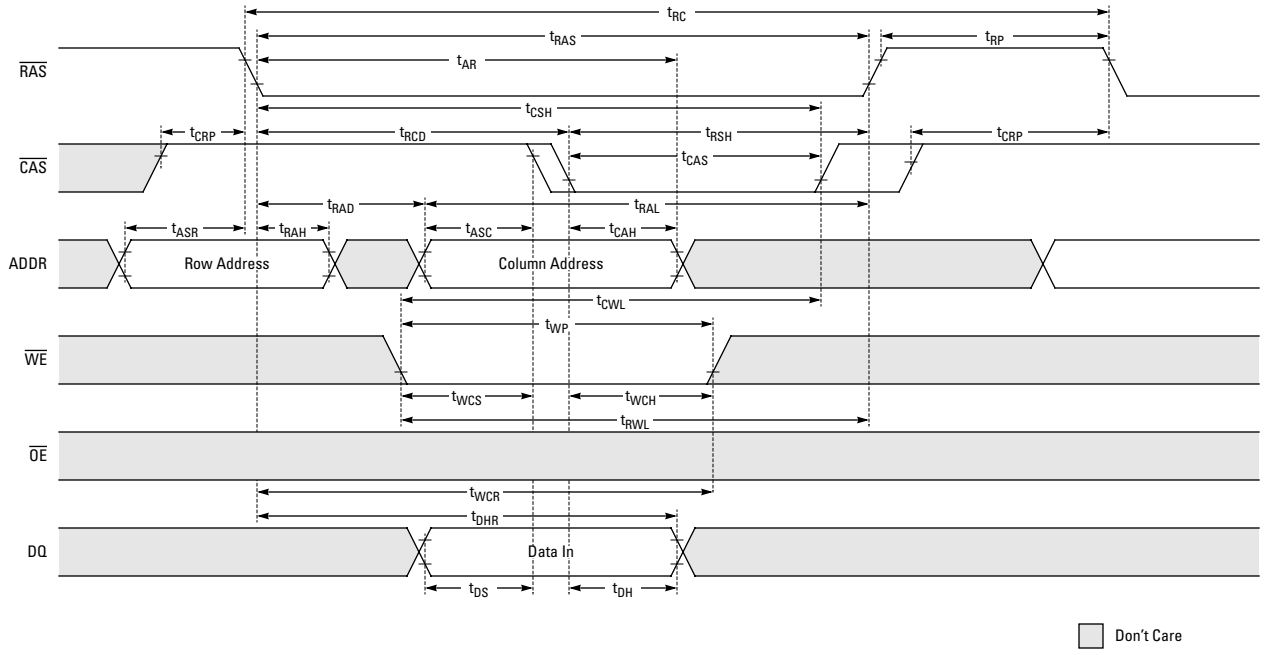


Figure 3. Early Write Cycle

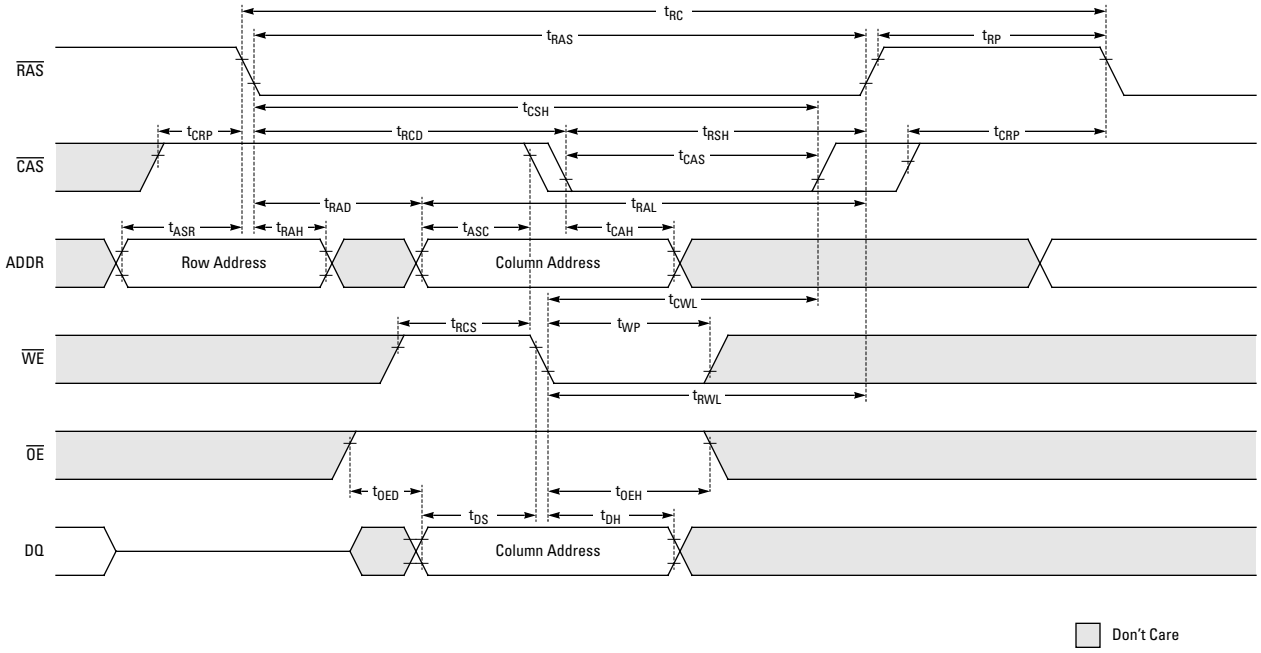


Figure 4. Late Write Cycle ($\overline{OE}$ Controlled Write)

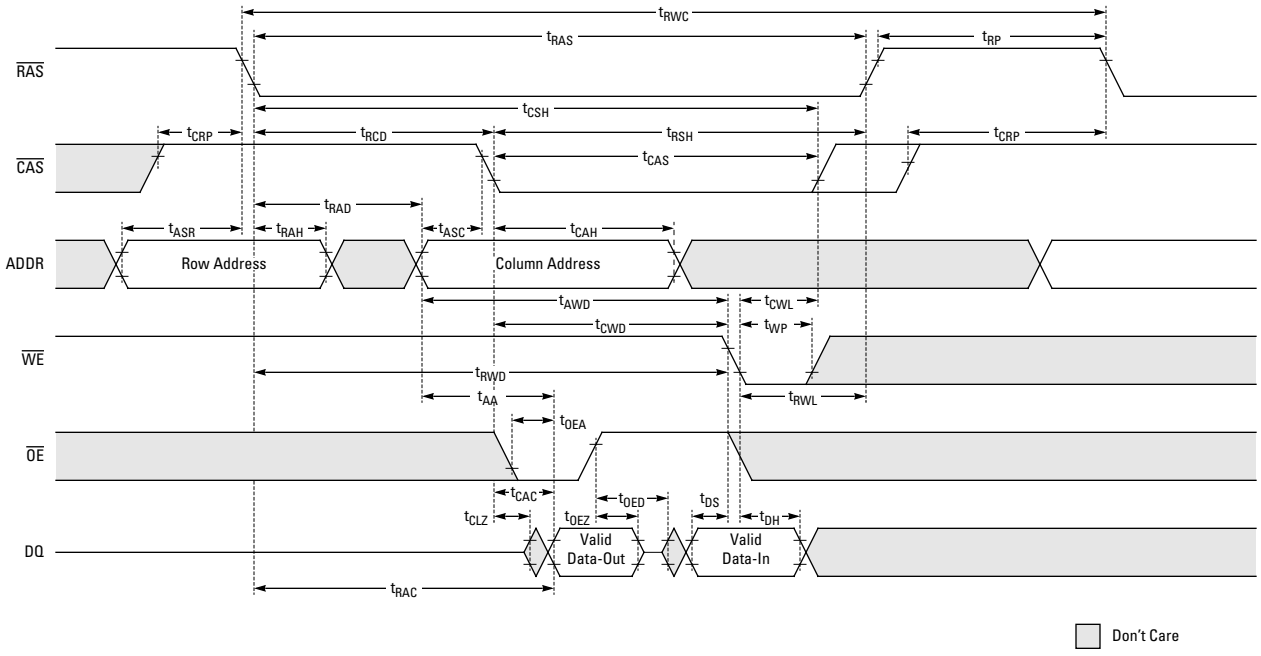


Figure 5. Read-Modify-Write Cycle

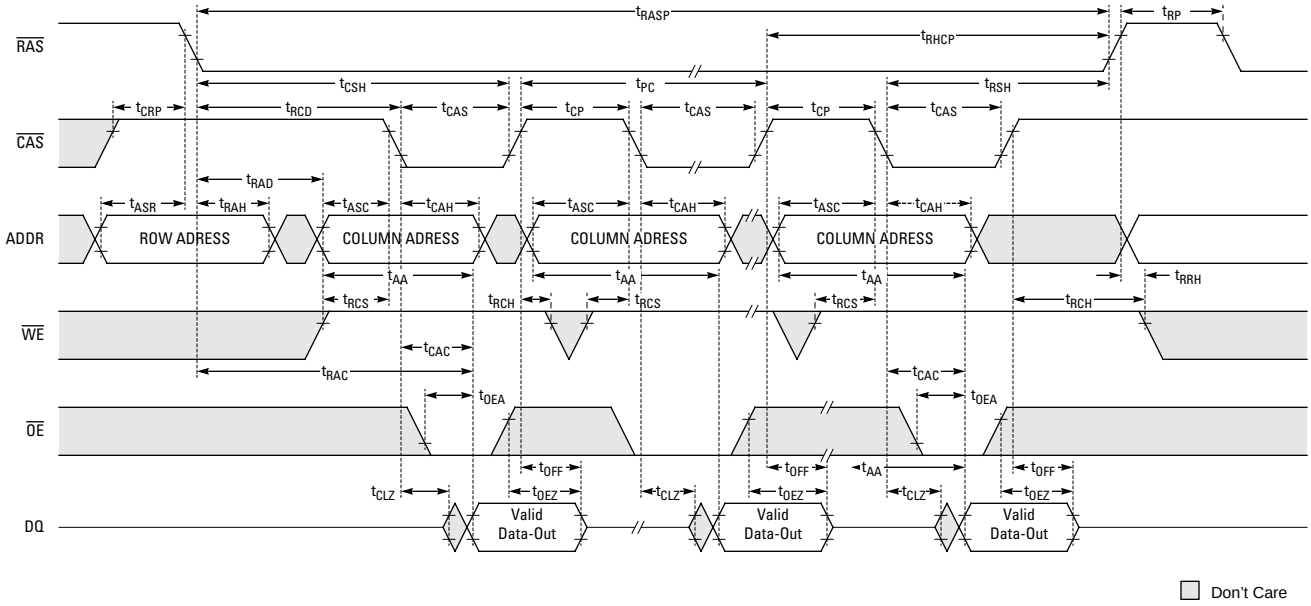


Figure 6. Fast Page Read Cycle

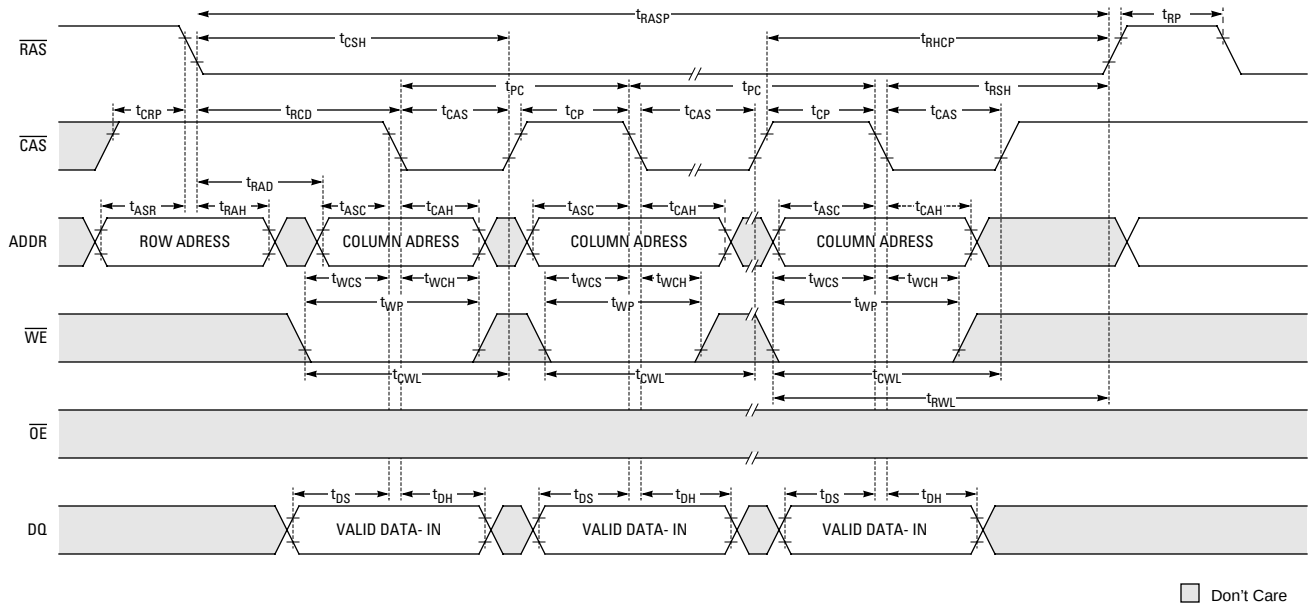


Figure 7. Fast Page Write Cycle

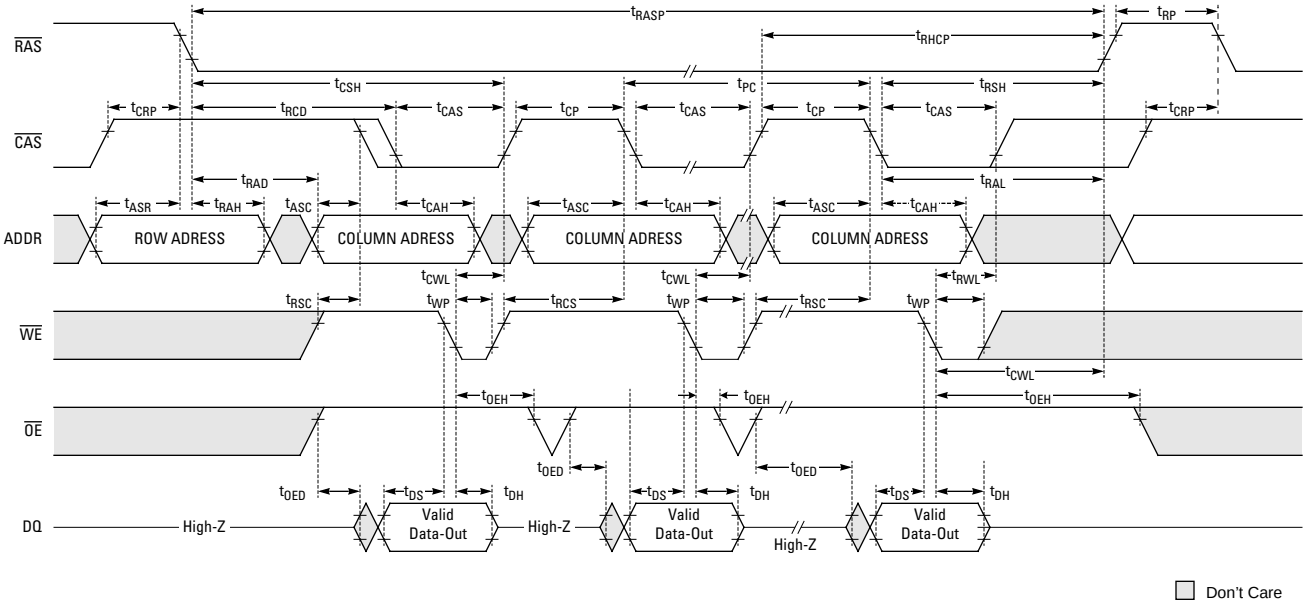


Figure 8. Fast Page Mode Late Write Cycle

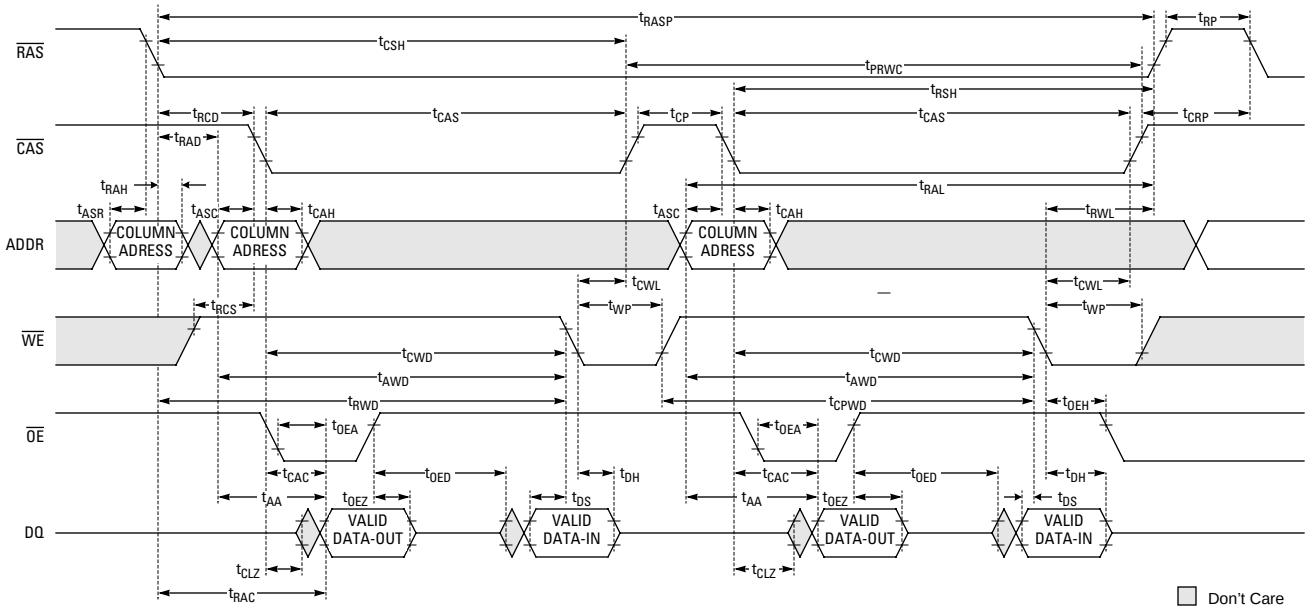
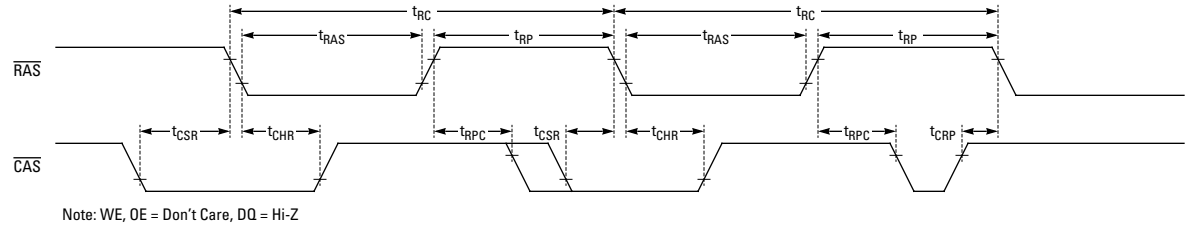
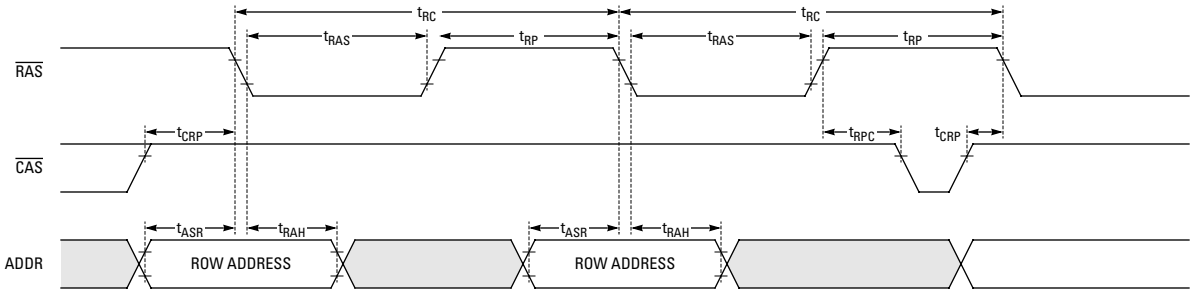


Figure 9. Fast Page Read-Modify-Write Cycle



Note: WE, OE = Don't Care, DQ = Hi-Z

Figure 10. $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



Note: WE, OE = Don't Care, DQ = Hi-Z

Figure 11. $\overline{RAS}$-Only Refresh Cycle

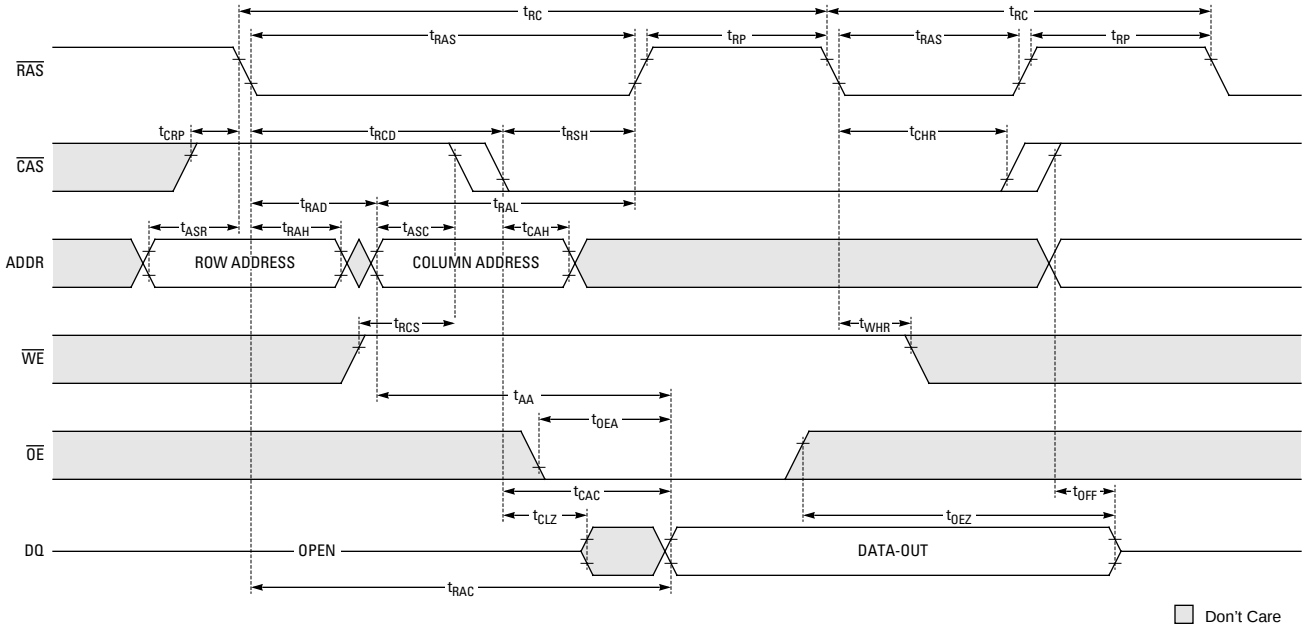


Figure 12. Hidden Refresh Cycle (Read)

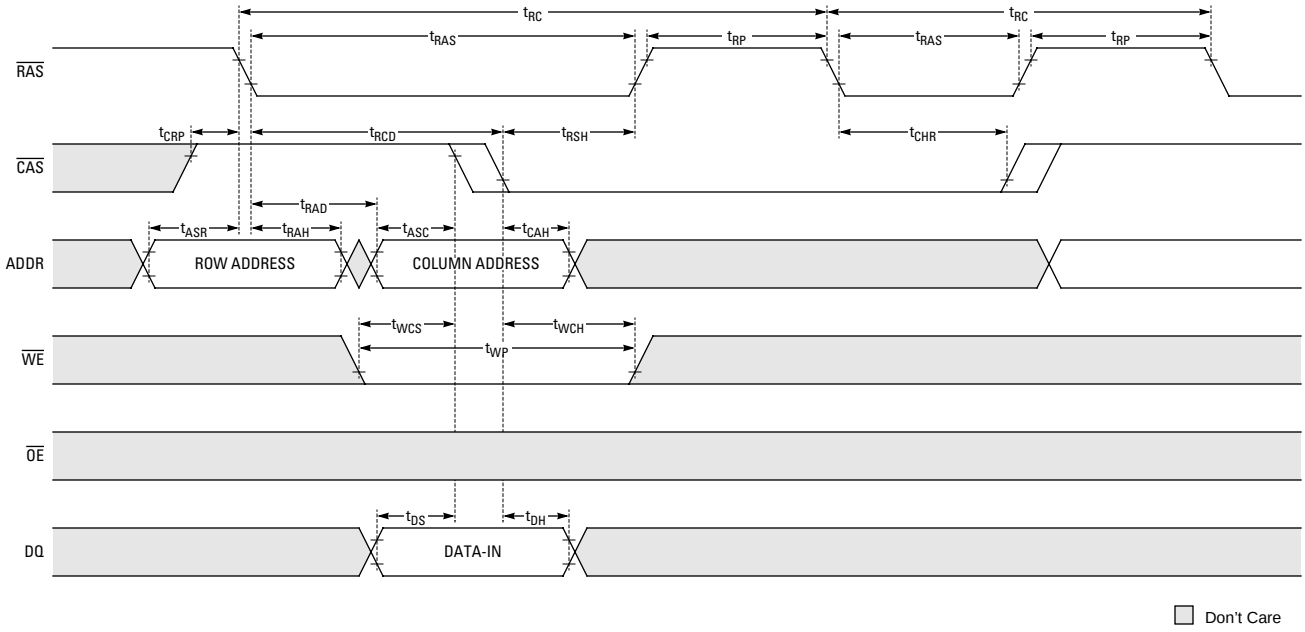


Figure 13. Hidden Refresh Cycle (Write)

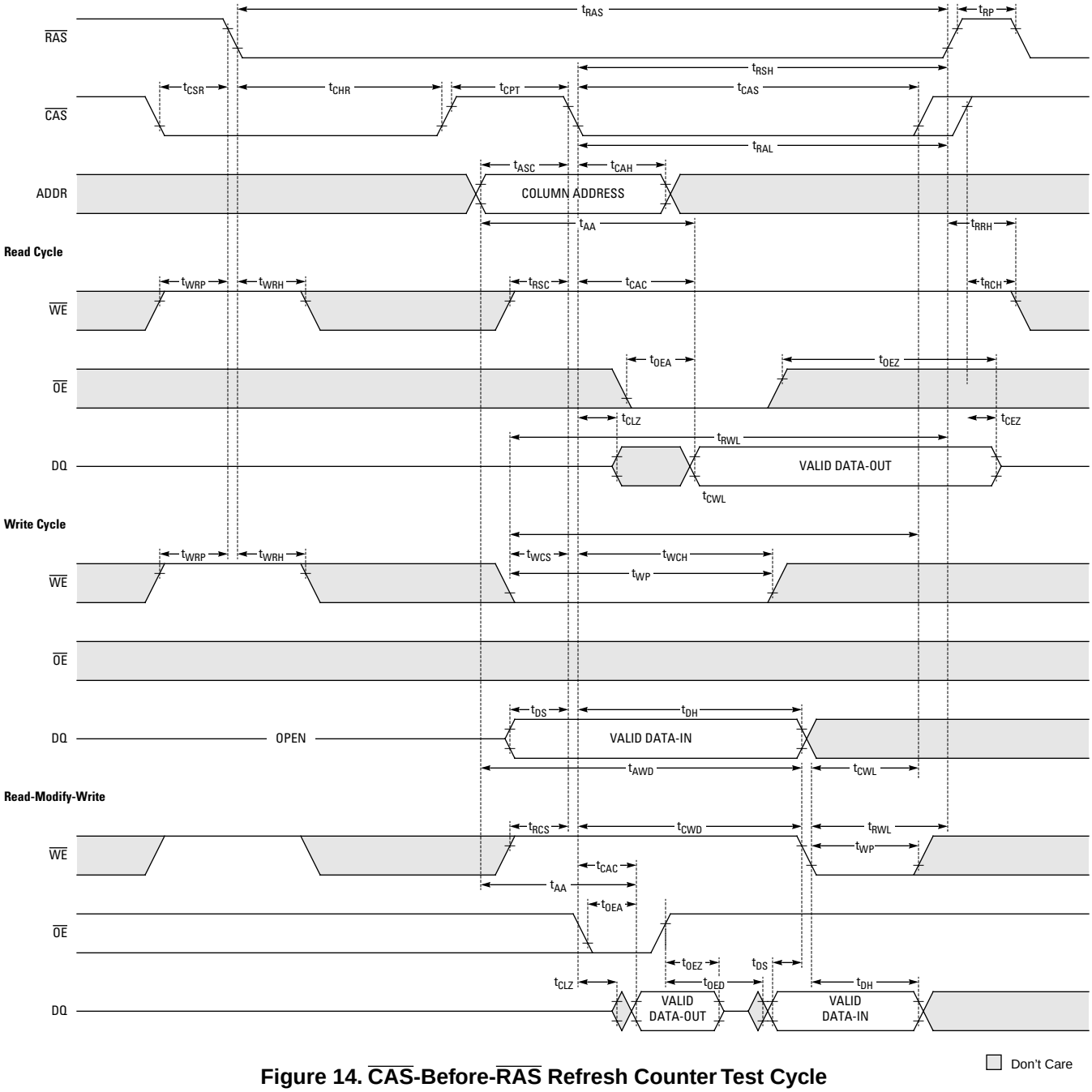


Figure 14. $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

PACKAGING INFORMATION

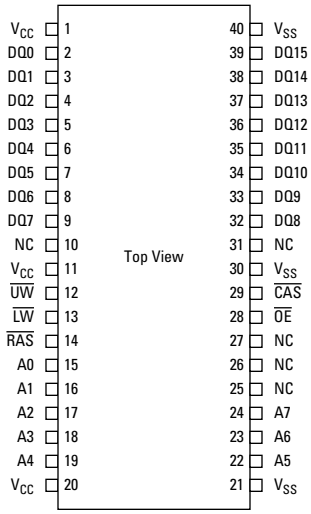


Figure 15. 40-Pin 400 mil Plastic SOJ Pin Assignment

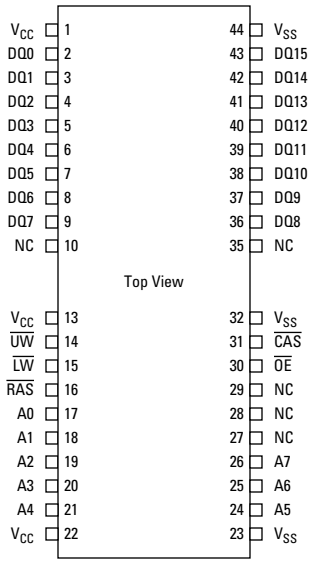
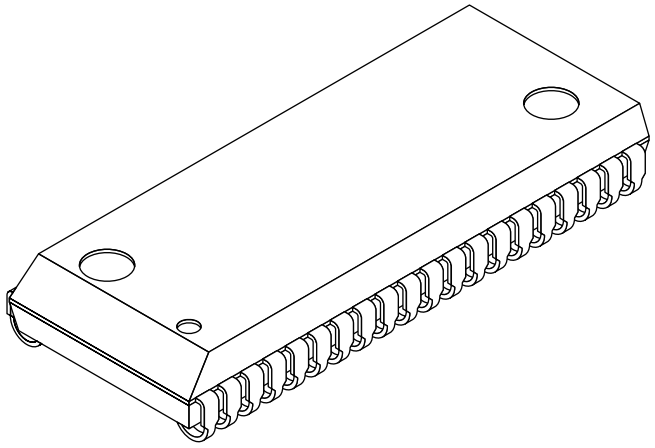


Figure 16. 44/40-Pin 400 mil TSOP (Type II) Pin Assignment



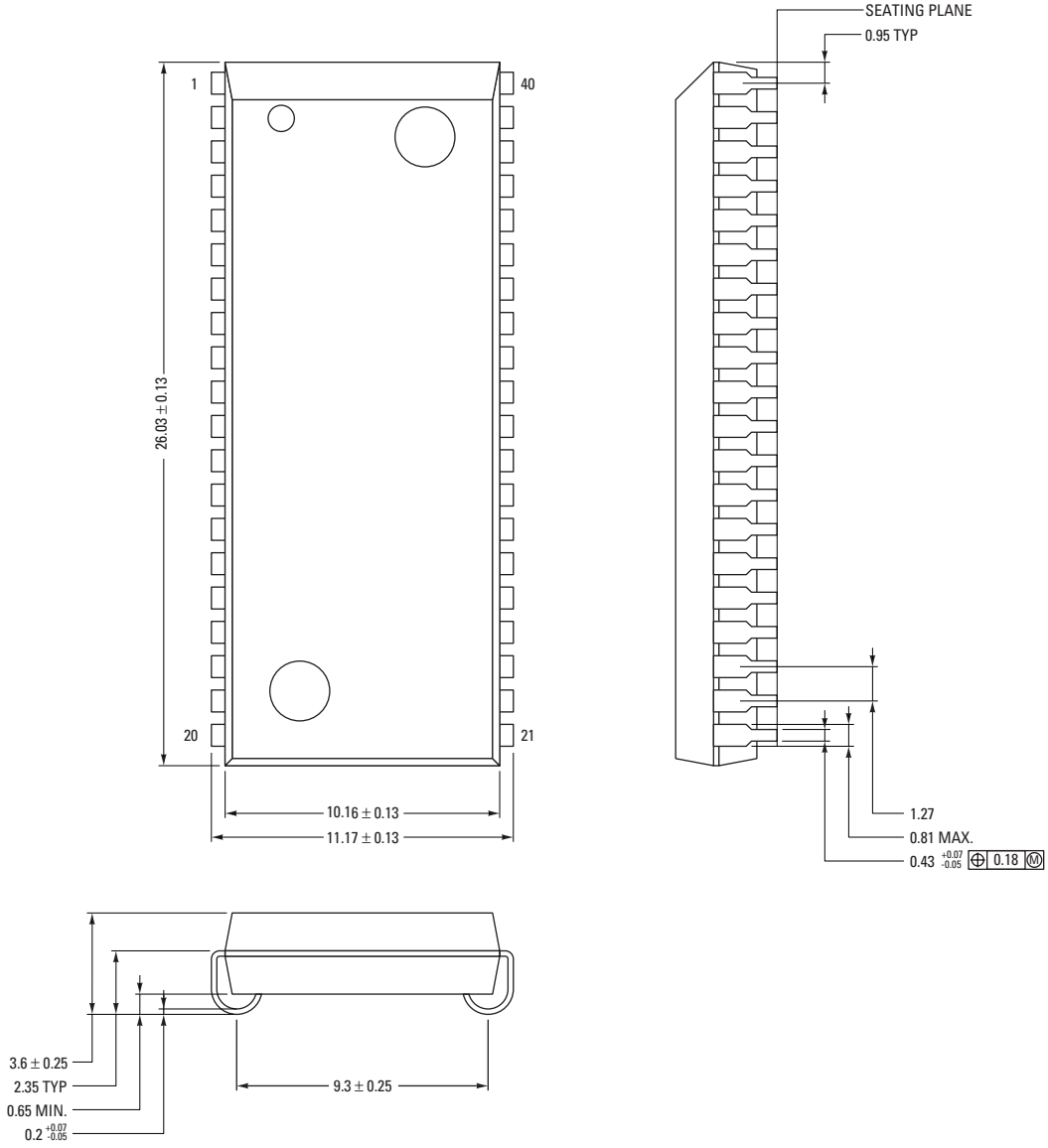
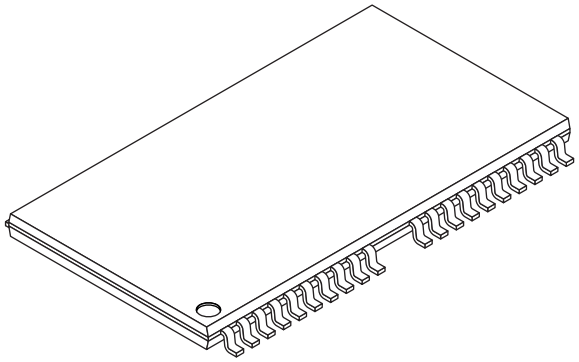


Figure 17. 40-Pin 400 mil Package Dimensions



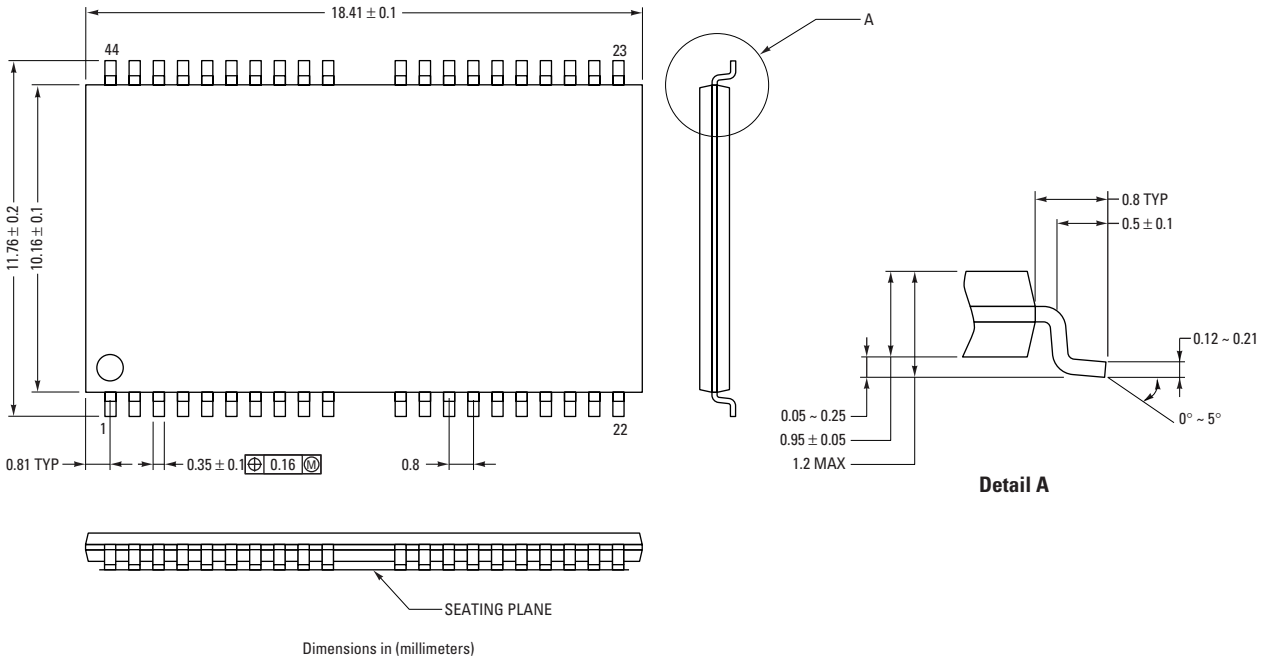


Figure 18. 40/44 TSOP (Type II) Package Dimensions

Ordering Information

Part Number	Speed	Power	Feature	Package
GLT41316-35J4	35 ns	Normal	FPM	40-Pin 400 mil SOJ
GLT41316-40J4	40 ns	Normal	FPM	40-Pin 400 mil SOJ
GLT41316-45J4	45 ns	Normal	FPM	40-Pin 400 mil SOJ
GLT41316-50J4	50 ns	Normal	FPM	40-Pin 400 mil SOJ
GLT41316-35TC	35 ns	Normal	FPM	44-Pin 400 mil TSOP
GLT41316-40TC	40 ns	Normal	FPM	44-Pin 400 mil TSOP
GLT41316-45TC	45 ns	Normal	FPM	44-Pin 400 mil TSOP
GLT41316-50TC	50 ns	Normal	FPM	44-Pin 400 mil TSOP

Notes:

Notes:

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