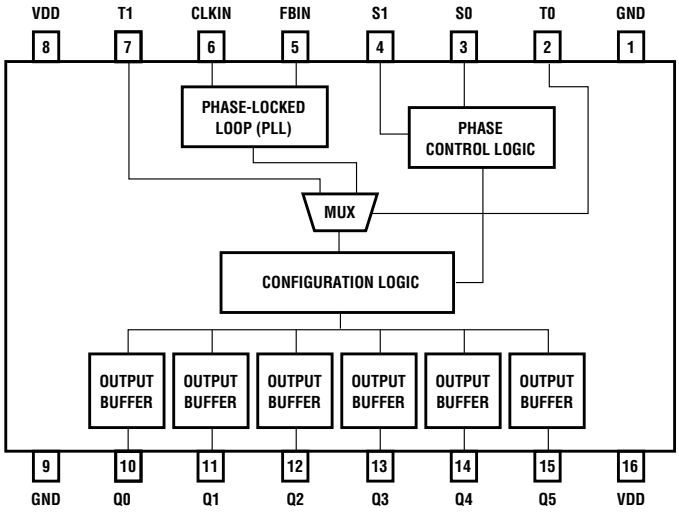
GA1110E

Multi-Phase Clock Buffer

Figure 1. Block Diagram



TriQuint's GA1110E is a low-skew TTL-level clock buffer chip with multi-phase clock generation. It produces multiple clock outputs which are normally phase- and frequency-synchronized to a periodic clock input signal. It offers the user the additional flexibility to adjust the phase of the individual outputs in increments of ± 2.5 ns. With the precise placement of output clock edges relative to a system clock input, the GA1110E can provide a complete system clocking solution.

The tight control over the phase and frequency of the output clocks is achieved with a 400 MHz internal phase-locked loop (PLL). By feeding back one of the output clocks (to FBIN), the on-chip PLL can continuously maintain synchronization between the input clock (CLKIN) and all six outputs. Any drift or gradual variation in the system clock will be matched and tracked at the six outputs.

The GA1110E offers the user fourteen different output clock configurations. Using the external feedback capability and the two select pins (S1 and S0), the desired phase relationships (among the 14 possibilities) of the output clocks may be chosen to best solve the system's clocking requirements. The output clock edges are "placed" in precise, digitally-controlled ± 2.5 ns increments relative to the input and feedback clock phase. The fourteen "phase-relationship" options are listed in Table 1 and example waveforms and block diagrams are shown in Figures 5 through 8.

Features

- *Zero-propagation-delay clock buffer*
- *Output skew controlled to ±250 ps (typ.), ± 500 ps (max.)*
- *Self-contained on-chip 400 MHz phase-locked loop (PLL)*
- *User-selectable phase shifting on the output clocks in 2.5 ns increments.*
- *Available in 20, 25, 33, 40 and 50 MHz versions*
- *High-drive, symmetric TTL-compatible outputs with rise time of 1.0 ns*
- *Special test mode*
- *130 mA operating current (typ.), 160 mA (max.)*
- *Standard 16-pin DIP and 28-pin surface-mount packages*

The GA1110E is fabricated using TriQuint's One-Up™ gallium arsenide technology to achieve precise timing control and to guarantee 100% TTL-compatibility. The 20, 25, 33, 40 and 50 MHz input frequencies make this device ideal for clock distribution, phase adjustment, and clock skew control in a wide range of high-performance RISC- and CISC-based systems.

Functional Description

The GA1110E TTL-level clock buffer/phase generator chip provides multiple outputs synchronized in phase and frequency to a periodic clock input. The chip utilizes two select pins and external feedback to allow the user to "phase-adjust" the outputs relative to the input clock. The phase adjustments can be made in increments of t_{PH}; this value is given in the AC Characteristics table.

Table 1 enumerates the fourteen configurations available to the user. The first two columns specify the signal levels on the select pins S1 and S0. These are active-HIGH signals. The third column indicates which output (Q0..5) should be externally connected to the feedback input (FBIN) to achieve the desired phase relationship shown for a given configuration in the table. The last six columns specify the resulting phase relationship of each output to the user clock input (CLKIN). A negative value is the time by which the output rising edge precedes the input (CLKIN) rising edge, while a positive value is the time by which the output rising edge follows the input (CLKIN) rising edge.

> ***Example:*** *The system clocking requirements may specify several low-skew outputs, one early clock, one late clock, and one inverted clock.*
>
> *Configuration 3 in Table 1 provides such a solution. With S1 = LOW, S0 = HIGH, and Q0 (or Q1 or Q4) connected back to FBIN, the required outputs will be generated. Q0, Q1 and Q4 will be phase-aligned to the input (CLKIN), Q3 will provide an early clock (by one t_{PH}, the phase-shift increment), Q2 will provide the late clock (by one t_{PH}), and Q5 will provide a phase-aligned, inverted copy of the input. The GA1110E's PLL will maintain these phase relationships continually, as shown in Figure 6.*

Several of the operating configurations in Table 1 include inverted clock outputs. If the inverted clock is aligned to the input (i.e. exactly 180 degrees out of phase), the table entry reads as "I". If this inverted clock is also phase-shifted, the phase shift is relative to CLKIN and is specified as "I+t" or "I–t."

> ***Example:*** *Configuration 5 of the table corresponds to S1 = LOW, S0 = HIGH and Q3 connected to FBIN. In this case, Q3 is phase-aligned to the input clock (CLKIN), Q0, Q1 and Q4 are phase-delayed by one t_{PH}, Q2 is phase-delayed by two t_{PH}s, and the Q5 output is an inverted copy of CLKIN, phase-delayed by one t_{PH}.*

Multiple-Chip Applications

Because of the tight input-output phase control, the GA1110E can be easily cascaded to build low-skew clock chains and clock trees. The problem of clock fanout can be solved with minimal skew between any two clocks in the chain. This can be done on a single circuit board, as well as across a backplane to maintain synchronization throughout multiple boards in a system.

Breaking the Feedback Loop

There is no requirement that the external feedback connection be a direct hardwire from an output pin to the FBIN pin. So long as the signal at FBIN is derived directly from one of the output pins and maintains its frequency, additional logic incorporating any delay whatsoever can be accommodated. The internal phase-locked loop will adjust the output clocks on the GA1110E to ensure zero phase-delay between the FBIN and CLKIN signals. This feature is extremely valuable in synchronizing ASICs to the system clock.

Caution: The signal at FBIN must be continuous (i.e. not a gated or conditional signal), and must be derived directly from one of the GA1110E's outputs.

Power-Up/Reset Synchronization

The GA1110E utilizes on-chip phase-locked loop technology to maintain synchronization between inputs and outputs. Whenever the device is powered up, or the system clock (CLKIN) is reset, the phase-locked loop requires a synchronization time (t_{SYNC}) before lock is achieved. The maximum time required is specified in the AC Characteristics table.

For lock to occur, one of the outputs must always be connected (either directly or through additional ICs) to the FBIN input.

Other TriQuint Clock Devices

TriQuint also offers the GA1210E, a low-skew TTL-level clock doubler. Using on-board PLL technology, the GA1210E generates multiple 2X clock outputs from a single input at 20, 25, 33, 40, or 50 MHz. By feeding back one of the outputs, a typical delay of $\pm$ 250 ps through the part is achieved. Skew across all six outputs is typically $\pm$ 250 ps.

GA1110E Test Mode

The GA1110E has a test mode which can be enabled if the test pin T0 is HIGH. Under that condition, the clock signal from the test pin T1 is used as the clock input to the configuration logic, instead of the output from the PLL. This mode can be used to test only the internal state machine and associated logic. Each speed type and configuration has a unique signature which is present at the output after "n" number of input clock pulses. [For the GA1110E-25 there will be one output clock cycle for every 16 input clock cycles from t_0.]

The figures below show the test mode and associated timing for Configuration 1 of the GA1110E-25. (See Configuration 1 in Table 1.) When powered up, the Q0 through Q5 outputs can be in any state. It can take up to 16 clocks to get the outputs to the predetermined state at t_0. The number of clock cycles at input T1 required for one output clock cycle is 20 for GA1110E-20, 12 for the GA1110E-33, 10 for the GA1110E-40 and 8 for the GA1110E-50.

The test input clock at T1 can either be used to single-step the outputs, or it can be clocked at rates up to 200 MHz. Please note that for the normal mode of operation, T0 is LOW (GND) and T1 can be HIGH (V_{DD}) or No Connect (N/C).

Figure 2. Test Mode for the GA1110E-25
(Configuration 1)

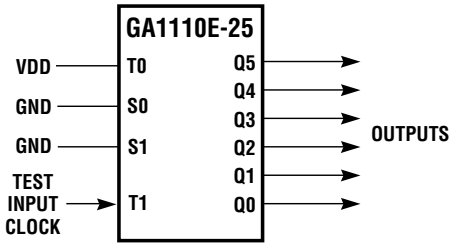
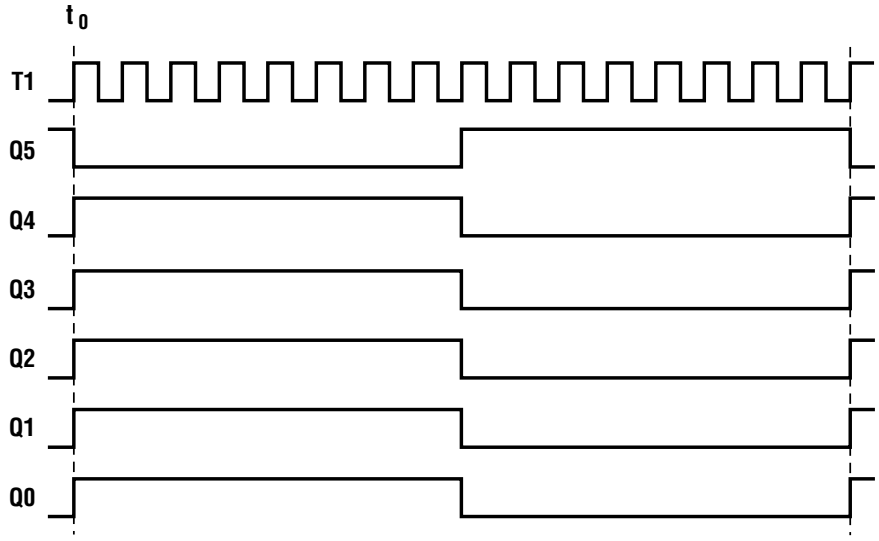


Figure 3. GA1110E-25 Test Mode Timing Waveform



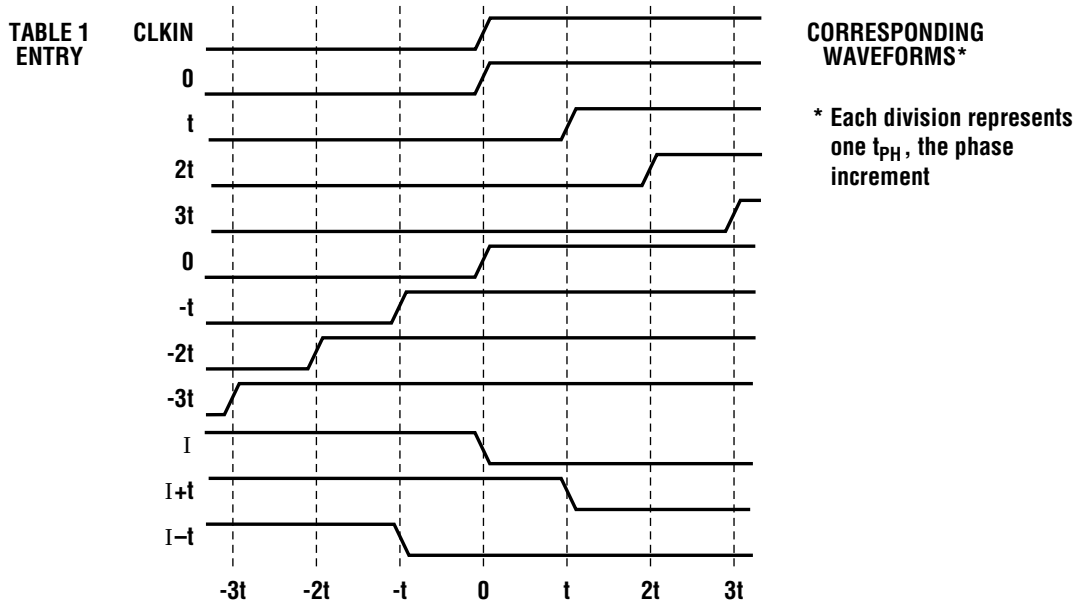
Note: The above timing applies to the case when S1 = S0 = 0 and T0 = 1 (test mode).

Table 1. Configuration Table

Configuration Number	Select Pins S1	Select Pins S0	Output Fed Back to FBIN	Output Phase Shift (see Figure 4) Q0	Q1	Q2	Q3	Q4	Q5
1	0	0	Q0..Q4	0	0	0	0	0	I
2	0	0	Q5	I	I	I	I	I	0
3	0	1	Q0, Q1, Q4	0	0	t	–t	0	I
4	0	1	Q2	–t	–t	0	–2t	–t	I–t
5	0	1	Q3	t	t	2t	0	t	I+t
6	0	1	Q5	I	I	I+t	I–t	I	0
7	1	0	Q0, Q2, Q3	0	t	0	0	–t	–2t
8	1	0	Q1	–t	0	–t	–t	–2t	–3t
9	1	0	Q4	t	2t	t	t	0	–t
10	1	0	Q5	2t	3t	2t	2t	t	0
11	1	1	Q0	0	t	t	–t	–t	–2t
12	1	1	Q1, Q2	–t	0	0	–2t	–2t	–3t
13	1	1	Q3, Q4	t	2t	2t	0	0	–t
14	1	1	Q5	2t	3t	3t	t	t	0

Notes: 1. "t" represents t_{PH}, the phase–shift increment specified on page 10.
2. A "0" phase implies the output is aligned to CLKIN.
3. A negative phase implies the output precedes CLKIN.
4. A positive phase implies the output follows CLKIN.
5. "I" implies an inverted version of CLKIN.

Figure 4. Legend



Configuration Examples

Following are four sample configurations corresponding to Table 1.

Figure 5. Configuration 1

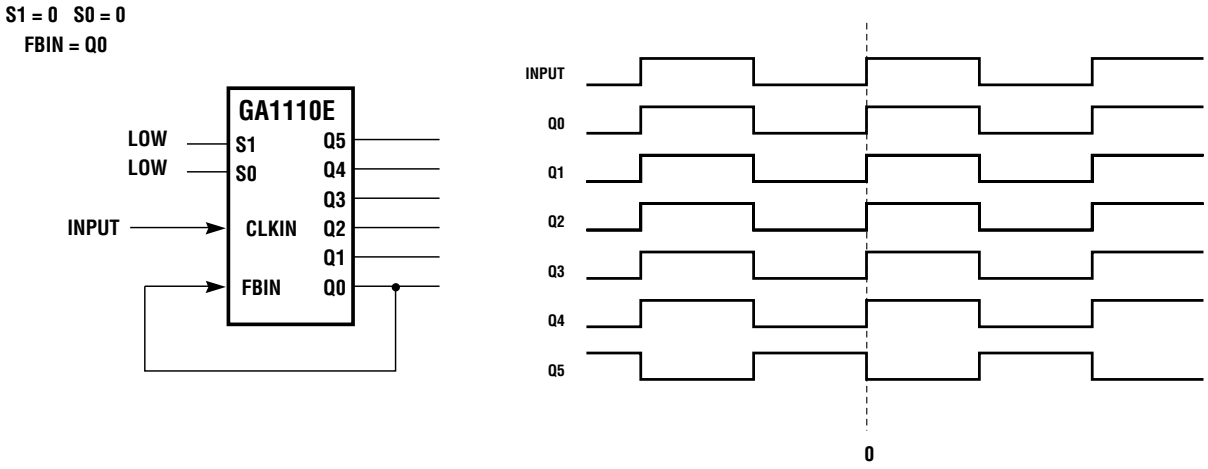


Figure 6. Configuration 3

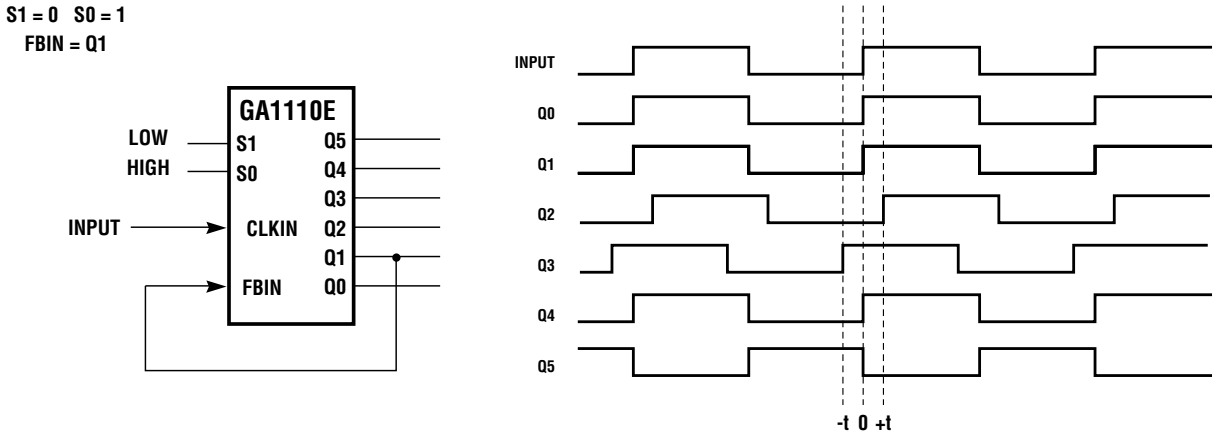


Figure 7. Configuration 8

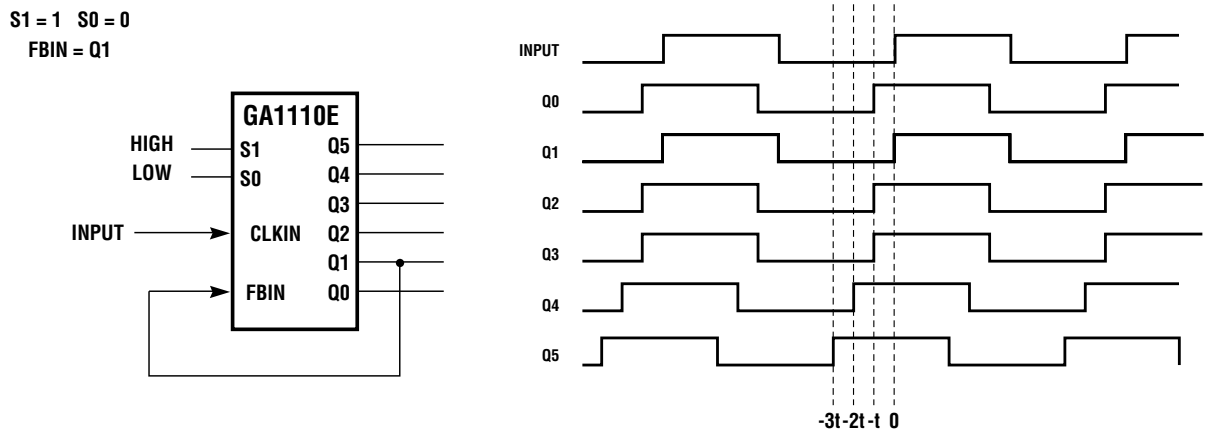
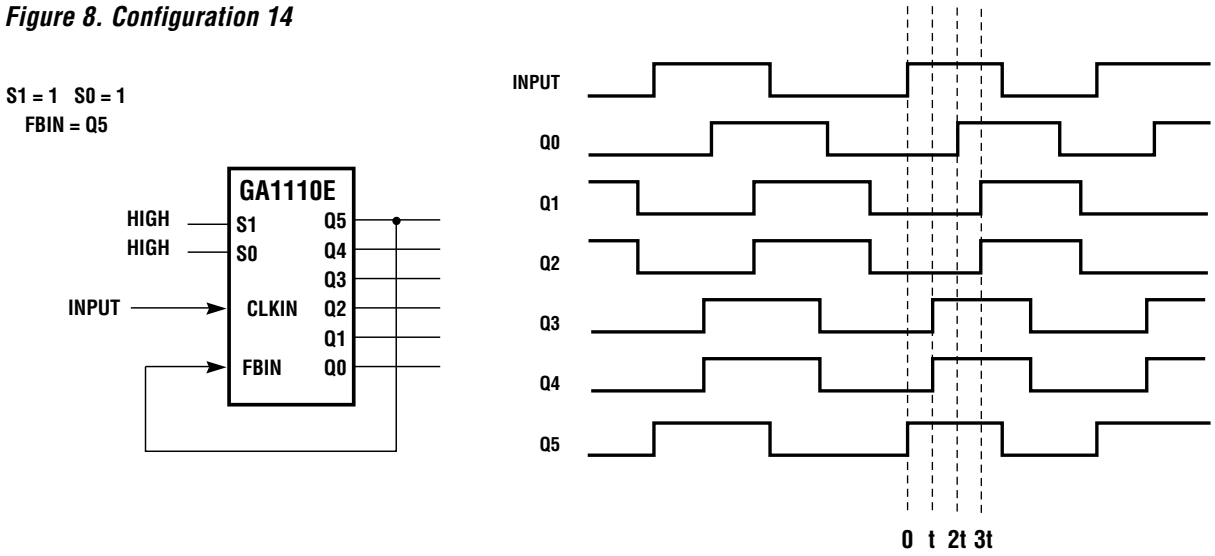


Figure 8. Configuration 14



SYSTEM TIMING PRODUCTS

Typical Applications

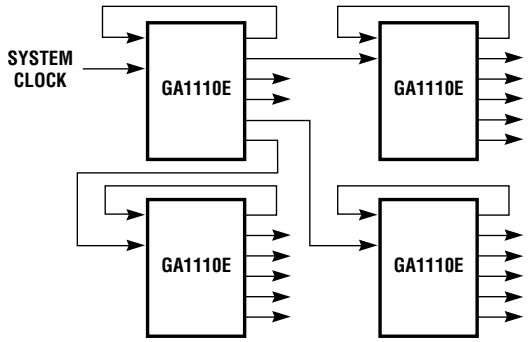
The GA1110E is designed to satisfy a wide range of system clocking requirements. The following are four of the most common clocking bottlenecks which can be alleviated using the GA1110E. These applications are illustrated in Figures 9A through 9D.

1) Low-Skew Clock Distribution / Clock Trees

The most basic bottleneck to clocking high-performance systems is generating multiple copies of a system clock, while maintaining low skew throughout the system.

- *The GA1110E guarantees low skew among all clocks in the system by controlling both the input-to-output delay and the skew among all outputs.*

Figure 9A. Low-Skew Clocks

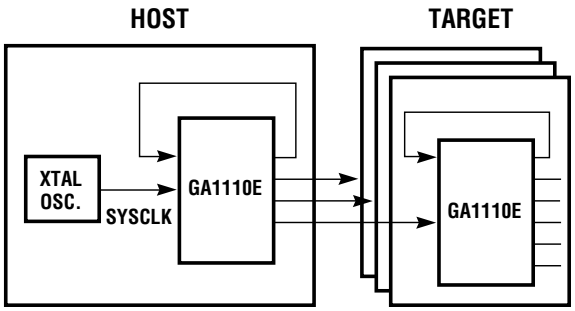


2) Board-to-Board Clock Synchronization

Many computing systems today consist of multiple boards and cards designed to run synchronously. The skew associated with routing clocks across a backplane presents a major hurdle to maximizing system performance.

- *The tightly controlled input/output delay of the GA1110E ensures all boards in the system are running synchronously.*
- *The phase-shift feature on the device outputs can be used to compensate for the differing physical distances between multiple cards in a system.*

Figure 9B. Board-to-Board Synchronization



Typical Applications (continued)

3) Leading and Lagging Edge Clock Generation

In synchronous or state machine designs where clocks must be sequential, or where metastability becomes a concern, tight edge placement of clock signals becomes a primary requirement.

- *The GA1110E, using its phase-control feature, can guarantee by design that clock signals are sequential in as little as 2.5 ns increments.*
- *This enables pipelined logic which is unbalanced to be clocked in different phases, alleviating setup/hold time requirements.*

4) Trace Delay / Loading Compensation

System designers often rely on various board layout techniques to compensate for signals driving different distances and/or loads.

- *The GA1110E can selectively "place" clock edges ahead or behind in 2.5 ns increments to compensate for severe mismatches.*
- *Because the output skew is tightly controlled, outputs of the same phase can be wired together to increase drive capability on heavily loaded clock signals.*

Figure 9C. Sequential Clock Signals

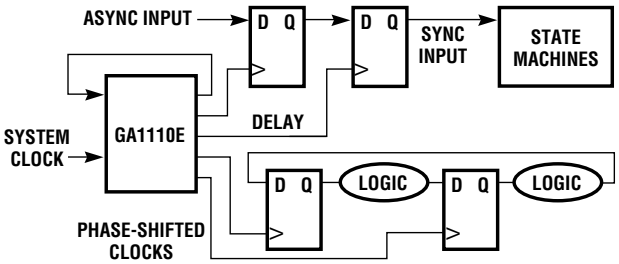
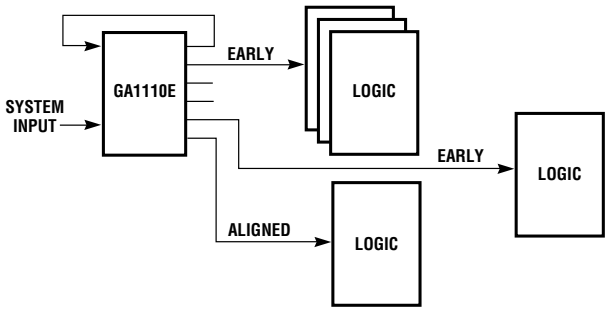
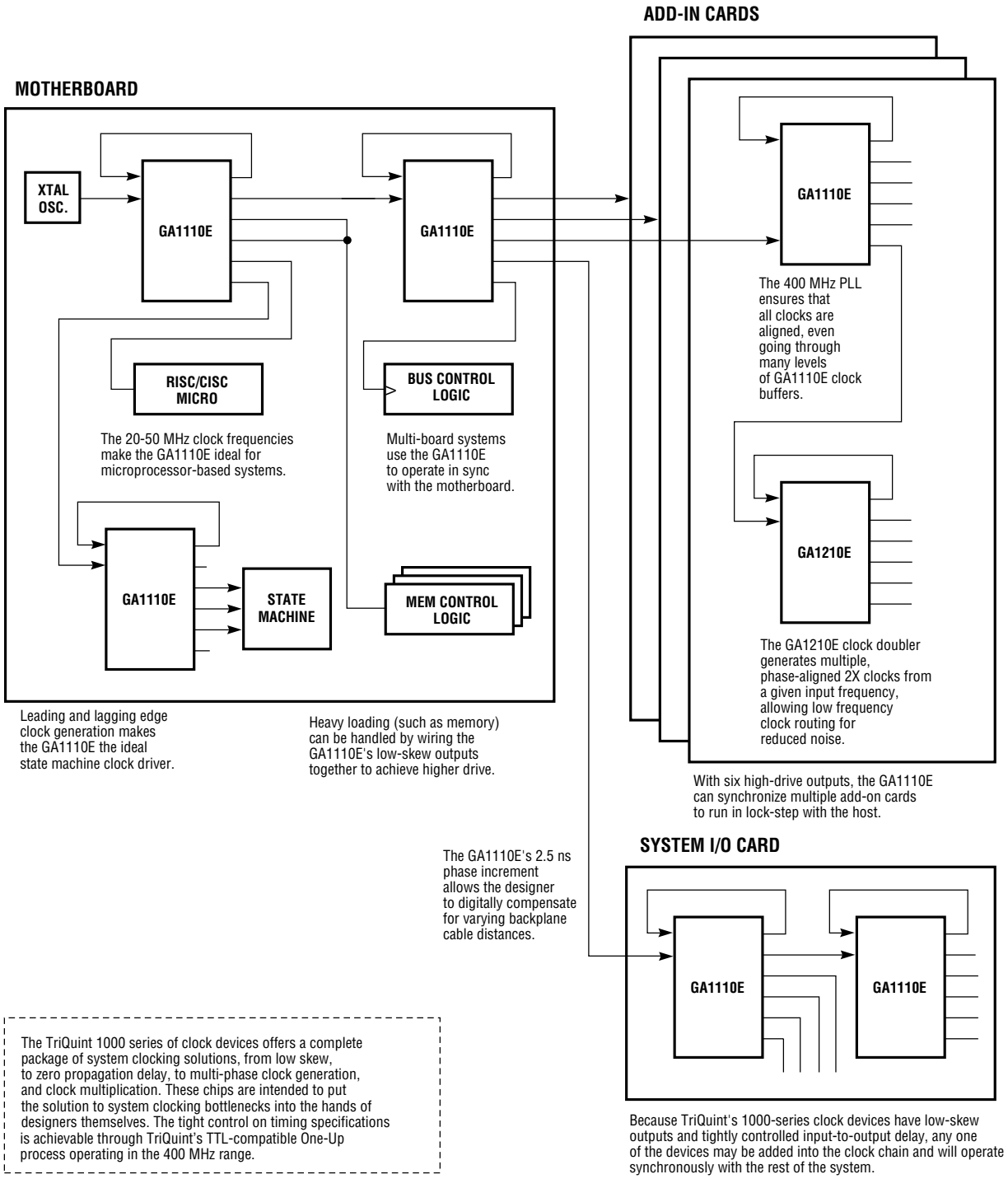


Figure 9D. Timing and Load Compensation



SYSTEM TIMING PRODUCTS

Figure 10. System Clocking Solutions



The TriQuint 1000 series of clock devices offers a complete package of system clocking solutions, from low skew, to zero propagation delay, to multi-phase clock generation, and clock multiplication. These chips are intended to put the solution to system clocking bottlenecks into the hands of designers themselves. The tight control on timing specifications is achievable through TriQuint's TTL-compatible One-Up process operating in the 400 MHz range.

Absolute Maximum Ratings

Storage temperature	–65 °C to +150 °C
Ambient temperature with power applied	–55 °C to +125 °C
Supply voltage to ground potential	–0.5 V to +7.0 V
DC input voltage	–0.5 V to +(V_{DD} + 0.5)
DC input current	–30 mA to +5 mA

DC Characteristics *(Supply voltage: +5 V ± 5% Ambient temp: 0 °C to +70 °C)*

Symbol	*Description*	*Test Conditions*	*Min*	*Limits [1] Typ*	*Max*	*Unit*
V_{OH}	Output HIGH voltage	V_{DD} = Min I_{OH}= –24 mA V_{IN}= V_{IH} or V_{IL}	2.4	3.55		V
V_{OL}	Output LOW voltage	V_{DD} = Min I_{OL} = 24 mA V_{IN}= V_{IH} or V_{IL}		0.23	0.5	V
V_{IH} [2]	Input HIGH level	Guaranteed input logical HIGH Voltage for all Inputs	2.0			V
V_{IL} [2]	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I_{IL}	Input LOW current	V_{DD} = Max V_{IN} = 0.40 V		–210	–400	µA
I_{IH}	Input HIGH current	V_{DD} = Max V_{IN} = 2.7 V		0	25	µA
I_I	Input HIGH current	V_{DD} = Max V_{IN} = 5.5 V		2	1000	µA
I_{SC} [3]	Output short-circuit current	V_{DD} = Max V_{OUT} = 0.5 V		–80		mA
I_{DD}	Power supply current	V_{DD} = Max		130	160	mA
V_I	Input clamp voltage	V_{DD} = Min I_{IN} = –18 mA		–0.62	–1.2	V
I_{OLD}	Dynamic switching	V_{DD} = Max V_{OLD} = 1.5 V		70		mA
I_{OHD}	current	V_{DD} = Max V_{OHD} = 1.5 V		–80		mA

Capacitance [4]

Symbol	*Description*	*Test Conditions*	*Min*	*Typ*	*Max*	*Unit*
C_{IN}	Input capacitance	V_{IN} = 2.0 V at f = 1 MHz		6		pF
C_{OUT}	Output capacitance	V_{OUT} = 2.0 V at f = 1 MHz		9		pF

Notes: 1. Typical limits are at V_{DD} = 5.0 V and T_A = 25 °C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. No more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} has been chosen to avoid test problems caused by tester ground degradation.
4. These parameters are not 100% tested, but are periodically sampled.

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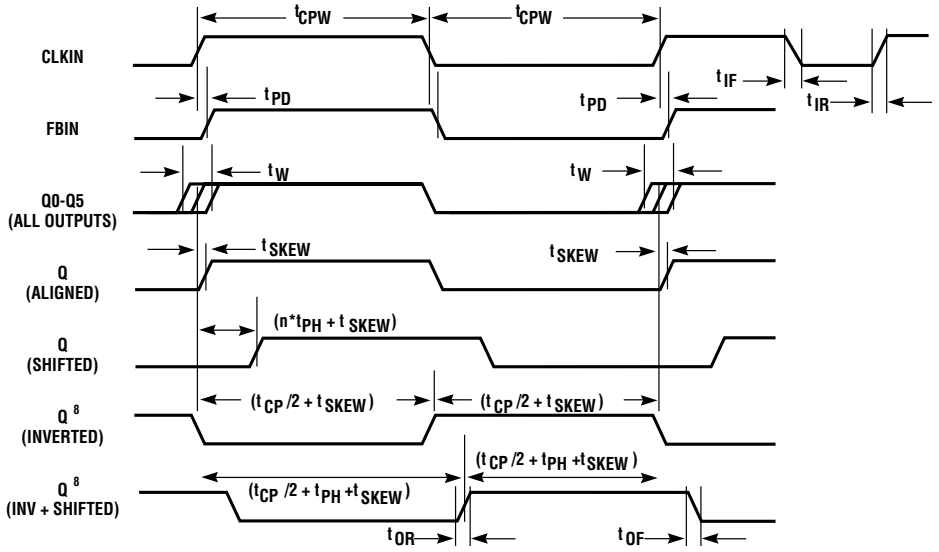
AC Characteristics *(Supply voltage: +5 V ± 5%; Ambient temp: 0 °C to 70 °C)*

Symbol	Description	–50 Min	–50 Typ	–50 Max	– 40 Min	– 40 Typ	– 40 Max	–33 Min	–33 Typ	–33 Max	–25 Min	–25 Typ	–25 Max	–20 Min	–20 Typ	–20 Max	Unit
F_{IN}	CLKIN frequency [1]	—	50	—	—	40	—	—	33	—	—	25	—	—	20	—	MHz
t_{CP}	CLKIN period	—	20	—	—	25	—	—	30	—	—	40	—	—	50	—	ns
t_{CPW}	CLKIN pulse width	5	10	—	6.25	12.5	—	7.5	15	—	10	20	—	12.5	25	—	ns
t_{IR},t_{IF}	Input rise/fall time (20 – 80%)	—	—	3.0	—	—	3.0	—	—	3.0	—	—	3.0	—	—	3.0	ns
t_{OR},t_{OF}	Output rise/fall time (80 – 20%)	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	—	1.0	3.0	ns
t_R	Output rise time (0.8 V to 2.0 V)	—	0.5	1.5	—	0.5	1.5	—	0.5	1.5	—	0.5	1.5	—	0.5	1.5	ns
t_{PD}	CLKIN ↑ to FBIN ↑ [2]	—	±250	±1000	—	±250	±1000	—	±250	±1000	—	±250	±1000	—	±250	±1000	ps
t_{SKEW}	Output Skew [3]	—	±250	±500	—	±250	±500	—	±250	±500	—	±250	± 500	—	±250	±500	ps
t_W	Output Window [4]	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	ns
t_{PH}	Phase-shift Increment [5]	2.5	2. 5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ns
t_{CYC}	Duty-cycle Variation [6]	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	ns
t_{SYNC}	Synchronization Time [7]	—	200	500	—	200	500	—	200	500	—	200	500	—	200	500	µs

Note: All AC specifications are measured with a 75 Ω transmission line load terminated with 75 Ω to 1.5 V. The skew specifications are guaranteed for equal loading at each output.

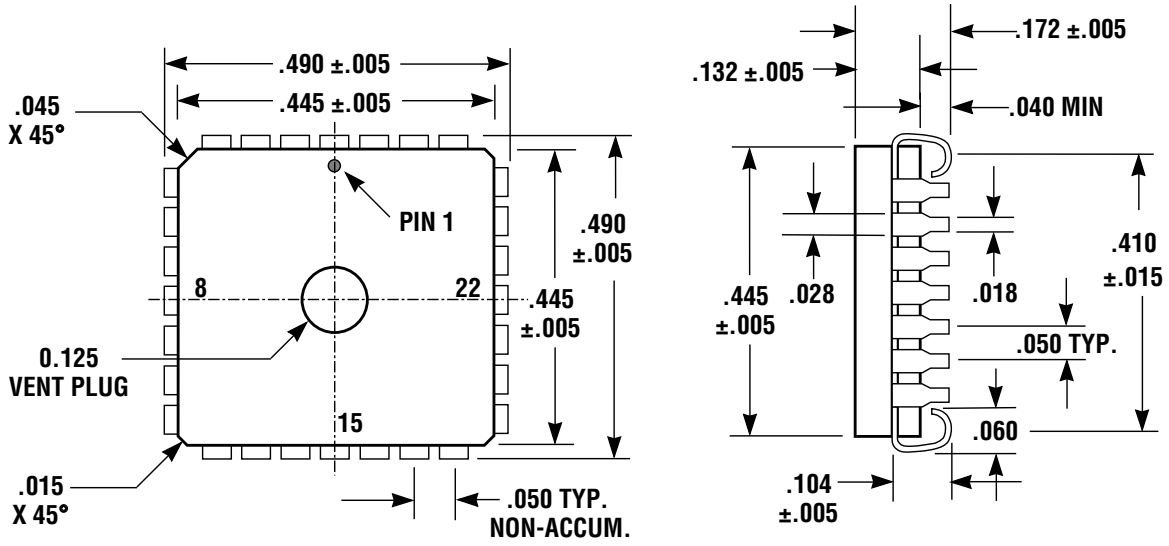
Figure 11. Switching Waveforms



Notes:
1. *The max, min range on CLKIN frequency is ± 5%.*
2. *The PLL maintains alignment of CLKIN and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50.*
3. *The output skew is measured from the middle of the output window. The maximum skew is guaranteed across all voltages and temperatures.*
4. *t_W specifies the width of the window in which all outputs will switch.*
5. *This increment is a digitally generated fraction of t_{CP} and will not vary with voltage or temperature The specifications for t_{PH} given in the table are for 50, 40, 33, 25, and 20 MHz operation, respectively.*
6. *This specification represents the deviation from 50/50 on the outputs; it is sampled periodically but is not guaranteed.*
7. *t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLKIN signal and a connection from one of the outputs to FBIN.*
8. *All specifications for inverted outputs apply to the rising edge only.*
9. *The device is AC tested only in the S0 = S1 = 0 mode.*

28-Pin MQuad J-Leaded Package Mechanical Specifications

(All dimensions are in inches)



28-Pin MQuad Pin Description

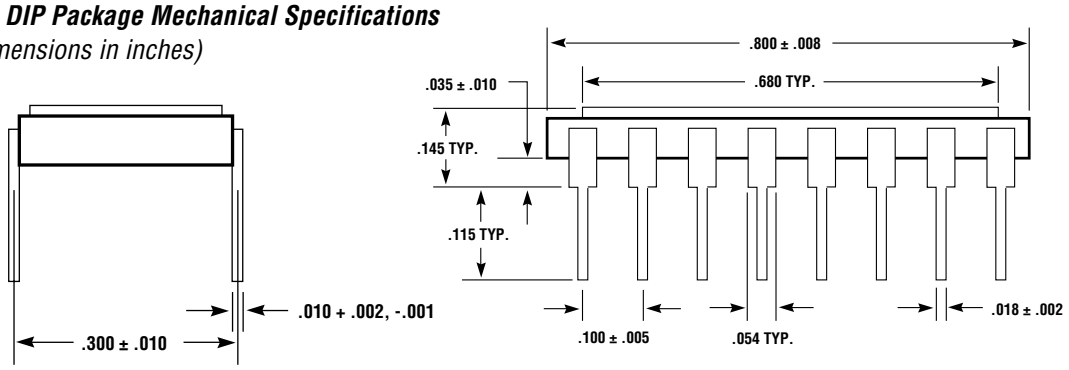
Pin #	*Pin Name*	*Description*	*I/O*
1	N/C	No Connect	—
2	GND	Ground	—
3	T0	Test 0	I [1]
4	N/C	No Connect	—
5	N/C	No Connect	—
6	S0	Select 0	I
7	S1	Select 1	I
8	N/C	No Connect	—
9	FBIN	Feedback In	I
10	CLKIN	System Clock	I
11	N/C	No Connect	—
12	N/C	No Connect	—
13	T1	Test 1	I [1]
14	GND	Ground	—

Pin #	*Pin Name*	*Description*	*I/O*
15	N/C	No Connect	—
16VDD	+5 V	—	
17	Q0	Output Clock 0	O
18	N/C	No Connect	—
19	N/C	No Connect	—
20	Q1	Output Clock 1	O
21	Q2	Output Clock 2	O
22	Q3	Output Clock 3	O
23	Q4	Output Clock 4	O
24	Q5	Output Clock 5	O
25	N/C	No Connect	—
26	N/C	No Connect	—
27	VDD	+5 V	—
28	VDD	+5 V	—

Note: 1. For normal operation, T0 is GND and T1 is V_{DD} or N/C (No Connect). For Test Mode, T0 is HIGH and T1 is Clock Pulse(s).

16-Pin DIP Package Mechanical Specifications

(All dimensions in inches)



16-Pin DIP Pin Description

Pin #	*Pin Name*	*Description*	*I/O*
1	GND	Ground	—
2	T0	Test 0	I [1]
3	S0	Select 0	I
4	S1	Select 1	I
5	FBIN	Feedback In	I
6	CLKIN	System Clock	I
7	T1	Test 1	I [1]
8	VDD	+5 V	—

Pin #	*Pin Name*	*Description*	*I/O*
9	GND	Ground	—
10	Q0	Output Clock 0	O
11	Q1	Output Clock 1	O
12	Q2	Output Clock 2	O
13	Q3	Output Clock 3	O
14	Q4	Output Clock 4	O
15	Q5	Output Clock 5	O
16	VDD	+5 V	—

Note: 1. For normal operation, T0 is GND and T1 is V_{DD} or N/C. For Test Mode, T0 is HIGH and T1 is Clock Pulse(s).

Ordering Information

To order, please specify as below shown:

GA1110E – nn p C

Input Frequency

20 – 20 MHz input
25 – 25 MHz input
33 – 33 MHz input
40 – 40 MHz input
50 – 50 MHz input

Package

S – 16-Pin DIP (side-brazed)
M – 28-Pin MQuad Surface-Mount

Temperature

C – Commercial

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel: (503) 615-9000**
Email: sales@tqs.com **Fax: (503) 615-8900**

For technical questions and additional information on specific applications:

Email: applications@tqs.com

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Revision 1.1.A November 1997