GSM31P256KB-I66 GSM31P512KB-I66 256KB / 512KB Modules COASt 3.1 Specification

Features

- For Intel Pentium CPU based systems
- Operates with clock speeds up to 66MHz
- Separate 5V and 3.3V power supplies
- Low cost and low profile card design using 160 gold plated leads
- Multiple ground pin and decopling capacitors provide maximum noise protection.
- Conform to Intel COASt 3.1 specification

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Functional Description

The GSM31P256KB-I66 and the GSM31P512KB-I66 are the secondary cache module designed for use with Intel Pentium CPU based system. These modules use GSI's Synchronous Burst SRAMs in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board.

Functional Description (cont'd)

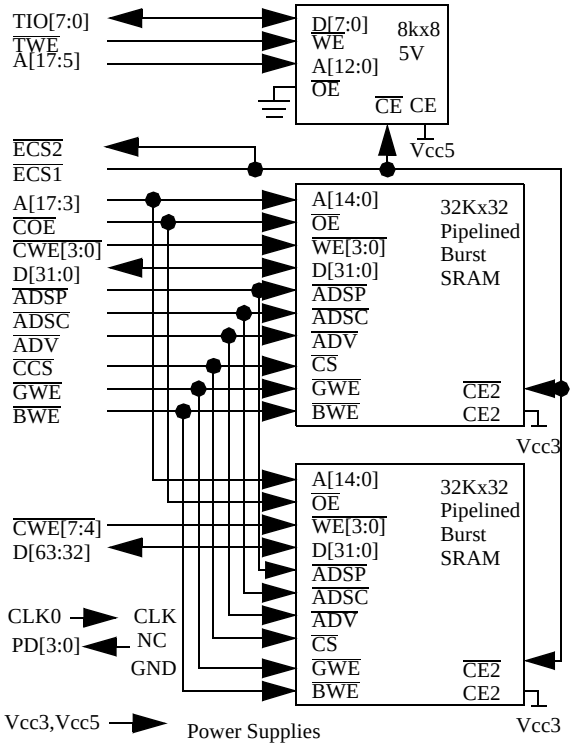
The GSM31P256KB-I66, and 256KB module, use GSI's GS81132Q 32KX32 synchronous burst SRAM and a single 5V 8Kx8 SRAM for the tag. The GSM14P512K-I66, a 512KB module, use GSI's GS82032Q 64KX32 synchronous burst SRAM and a single 5V 32Kx8 SRAM for the tag.

The 3.3V data RAM and the 5V tag RAM provide an exact interface between the module and PC chip set. Four presence detect bits (PD) allow the system to recognize the type of cache configuration present.

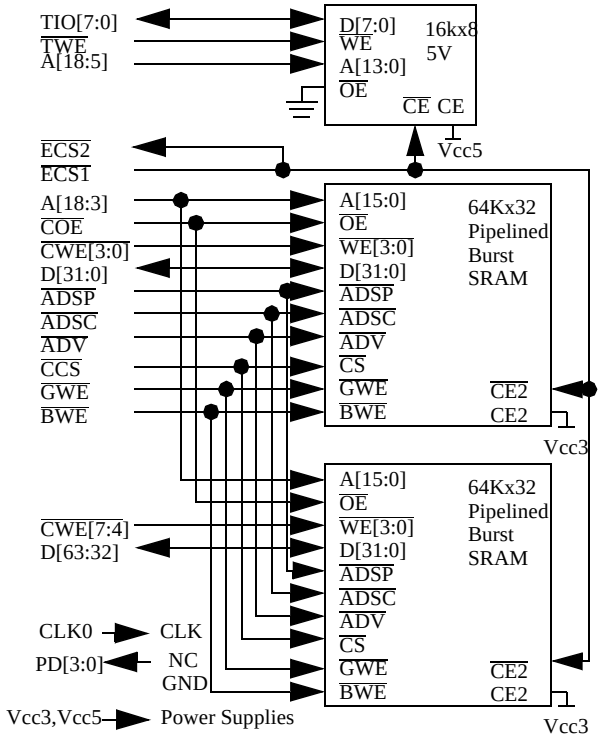
The low profile card edge package allows 160 signal leads to be placed on a module, measuring 4.35 inches long, a maximum of 0.310 inches thick and a maximum of 1.14 inches tall. This compact design allows the OEM to make better use of the real estate on the mother-board for added functions or smaller design for cost reduction.

All inputs and outputs and TTL compatible and operate from two separate 5V and 3.3V power supplies. The use of multiple ground pins and decoupling capacitors on-board reduces failure due to noise.

Functional Block Diagram - GSM31P256KB-I66



Functional Block Diagram - GSM31P512KB-I66



Pin Configuration

GND	81	1	GND
TIO1	82	2	TIO0
TIO7	83	3	TIO2
TIO5	84	4	TIO6
TIO3	85	5	TIO4
NC	86	6	NC
VCC5	87	7	VCC3
NC	88	8	$\overline{\text{TWE}}$
$\overline{\text{ADV}}$	89	9	$\overline{\text{ADSC}}$
GND	90	10	GND
$\overline{\text{COE}}$	91	11	$\overline{\text{CWE4}}$
$\overline{\text{CWE5}}$	92	12	$\overline{\text{CWE6}}$
$\overline{\text{CWE7}}$	93	13	$\overline{\text{CWE0}}$
$\overline{\text{CWE1}}$	94	14	$\overline{\text{CWE2}}$
VCC5	95	15	VCC3
$\overline{\text{CWE3}}$	96	16	$\overline{\text{CCS}}$
NC	97	17	$\overline{\text{GWE}}$
NC	98	18	$\overline{\text{BWE}}$
GND	99	19	GND
NC	100	20	A3
A4	101	21	A7
A6	102	22	A5
A8	103	23	A11
A10	104	24	A16
VCC5	105	25	VCC3
A17	106	26	A18[1]
GND	107	27	GND
A9	108	28	A12
A14	109	29	A13
A15	110	30	$\overline{\text{ADSP}}$
NC	111	31	$\overline{\text{ECS1}}$
PD0	112	32	$\overline{\text{ECS2}}$
PD2	113	33	PD1
NC	114	34	PD3
GND	115	35	GND
CLK0	116	36	NC
GND	117	37	GND
D63	118	38	D62
VCC5	119	39	VCC3
D61	120	40	D60
D59	121	41	D58
D57	122	42	D56
GND	123	43	GND
D55	124	44	D54
D53	125	45	D52
D51	126	46	D50
D49	127	47	D48
GND	128	48	GND
D47	129	49	D46
D45	130	50	D44
D43	131	51	D42
VCC5	132	52	VCC3
D41	133	53	D40
D39	134	54	D38
D37	135	55	D36
GND	136	56	GND
D35	137	57	D34
D33	138	58	D32
D31	139	59	D30
VCC5	140	60	VCC3
D29	141	61	D28
D27	142	62	D26
D25	143	63	D24
GND	144	64	GND
D23	145	65	D22
D21	146	66	D20
D19	147	67	D18
VCC5	148	68	VCC3
D17	149	69	D16
D15	150	70	D14
D13	151	71	D12
GND	152	72	GND
D11	153	73	D10
D9	154	74	D8
D7	155	75	D6
VCC5	156	76	VCC3
D5	157	77	D4
D3	158	78	D2
D1	159	79	D0
GND	160	80	GND

Pin Description

Pin Name	Type	Description
A[18:3]	I	Cache Address Inputs
$\overline{\text{ADSC}}$	I	Cache Address Status
$\overline{\text{ADSP}}$	I	Processor Address Status
$\overline{\text{ADV}}$	I	Burst Address Advance
$\overline{\text{BWE}}$	I	Byte Write Enable
$\overline{\text{CCS}}$	I	Chip Select
CLK0	I	System Clock
$\overline{\text{COE}}$	I	Cache Output Enable
$\overline{\text{CWE[7:0]}}$	I	Cache Write Enables
D[63:0]	I/O	Cache Data Input/Output
$\overline{\text{ECS[1:0]}}$	I	External Chip Select
GWE	I	Global Write Enable
PD[3:0]	O	Presence Detect Outputs
TIO[7:0]	I/O	Tag Inputs/Outputs
$\overline{\text{TWE}}$	I	Tag Write Enable
Vcc3	-	3.3V Power Supply
Vcc5	-	5V Power Supply
GND	-	Ground
NC	-	No Connect

Notes:
1. Pin 26, A18, is a no connect in the GSM14P256K-I66 version

Presence Detect Table

PD3	PD2	PD1	PD0	Device Indicated
NC	NC	NC	NC	No Module Present
NC	GND	NC	NC	GSM14P256K-I66
GND	NC	NC	NC	GSM14P512K-I66

Absolute Maximum Ratings

Parameter	*Symbol*	*Value*	*Unit*
Supply Voltage 3.3V Vcc Pins 5.0V Vcc Pins	 Vcc3 Vcc5	 -0.5 to +4.6 -0.5 to 6.0	 V V
Operating Temperature	Ta	0 to +70	^{o}C
Storage Temperature	Ts	-55 to +125	^{o}C

Recommended Operating Conditions

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply Voltage 3.3V Vcc Pins 5.0V Vcc Pins	 Vcc3 Vcc5	 3.135 4.75	 3.3 5.0	 3.6 5.25	 V V
Operating Temperature	Ta	0	-	+70	^{o}C
Input High Voltage	Vih	2.0	-	Vcc+0.3	^{o}C
Input Low Voltage	Vil	-0.3	-	0.8	

Capacitance

Parameter	*Symbol*	*Max*	*Unit*
Address Input Capacitance	CIN1	20	pF
Control Signal Input Capacitance	CIN2	10	pF
TAG Input Capacitance	CIN3	10	pF
Output Enable Capacitance	CIN4	15	pF
Data I/O Capacitance	CI/O	10	pF

Note: These parameters are guaranteed by design, but not tested.

DC Electrical Characteristics Over the Operating Range

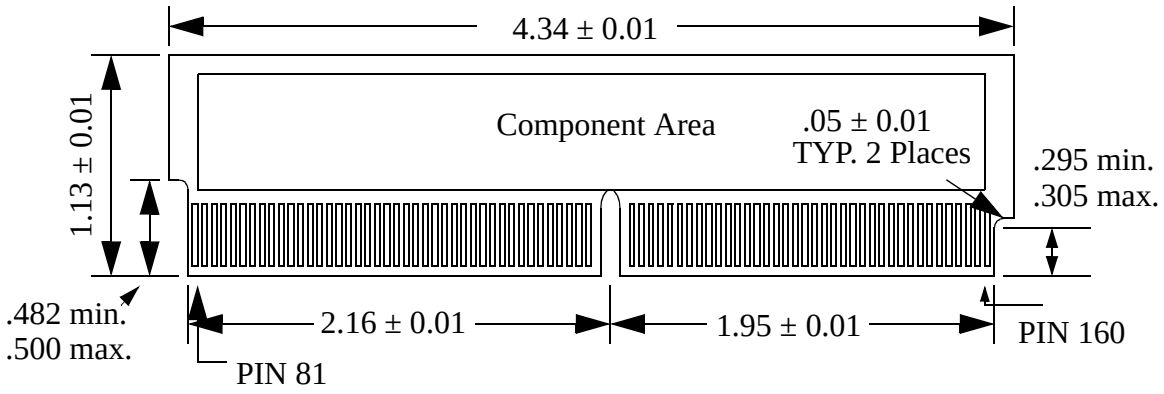
Parameter	*Test Condition*	*Symbol*	*Min*	*Max*	*Unit*
Input Leakage Current (Data & Control)	VIN=0 to Vcc3	ILI	-	± 20	uA
Output Leakage Current (Data & Control)	VOUT=0 to Vcc3, $\overline{CS}$≥VIH	IOUT	-	± 20	uA
Output High Voltage	IOH=-4.0mA	VOH	2.4	-	V
Output Low Voltage	IOL=8.0mA	VOL	-	0.4	V
Operating Supply Current, 5V Power	Vcc5=Max, IOUT=0mA, f=Max	Icc5	-	180	mA
Operating Supply Current, 3.3V Power	Vcc3=Max, IOUT=0mA, f=Max	Icc3	-	500	mA
AC Standby Supply Current, 3.3V Power	Vcc=Max, $\overline{CS}$≥VIH, f=max	ISB3	-	80	mA
Full CMOS Standby Current	Vcc=Max, $\overline{CS}$≥Vcc3-0.2, f=0MHz, VIN>Vcc3-0.2 or VIN<0.2	ISB31	-	40	mA

Ordering Information

Part Number	Cache Size	Speed
GSM31P256KB-I66	256KB	66MHz
GSM31P512KB-I66	512KB	66MHz

Package Dimension

Front View



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