10 Gbit/s AGC Amplifier GD19902

Preliminary

General Description

The GD19902 device is an amplifier designed for Automatic Gain Control (AGC), with high input overload, high gain, intended for use in high bandwidth applications such as 10 Gbit/s STM-64/ OC-192 receiver front-end.

GD19902 provides on chip peak detect circuitry as well as monitors on the output DC levels for balancing the outputs.

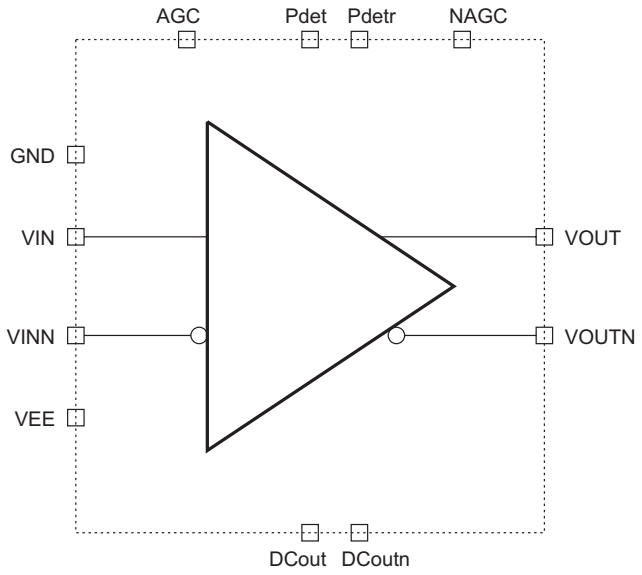
Gain is controlled from -3 dB to +20 dB through the AGC input.

The differential inputs can be used with a single-ended as well as a true differential input signal.

GD19902 is DC coupled.

On-chip 50 Ω termination of the input and output signals reduces the need for external components.

Together with a 10 Gbit/s CDR (GD16544) error free operation is obtained with < 2 × 8 mV_{PP} input signal.



Features

- Gain: 20 dB.
- High output: 1.0 $V_{PP.}$
- Output peak-peak monitor.
- Single power supply: -8 V.
- No external choke required.
- Bandwidth: 8 GHz (-3 dB), typical.
- Power dissipation: 2.8 W, typical.
- Output DC level monitors.

Applications

- Tele Communication transmission systems:
  - SDH STM-64
  - SONET OC-192
- WDM applications.
- 10 Gbit optical receivers.

Functionality

The typical application diagram for GD19902 is shown in Figure 1.

The GD19902 can be driven with a single ended or a differential input. In the case of single ended input, the differential output swing is halved, and the other input port must be AC shorted to GND. The inputs can be DC coupled, but then the applied circuit must not alter the quiescent input voltage. The outputs can be DC coupled, but then the DC level will be reduced from –1.4 V to –0.7 V.

The amplifier gain is controlled through the pins AGC and NAGC. These are *not* differential pins. The AGC pin is used for variable gain, and the NAGC pin for fixed maximum gain (if connected to GND). The two pins must *not* be connected simultaneously. If the two pins are both left open, maximum gain is also achieved, even though this setting is not recommended.

The gain is fixed, when a fixed voltage is applied on the AGC pin as illustrated in Figure 2. The maximum output is clamped to approximately 1.2 V_{PP}.

An external AGC circuit can be applied to the AGC pin as required in the specific application. The Pdet output varies with respect to the output peak-to-peak swing according to Figure 3 shown below. The Pdetr output accommodates for variations in the Pdet output caused by power supply and case temperature drift. The datasheet for the evaluation board GD99902 includes schematic for a suggested AGC circuit.

To keep the DC levels of the outputs balanced, the GD19902 features internal DC level monitors for the output pins. An external feedback circuit from pin DCout and DCoutn back to one of the inputs (through a bias T) will balance out any drift in the output DC levels. This feature serves two purposes. Primarily in the case of DC coupled outputs, the DC levels must be balanced at the input of the following DeMUX circuit (e.g. GD16544). Secondly, the output buffer transistors should be kept at a fixed operating point. The datasheet for the evaluation board GD99902 includes schematic for a suggested DC nulling circuit.

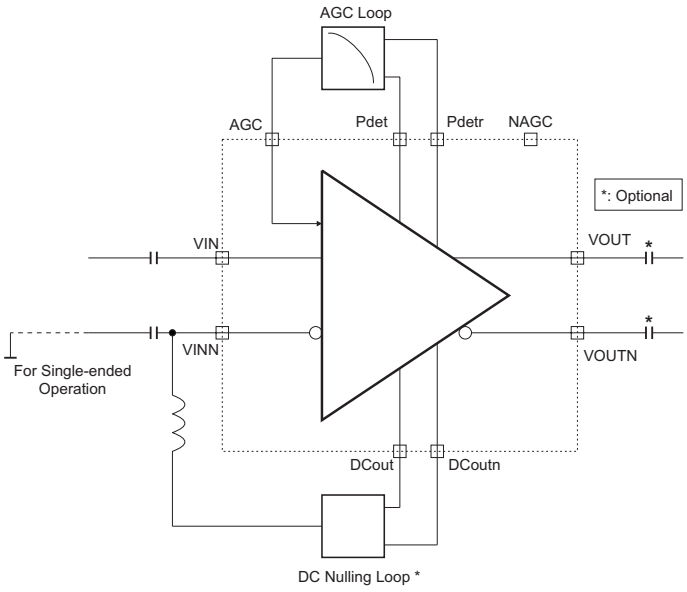


Figure 1. *Application Diagram*

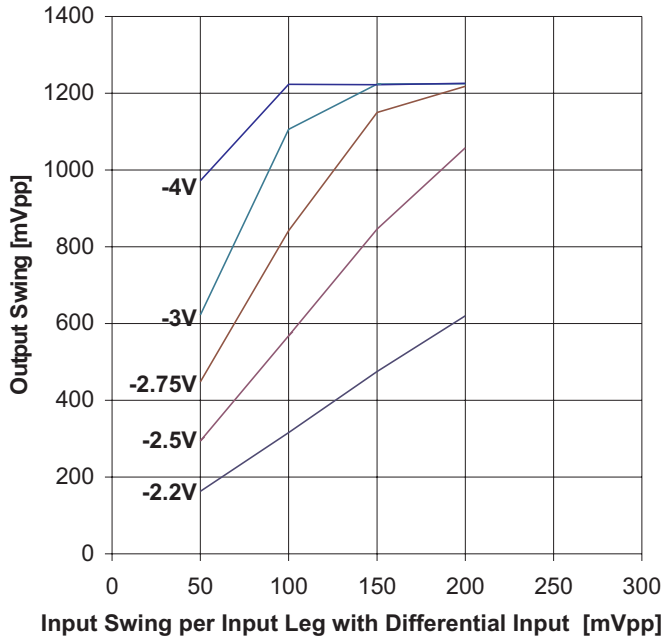


Figure 2. *Gain characteristics for fixed gain operation. Typical*

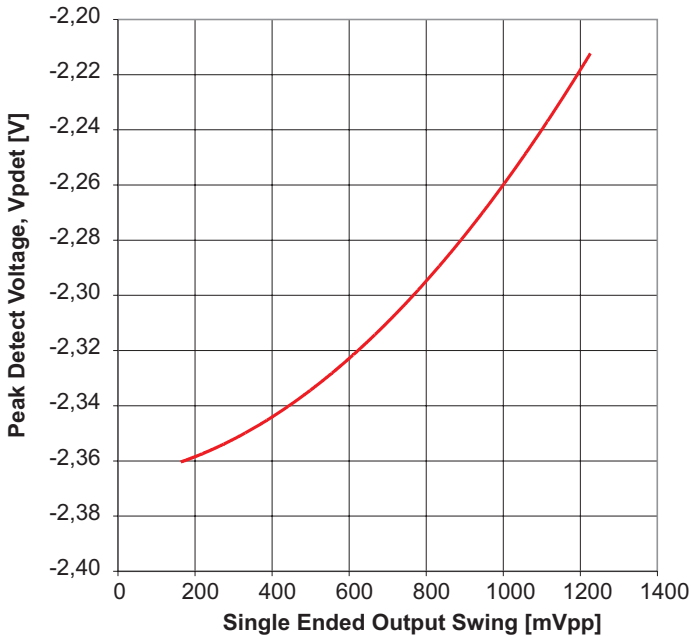


Figure 3. *Peak detect output vs. output swing. -4.0 V < V_{AGC} < -2.2 V. Typical*

Application

The GD19902 can be used with the GD19906 Transimpedance Amplifier in conjunction with other GIGA products as shown in the figure below – composing a full 10 Gbit/s receiver front-end.

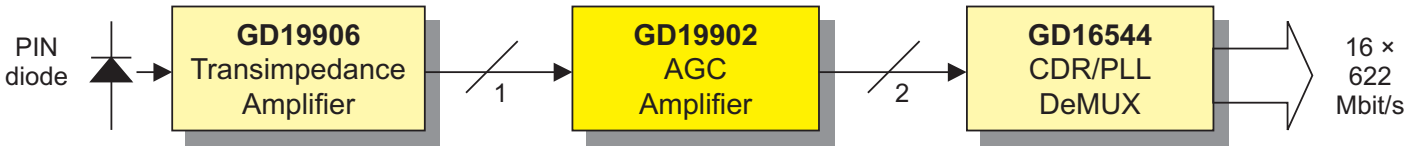


Figure 4. *Building blocks for a 10 Gbit/s reception system.*

The GD19906 device converts and pre-amplifies the current from the PIN diode, which is delivered to the AGC amplifier GD19902 single-ended. This device produces a differential signal suitable for driving the GD16544 DeMUX. The 16 demultiplexed data signals (and clock) available at the DeMUX output can be fed to a system ASIC. If required, a second level demultiplexer (GD16334) can be added for further reduction of the signal speeds. A set of four synchronized GD16334 demultiplexers will bring the original 10 Gbit/s signal down to 78 Mbit/s.

Please see separate data sheets for the TIA amplifier and the DeMUX devices.

GIGA offers corresponding building blocks for the transmit functions (see GD19901, 19903, and GD16555).

The required optical input power in the set-up shown in Figure 4 can be estimated as follows. The current generated by the PIN diode is given as Id = Pd / r, and the voltage swing after the TIA as VTIA = Id × RTIA. The GD19902 typically requires 50 mV_{PP} at the input, the GD19906 has a typical transimpedance gain of 500 Ω, and assuming a PIN diode responsivity of 1 A/W, we get:

VTIA = 50 mV
Id = VTIA/RTIA = 50 mV / 500 Ω = 0.1 mA
Pd = Id × r = 0.1 mA × 1 A/W = 0.1 mW

Assuming an optical non-return-to-zero (NRZ) signal with 50 % duty cycle between one's and zero's, this corresponds to an optical average power of:

Popt = Pd × 50 % = 0.1 mW × 0.5 = 0.5 mW or Popt = 10 × log10(0.05 mW/1 mW) = -13 dBm.

At the output of the GD19902 the each leg of the differential signal will have an amplitude swing of:

Vout = VTIA × G = 50 mV × 10^(20 dB/20) = 500 mV (single-ended) or 1000 mV (differential).

This calculation does not include noise generated at the optical PIN diode nor in the TIA amplifier.

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
VIN, VINN	27, 25	AC	Data Input, differential 10 Gbit/s. DC coupled, see Figure 1.
VOUT, VOUTN	59, 61	AC	Data Output, differential 10 Gbit/s. DC coupled, see Figure 1.
Pdet	3	DC	Peak Detect Output.
Pdetr	49	DC	Peak Detect Reference Level Output.
AGC	16	DC	AGC Control Line Input.
NAGC	36	DC	Maximum Gain Input.
GND	1, 4, 9, 14, 19, 20, 21, 22, 23, 24, 26, 28, 29, 30, 31, 32, 33, 34, 38, 43, 48, 51, 52, 53, 54, 55, 56, 57, 58, 60, 62, 63, 64, 65, 66, 67, 68	PWR	Ground.
VEE	17, 18, 35	PWR	Negative supply voltage.
DCoutn, DCout	5, 47	DC	Output DC levels.
NC	2, 6, 7, 8, 10, 11, 12, 13, 15, 37, 39, 40, 41, 42, 44, 45, 46, 50		Not Connected.

Package Pinout

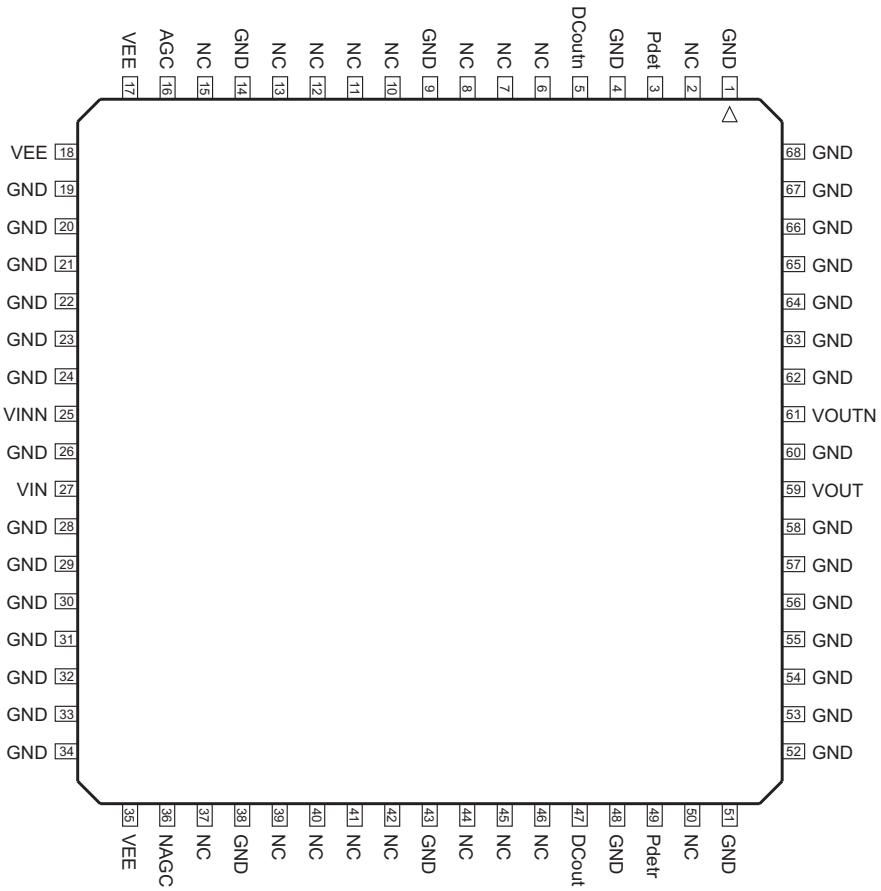


Figure 5. *Package 68 pin MLC, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to GND.
All currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
VEE	Negative Supply		-9		GND	V
VIN,VINN	Input Voltage		-2.5		0.5	V
VOUT, VOUTN	Output Voltage				1.75	V_{PP}
AGC	AGC Voltage Level		-4.0		0.5	V
NAGC	NAGC Voltage Level		-4.0		0	V
T_0	Operating Temperature	Case	0		70	°C
T_S	Storage Temperature		-65		125	°C

Precautions

Class 1 ESD

- Output: 500 V; Input: 100 V

DC Characteristics

T_{CASE} = 0 °C to 70 °C, VEE = -8.0 V ±5 %.
All voltages in the table are referred to GND.
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
VEE	Negative Supply		-8.4	-8.0	-7.6	V
IEE	Negative Supply Current		-300	-350	-375	mA
P_{DISS}	Power Dissipation			2.5	3.15	W
$V_{VIN,VINN}$	Quiescent Input Voltage			-0.85		V
$V_{VOUT,VOUTN}$	Quiescent Output Voltage	AC coupled outputs		-1.4		V
$V_{DCout, DCoutn}$	Output DC Levels	AC coupled outputs		-1.4		V

AC Characteristics

T_{CASE} = 0 °C to 70 °C, VEE = -8.0 V ±5 %.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
f_{3dB}	Bandwidth		7.5	10.0		GHz
$V_{VOUT,VOUTN}$	Output Data Amplitude			0.5	1.2	V_{PP}
Gmax	Maximum Gain		18	20	22	dB
Gmin	Minimum Gain				-3	dB
T_{RISE}	Rise Time	20 - 80 %		40		ps
T_{FALL}	Fall Time	20 - 80 %		44		ps
V_{VIN}, V_{VINN}	Input Data Amplitude			0.05	1.250	V_{PP}
S11	0 - 6 GHz 6 - 10 GHz			-7 -5		dB dB
S12	0 - 6 GHz 6 - 10 GHz			-7 -5		dB dB

Package Outline

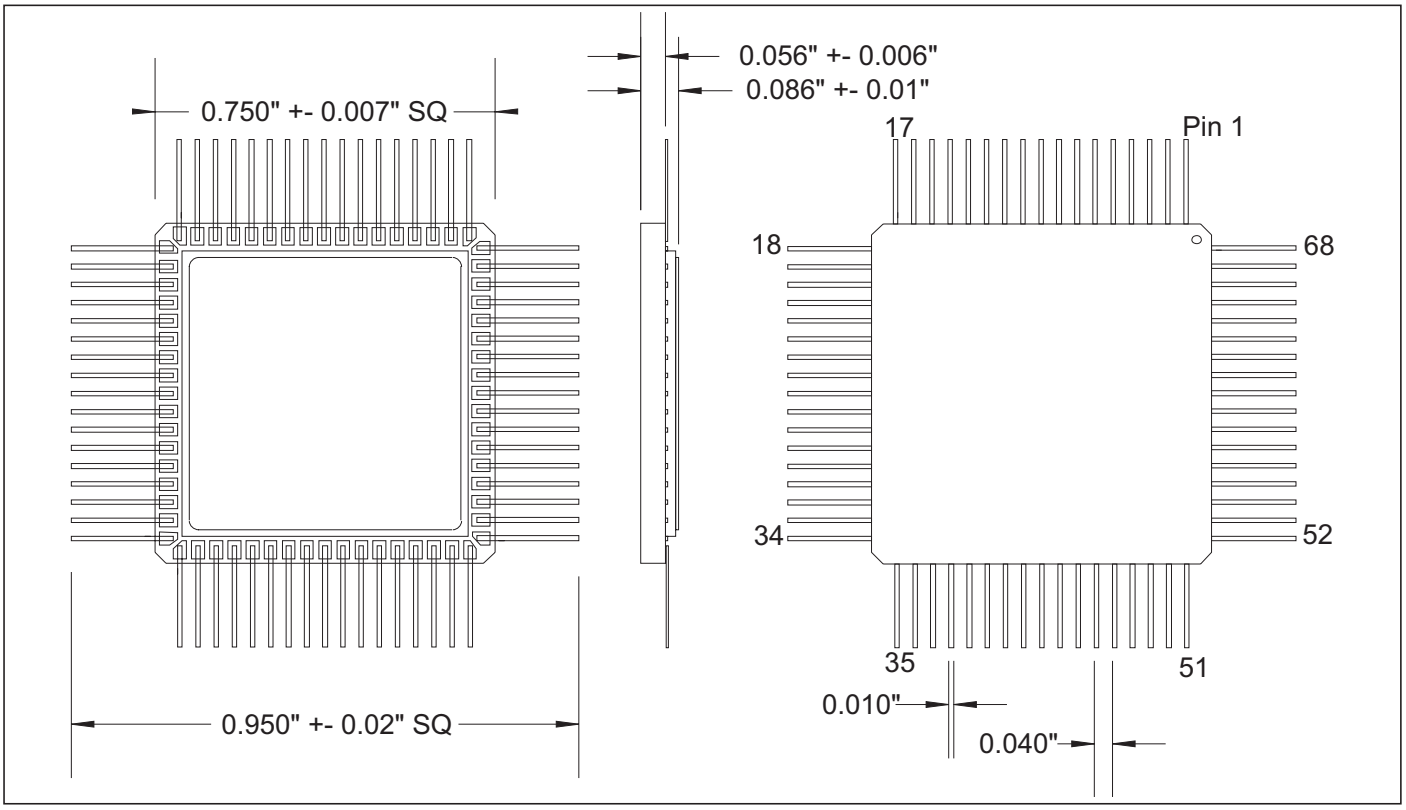


Figure 6. *Package 68 pin MLC, Straight Leads. All dimensions are in inch.*

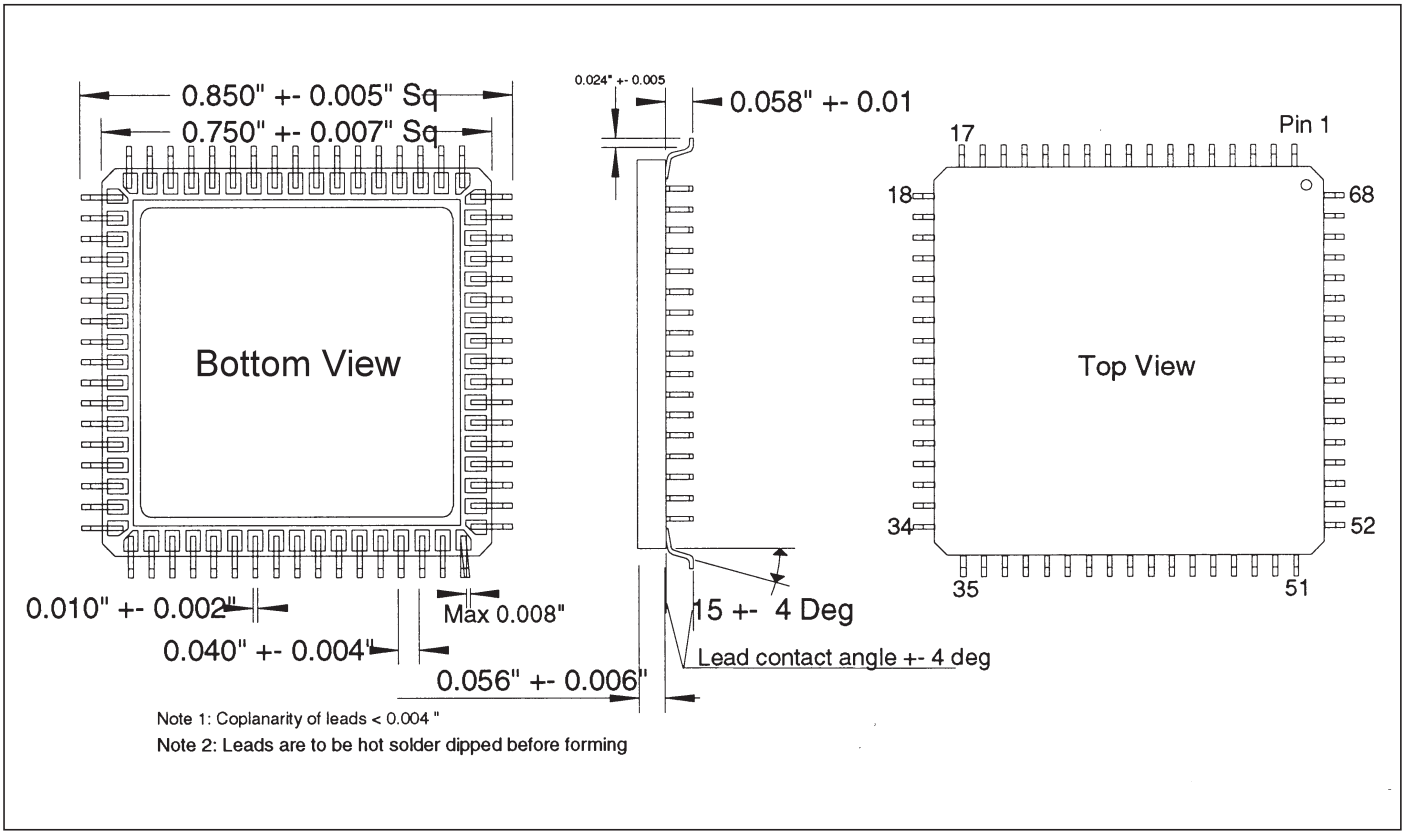


Figure 7. *Package 68 pin MLC, Gullwings Leads. All dimensions are in inch.*

References

Data Sheet for: GD99902, GD19906, GD16544 and GD16555B (latest revision)

Device Marking

Figure 8. *Device Marking. Top View.*

Ordering Information

Please order as specified below:

Product Name:	Package Type:	Case Temperature Range:	Options:
GD19902-68AB	**68 pin Straight Leads,** Multi Layer Ceramic	0..70 °C	
GD19902-68BA	**68 pin Gull wings Leads**, Multi Layer Ceramic	0..70 °C	

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