PRELIMINARY

CY7C1346A/GVT7164D36

64K x 36 Synchronous Pipelined Burst SRAM

Features

- **Fast access times: 3.5, 3.8, and 4.0 ns**
- **Fast clock speed: 166, 150, 133, and 117 MHz**
- **Provide high-performance 3-1-1-1 access rate**
- **Fast $\overline{OE}$ access times: 3.5 ns and 3.8 ns**
- **Optimal for depth expansion (one cycle chip deselect to eliminate bus contention)**
- **3.3V –5% and +10% power supply**
- **Separate isolated output buffer supply compatible with 3.3V and 2.5V I/O (V_{CCQ}): 2.375V to 3.6V**
- **5V tolerant inputs except I/Os**
- **Clamp diodes to V_{SSQ} at all inputs and outputs**
- **Common data inputs and data outputs**
- **Byte Write Enable and Global Write control**
- **Three chip enables for depth expansion and address pipeline**
- **Address, data and control registers**
- **Internally self-timed Write Cycle**
- **Burst control pins (interleaved or linear burst sequence)**
- **Automatic power-down for portable applications**
- **High-density, high-speed packages**

Functional Description

The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1346A/GVT7164D36 SRAM integrates 65,536x36 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ($\overline{CE}$), depth-expansion Chip Enables ($\overline{CE2}$ and CE2), Burst Control inputs ($\overline{ADSC}$, $\overline{ADSP}$, and $\overline{ADV}$), Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, and $\overline{BWE}$), and Global Write ($\overline{GW}$).

Asynchronous inputs include the Output Enable ($\overline{OE}$), Burst Mode Control (MODE), and sleep mode control (ZZ). The data outputs (Q), enabled by $\overline{OE}$, are also asynchronous.

Addresses and chip enables are registered with either address status processor ($\overline{ADSP}$) or Address Status Controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance pin ($\overline{ADV}$).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed Write cycle. Write cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. $\overline{BW1}$ controls DQ1–DQ8 and DQP1. $\overline{BW2}$ controls DQ9–DQ16 and DQP2. $\overline{BW3}$ controls DQ17–DQ24 and DQP3. $\overline{BW4}$ controls DQ25–DQ32 and DQP4. $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, and $\overline{BW4}$ can be active only with $\overline{BWE}$ being LOW. $\overline{GW}$ being LOW causes all bytes to be written.

The CY7C1346A/GVT7164D36 operates from a +3.3V power supply. All inputs and outputs are TTL-compatible. The device is ideally suited for 486, Pentium®, 680x0, and PowerPC™ systems and for systems that are benefited from a wide synchronous data bus.

Selection Guide

	7C1346A-166 7164D36-3	7C1346A-150 7164D36-4	7C1346A-133 7164D36-5	7C1346A1-117 7164D36-6
Maximum Access Time (ns)	3.5	3.8	4.0	4.0
Maximum Operating Current (mA)	425	400	375	350
Maximum CMOS Standby Current (mA)	2	2	2	2

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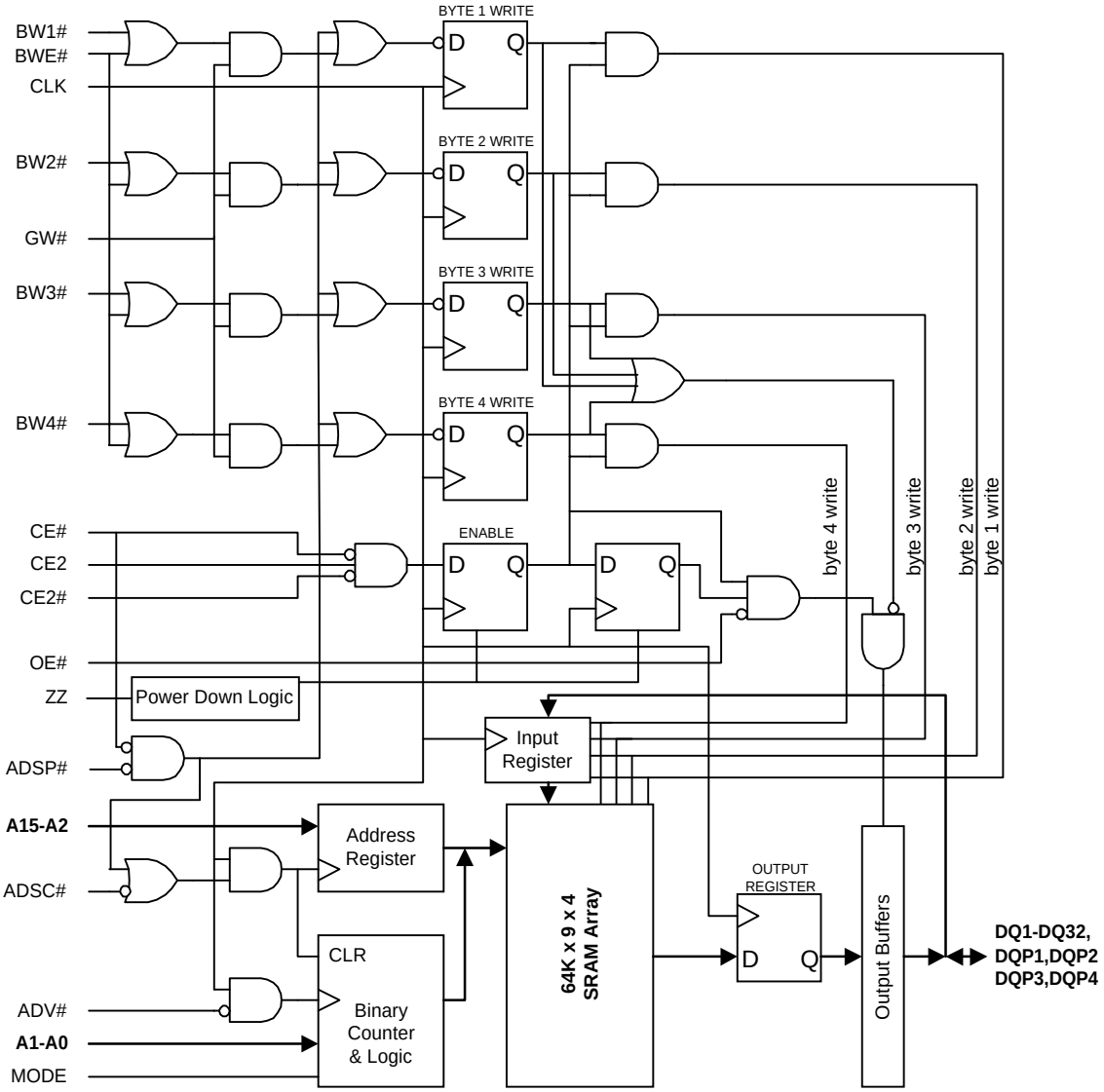
PowerPC is a trademark of IBM Corporation.

64K x 36 (CY7C1344A/GVT7164B36) Functional Block Diagram[1]

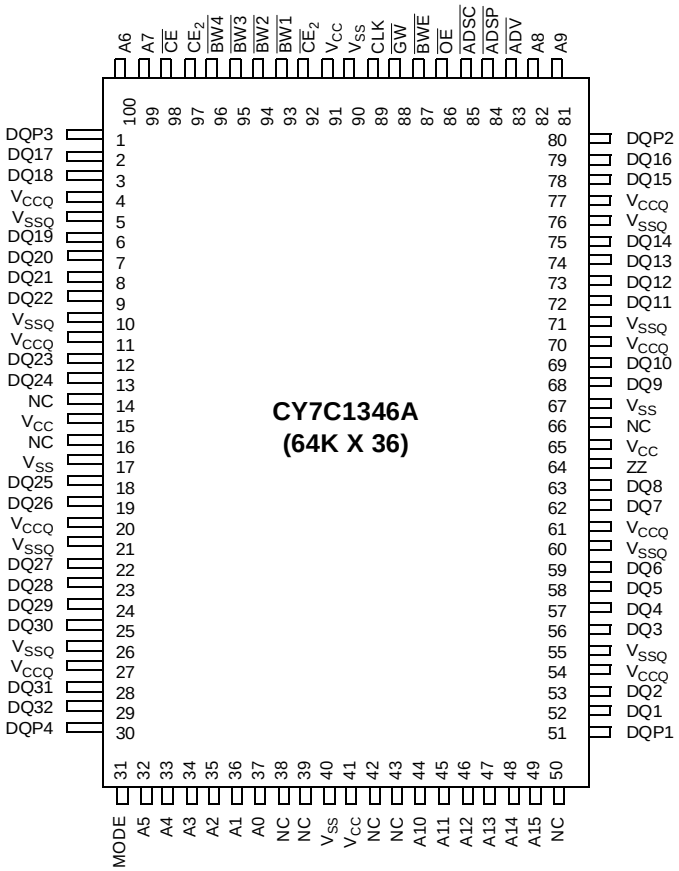


Note:

1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions, and timing diagrams for detailed information.

Pin Configurations

100-Pin TQFP
Top View



Pin Descriptions

Pin Name	Type	Description
A0–A15	Input-Synchronous	Addresses: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input-Synchronous	Byte Write: A byte write is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1–DQ8 and DQP1. $\overline{BW2}$ controls DQ9–DQ16 and DQP2. $\overline{BW3}$ controls DQ17–DQ24 and DQP3. $\overline{BW4}$ controls DQ25–DQ32 and DQP4. Data I/O are high impedance if either of these inputs are LOW, conditioned by $\overline{BWE}$ being LOW.
$\overline{BWE}$	Input-Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the set-up and hold times around the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	Global Write: This active LOW input allows a full 36-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the set-up and hold times around the rising edge of CLK.
CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.
$\overline{CE}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device and to gate $\overline{ADSP}$.

Pin Descriptions (continued)

Pin Name	Type	Description
$\overline{CE2}$	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.
CE2	Input-Synchronous	Chip Enable: This active HIGH input is used to enable the device.
$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
$\overline{ADV}$	Input-Synchronous	Address Advance: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
$\overline{ADSP}$	Input-Synchronous	Address Status Processor: This active LOW input, along with $\overline{CE}$ being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
$\overline{ADSC}$	Input-Synchronous	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
MODE	Input-Static	Mode: This input selects the burst sequence. A LOW on this pin selects Linear Burst. A NC or HIGH on this pin selects Interleaved Burst.
ZZ	Input-Asynchronous	Snooze: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (No Connect).
DQ1–DQ32	Input/Output	Data Inputs/Outputs: First Byte is DQ1–DQ8. Second Byte is DQ9–DQ16. Third Byte is DQ17–DQ24. Fourth Byte is DQ25–DQ32. Input data must meet set-up and hold times around the rising edge of CLK.
DQP1, DQP2, DQP3, DQP4	Input/Output	Parity Inputs/Outputs: DQP1 is parity bit for DQ1–DQ8 and DQP2 is parity bit for DQ9–DQ16. DQP3 is parity bit for DQ17–DQ24 and DQP4 is parity bit for DQ25–DQ32.
V_{CC}	Supply	Power Supply: +3.3V –5% and +10%.
V_{SS}	Ground	Ground: GND.
V_{CCQ}	I/O Supply	Output Buffer Supply: +2.375 to 3.6V.
V_{SSQ}	I/O Ground	Output Buffer Ground: GND.
NC	-	No Connect: These signals are not internally connected.

Burst Address Table (MODE = NC/V_{CC})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

Burst Address Table (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

Truth Table[2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Partial Truth Table for Read/Write

FUNCTION	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE one byte	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

Notes:

2. X means “Don’t Care.” H means logic HIGH. L means logic LOW. $\overline{WRITE}$ = L means [$\overline{BWE}$ + $\overline{BW1}$*$\overline{BW2}$*$\overline{BW3}$*$\overline{BW4}$]*$\overline{GW}$ equals LOW. $\overline{WRITE}$ = H means [$\overline{BWE}$ + $\overline{BW1}$*$\overline{BW2}$*$\overline{BW3}$*$\overline{BW4}$]*$\overline{GW}$ equals HIGH.
3. $\overline{BW1}$ enables write to DQ1–DQ8 and DQP1. $\overline{BW2}$ enables write to DQ9–DQ16 and DQP2. $\overline{BW3}$ enables write to DQ17–DQ24 and DQP3. $\overline{BW4}$ enables write to DQ25–DQ32 and DQP4.
4. All inputs except $\overline{OE}$ must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
5. Suspending burst generates wait cycle.
6. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required set-up time plus High-Z time for $\overline{OE}$ and staying HIGH throughout the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW along with chip being selected always initiates a READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting $\overline{WRITE}$ LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines only, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS} ..... –0.5V to +4.6V

V_{IN}..... –0.5V to +6V

Storage Temperature (plastic).....–55°C to +150°

Junction Temperature .....+150°

Power Dissipation 1.6W

Short Circuit Output Current ..... 100 mA

Operating Range

Range	Ambient Temperature[9]	V_{CC}
Com'l	0°C to +70°C	3.3V –5%/+10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IH}	Input High (Logic 1) Voltage[10, 11]		2.0	V_{CCQ}+0.3	V
V_{II}	Input Low (Logic 0) Voltage[10, 11]		–0.3	0.8	V
IL_I	Input Leakage Current[12]	0V ≤ V_{IN} ≤ V_{CC}	–2	2	µA
IL_O	Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	–2	2	µA
V_{OH}	Output High Voltage[10, 13]	I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output Low Voltage[10, 13]	I_{OL} = 8.0 mA		0.4	V
V_{CC}	Supply Voltage[10]		3.135	3.6	V
V_{CCQ}	I/O Supply		2.375	3.6	V

Parameter	Description	Conditions	Typ.	-3 166 MHz	-4 150 MHz	-5 133 MHz	-6 117 MHz	Unit
I_{CC}	Power Supply Current: Operating[14, 15, 16]	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ t_{KC} Min.; V_{CC} = Max.; outputs open	300	425	400	375	350	mA
I_{SB2}	CMOS Standby[15, 16]	Device deselected; V_{CC} = Max.; all inputs ≤ V_{SS} + 0.2 or ≥ V_{CC} – 0.2; all inputs static; CLK frequency = 0	1	2	2	2	2	mA
I_{SB3}	TTL Standby[15, 16]	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; V_{CC} = Max.; CLK frequency = 0	4	10	10	10	10	mA
I_{SB4}	Clock Running[15, 16]	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; V_{CC} = Max.; CLK cycle time ≥ t_{KC} Min.	80	130	130	130	130	mA

Thermal Consideration

Parameter	Description	Conditions	TQFP Typ.	Unit
Θ_{JA}	Thermal Resistance - Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch 4-layer PCB	25	°C/W
Θ_{JC}	Thermal Resistance - Junction to Case		9	°C/W

Notes:

9. T_A is the case temperature.
10. All voltages referenced to V_{SS} (GND).
11. Overshoot: V_{IH} ≤ +6.0V for t ≤ t_{KC}/2.
    Undershoot: V_{IL} ≤ –2.0V for t ≤ t_{KC}/2.
12. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±30 µA.
13. AC I/O curves are available upon request.
14. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
15. "Device Deselected" means the device is in Power-Down mode as defined in the truth table. "Device Selected" means the device is active.
16. Typical values are measured at 3.3V, 25°C and 20-ns cycle time.

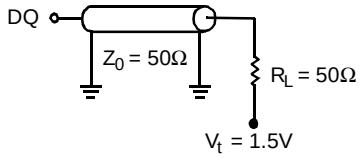
Capacitance

Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_I	Input Capacitance[17]	T_A = 25°C, f = 1 MHz, V_{CC}= 3.3V	4	5	pF
C_O	Input/Output Capacitance (DQ)[17]		7	8	pF

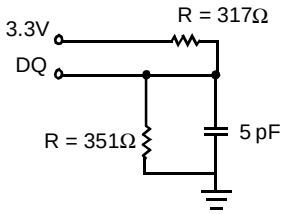
Typical Output Buffer Characteristics

Output High Voltage	Pull-up Current		Output Low Voltage	Pull-down Current	
V_{OH} (V)	I_{OH} (mA) Min.	I_{OH} (mA) Max.	V_{OL} (V)	I_{OL} (mA) Min.	I_{OL} (mA) Max.
–0.5	–38	–105	–0.5	0	0
0	–38	–105	0	0	0
0.8	–38	–105	0.4	10	20
1.25	–26	–83	0.8	20	40
1.5	–20	–70	1.25	31	63
2.3	0	–30	1.6	40	80
2.7	0	–10	2.8	40	80
2.9	0	0	3.2	40	80
3.4	0	0	3.4	40	80

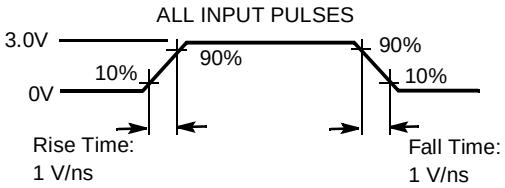
AC Test Loads and Waveforms



(a)



(b)



(c)

Note:
17. This parameter is sampled.

Switching Characteristics Over the Operating Range[19]

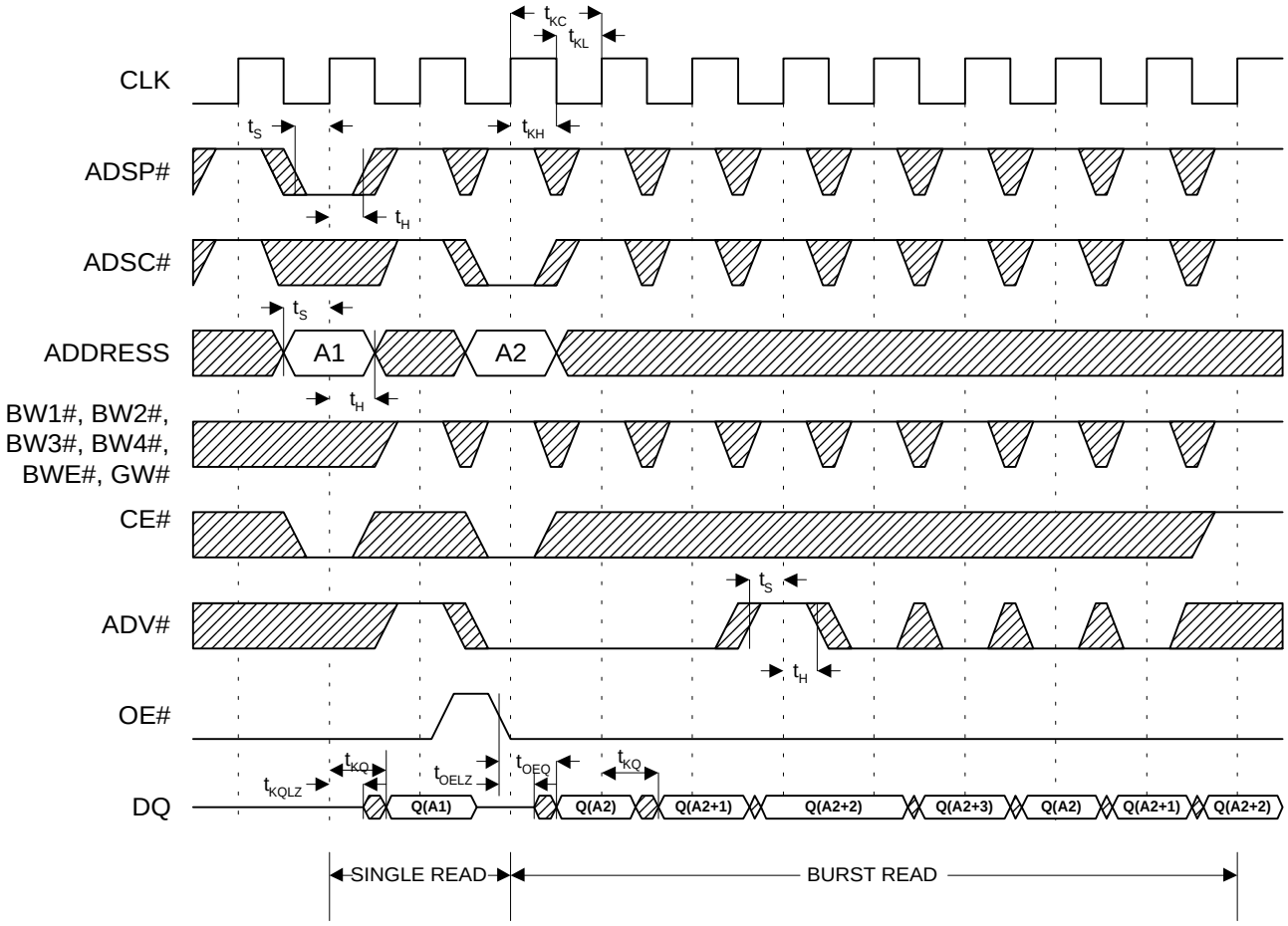
Parameter	Description	-3 166 MHz		-4 150 MHz		-5 133 MHz		-6 117 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock										
t_{KC}	Clock Cycle Time	6.0		6.7		7.5		8.5		ns
t_{KH}	Clock HIGH Time	2.4		2.6		2.8		3.4		ns
t_{KL}	Clock LOW Time	2.4		2.6		2.8		3.4		ns
Output Times										
t_{KQ}	Clock to Output Valid		3.5		3.8		4.0		4.0	ns
t_{KQX}	Clock to Output Invalid	1.5		1.5		1.5		1.5		ns
t_{KQLZ}	Clock to Output in Low-Z[17, 18, 20]	0		0		0		0		ns
t_{KQHZ}	Clock to Output in High-Z[17, 18, 20]	1.5	6.0	1.5	6.7	1.5	7.5	1.5	8.5	ns
t_{OEQ}	OE to Output Valid[21]		3.5		3.5		3.8		3.8	ns
t_{OELZ}	OE to Output in Low-Z[17, 18, 20]	0		0		0		0		ns
t_{OEHZ}	OE to Output in High-Z[17, 18, 20]		3.5		3.5		3.8		3.8	ns
Set-Up Times										
t_S	Address, Controls and Data In[22]	1.5		1.5		1.5		2.0		ns
Hold Times										
t_H	Address, Controls and Data In[22]	0.5		0.5		0.5		0.5		ns

Notes:

18. Output loading is specified with C_L=5 pF as in AC Test Loads.
19. Test conditions as specified with the output loading as shown in AC Test Loads unless otherwise noted.
20. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
21. $\overline{OE}$ is a “Don’t Care” when a byte write enable is sampled LOW.
22. This is a synchronous device. All synchronous inputs must meet specified set-up and hold time, except for “Don’t Care” as defined in the truth table.

Timing Diagrams

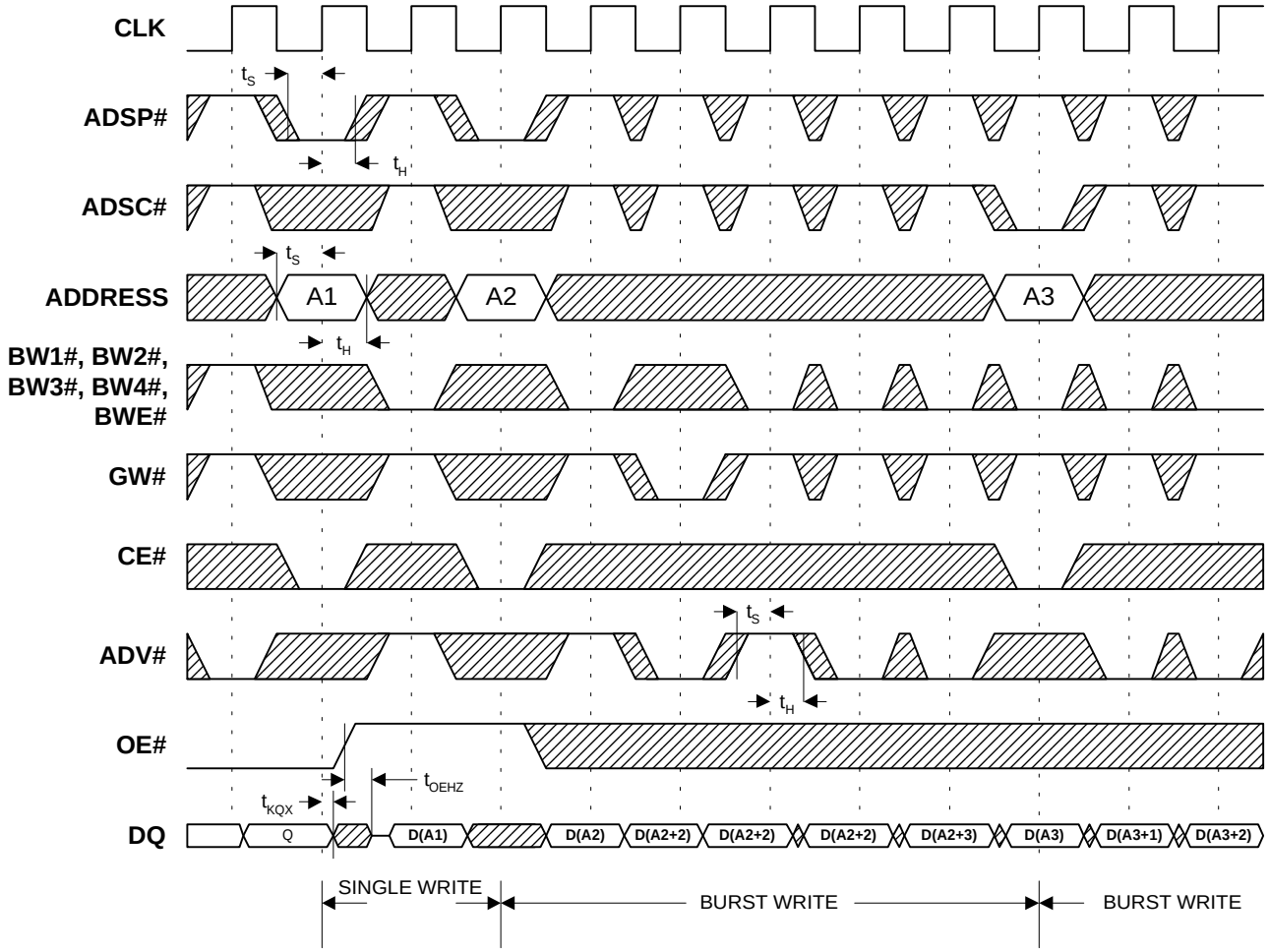
Read Timing[23]



Note:
23. $\overline{CE}$ active in this timing diagram means that all chip enables $\overline{CE}$, $\overline{CE2}$, and CE2 are active.

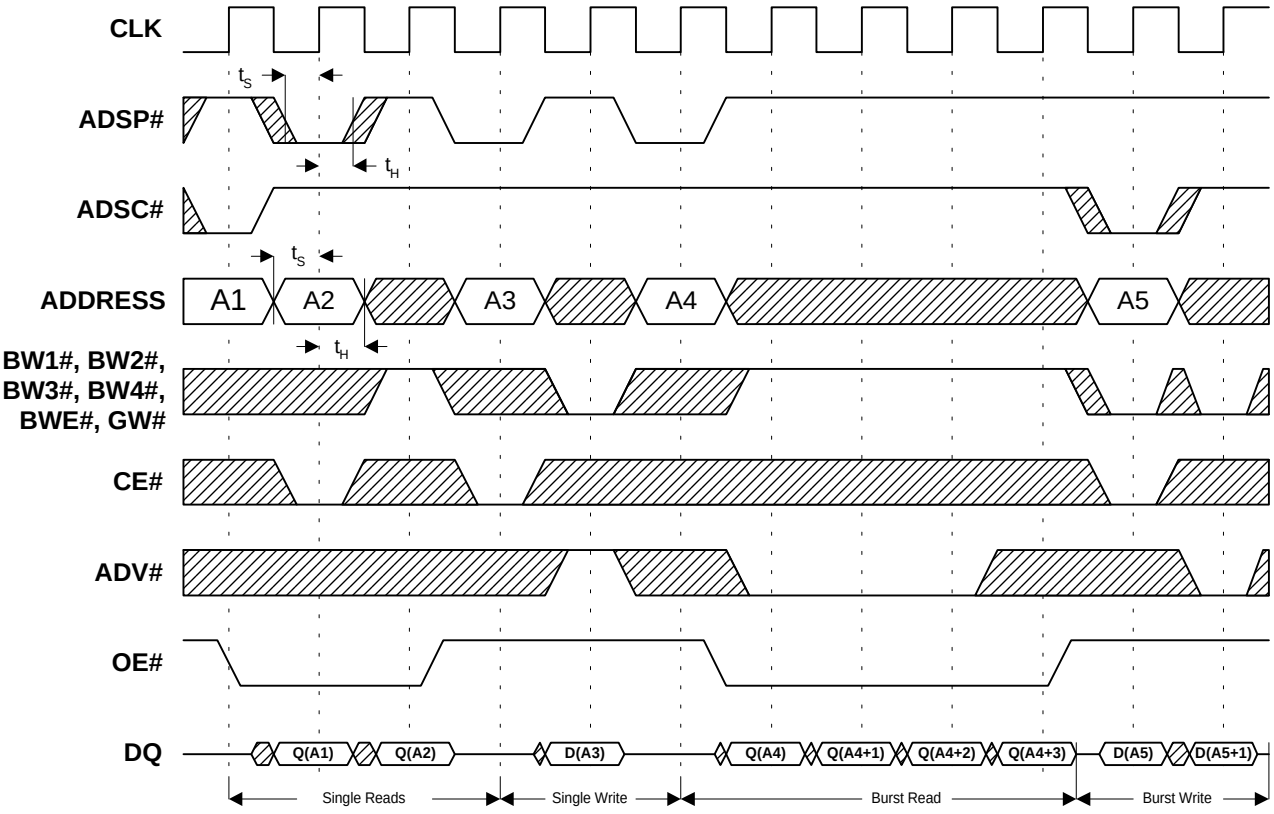
Timing Diagrams (continued)

Write Timing[23]



Timing Diagrams (continued)

Read/Write Timing[23]



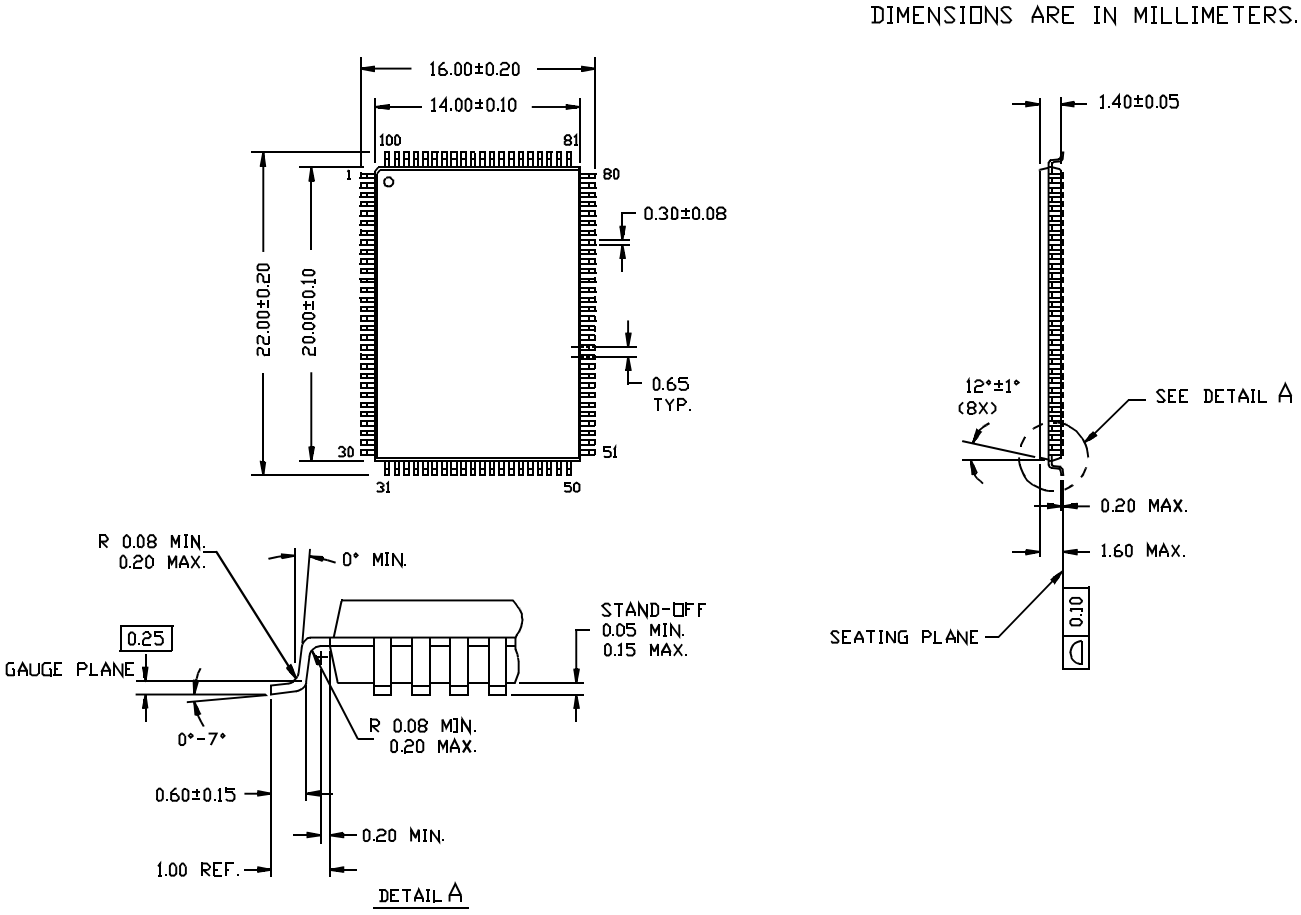
Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	CY7C1346A-166AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT7164D36T-3			
150	CY7C1346A-150AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT7164D36T-4			
133	CY7C1346A-133AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT7164D36T-5			
117	CY7C1346A-117AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	GVT7164D36T-6			

Document #: 38-01020-**

Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



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