GRF1001 1.6-1.8GHz Frequency Synthesizer with Integrated VCO

General Descriptions

The GRF1001 is a CMOS monolithic integrated circuit for CDMA systems. The circuit includes an on-chip RF VCO, phase-frequency detector (PFD), charge pump, and loop filter. With this circuit, the local oscillator (LO) signal can be generated with only few external elements, such as bypass elements and matching elements. The circuit also includes an IF PLL and charge pump to facilitate board level design. Only a tank circuit and loop filter are needed to complete IF frequency generation. The device will be provided in a 20-pin QFN package.

Features

- Proprietary Fractional-N Frequency Synthesizer Architecture
- On-chip PLL Frequency Synthesizer
- On-chip RF VCO
- On-chip Loop Filter
- 2.7V to 3.3V operation
- 15mA typical supply current
- IF power down mode

Application

- PCS (Korean PCS and US PCS) dual-mode CDMA systems

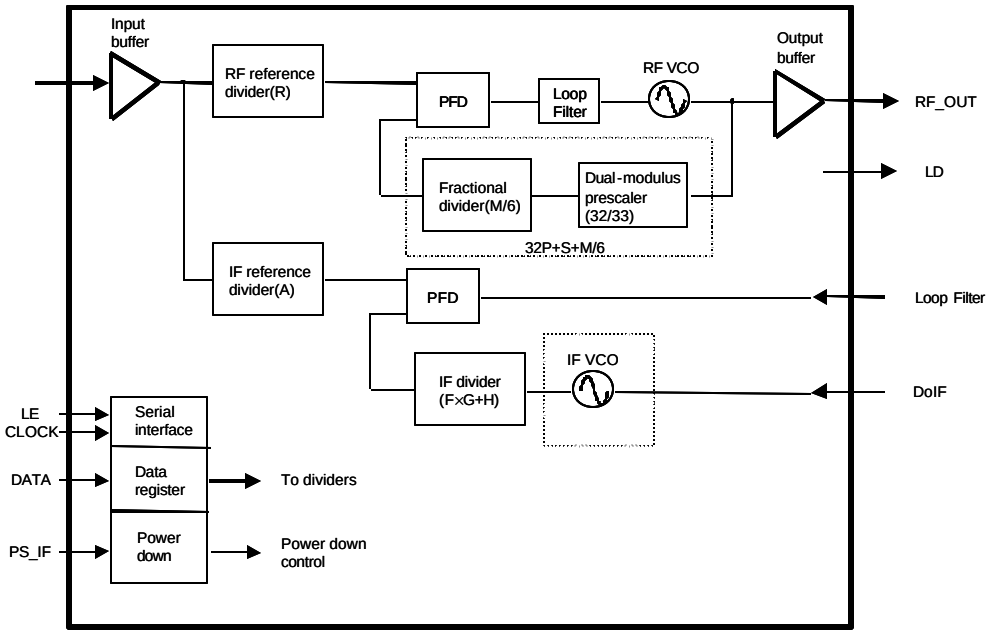

Figure 1. GRF1001 Circuit Block Diagram

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Function Description

Product Description

The GRF1001 has a highly integrated CMOS PLL for generating the local oscillator (LO) signal in the PCS system around 1.7MHz. The wide operating range of the circuit enables dual-mode function in different bands (Korean PCS and US PCS) and allows both to be implemented in the same circuit. The circuit includes all functional blocks, including RF VCO, prescaler, PFD, and loop filter. Only few external elements are needed to complete the PLL, specifically matched output impedance and bypass elements for power line stabilization.

The GRF1001 circuit includes IF VCO, IF prescaler, and PFD to support IF carrier generation. An off-chip inductor and appropriate loop filter are used to tune the IF frequency at the desired value.

The circuit uses a patent-pending Fractional-N synthesizer architecture to support 10KHz channel spacing. The circuit supports various reference frequencies with 10KHz minimum resolution, such as 19.6, 19.68, and 19.8MHz. The Fractional-N architecture has very low spurious modulation effect, which is a big problem in conventional scheme. This enables fast lock-up to reduce the power consumption and system set-up time. Another advantage of is that the occupied area of the loop filter is reduced compared to integer-N, which allows the loop filter to be included in the circuit to minimize the external noise coupling and save space on the board.

IF-PLL Section

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{4 \times (A+1) + (B+1)\} \times f_{OSC} / R \ (B < A)$

f_{VCO} : Output frequency of voltage controlled oscillator(VCO)
A : Preset divide ratio of binary 13-bit programmable counter ($1 \le A \le 8,191$)
B : Preset divide ratio of binary 4-bit swallow counter ($0 \le B \le 15$)
f_{OSC} : Reference oscillation frequency

R : Preset divide ratio of binary 15-bit programmable reference counter ($2 \le R \le 32,767$)

RF-PLL Section

$f_{VCO} = \{32 \times P + S + (M / 6)\} \times f_{OSC} / R \ (S < P)$

f_{VCO} : Output frequency of voltage controlled oscillator(VCO)
P : Preset divide ratio of binary 13-bit programmable counter ($2 \le P \le 8,191$)
S : Preset divide ratio of binary 6-bit swallow counter ($0 \le S \le 63$)
M : Preset 3-bit numerator of modulus counter ($0 \le M \le 5$)
f_{OSC} : Reference oscillation frequency

R : Preset divide ratio of binary 13-bit programmable reference counter ($1 \le R \le 8,191$)

Power down modes

The circuit includes the various power down modes to reduce the power consumption. The IF-PLL enters in power saving mode by setting PDN_{IF} pin to low. When the PDN_{IF} is high, the IF-PLL operates in normal mode. During power down mode, phase detector output(DoIF) becomes high impedance and thus IF-PLL loses lock.

A register(register 0) has a allocated bit(PDN_{RF}) for power down of the RF-PLL. This register can be written by the serial interface. When PDN_{RF} is low, the RF-PLL enters in power saving mode and loses lock.

Serial interface

The frequency setting and other auxiliary functions, such as power down, are established by the serial interface. The serial interface is a 3-wire serial interface that have CLOCK, DATA, and LE(Load ENABLE) pins.

Programmable dividers in the RF/IF PLL are separated and controlled individually. Each divider has its own register. The data pin is serially accessed in a shift register. The operation of shift register is controlled by a clock pin. On the rising edge of clock, one bit of serial data is transferred into the shift register. When LE signal is high, the data stored in the shift register is transferred to one register latch depending upon the control bit data setting.

When all bits are loaded in the shift register, the stored value in shift register is transferred to the corresponding register according to the control bits setting. The time at which data loading occurs is indicated by low-to-high transition of LE signal.

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Electrical specifications

Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.4 to 5	VDC
Storage Temperature Range	-40 to 85	°C

Parameter	Min	Typ	Max	Unit	Remarks
Supply Voltage	2.7	3.0	3.3	Volt	DC voltage
Current Consumption		18	20	mA	
Frequency Range	1.6		1.8	GHz	RF frequency
Output Power	-3	0	3	dBm	
Lock Time		0.5	0.6	msec	26MHz Band
Operating Temperature	-30		80	°C	
Phase Noise		-111	-108	dBc/Hz	@100kHz offset
		-133	-130		@1MHz offset
2nd Harmonic Suppression			-20		
IF Input Frequency			500	MHz	

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