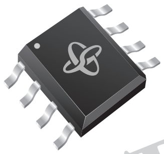
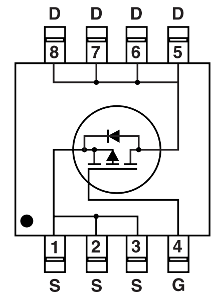
GF4425

P-Channel Enhancement-Mode MOSFET

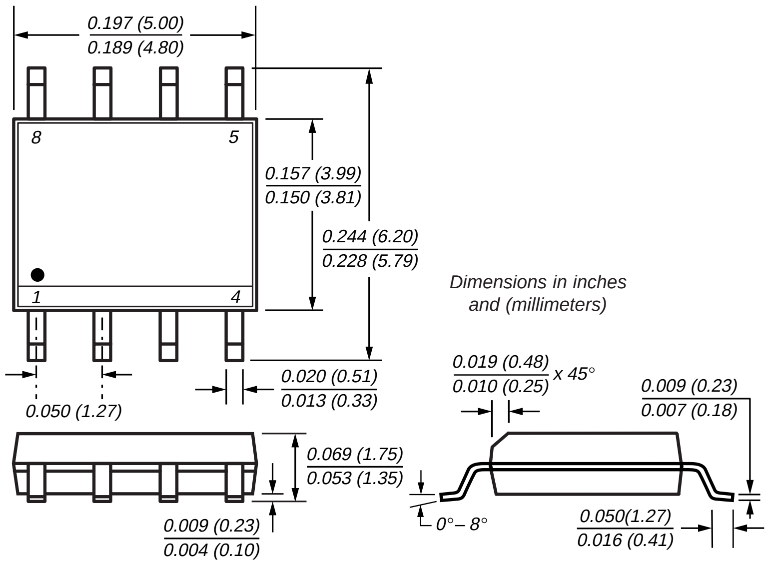
V_{DS} –30V **$R_{DS(ON)}$** 14mΩ **I_D** -11A

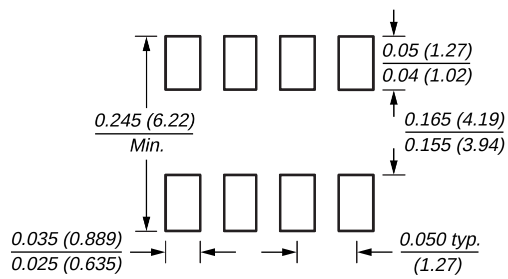


TRENCH GENFET® New Product



SO-8





Mounting Pad Layout

Mechanical Data

Case: SO-8 molded plastic body

Terminals: Leads solderable per MIL-STD-750, Method 2026

High temperature soldering guaranteed: 250°C/10 seconds at terminals

Mounting Position: Any

Weight: 0.5g

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Specially Designed for Low Voltage DC/DC Converters
- Fast Switching for High Efficiency

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[1]	T_A = 25°C T_A = 70°C	I_D	–11 –8.7	A
Pulsed Drain Current		I_{DM}	–50	
Maximum Power Dissipation	T_A = 25°C T_A = 70°C	P_D	2.5 1.6	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Maximum Junction-to-Ambient[1]		$R_{θJA}$	50	°C/W

Notes: (1) Surface Mounted on FR4 Board, t ≤ 10 sec.

GENERAL SEMICONDUCTOR®

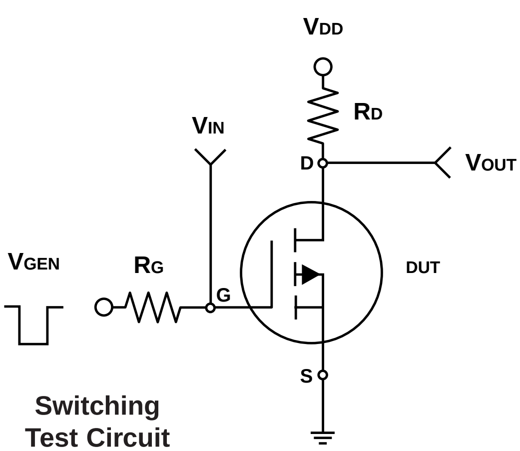
GF4425

P-Channel Enhancement-Mode MOSFET

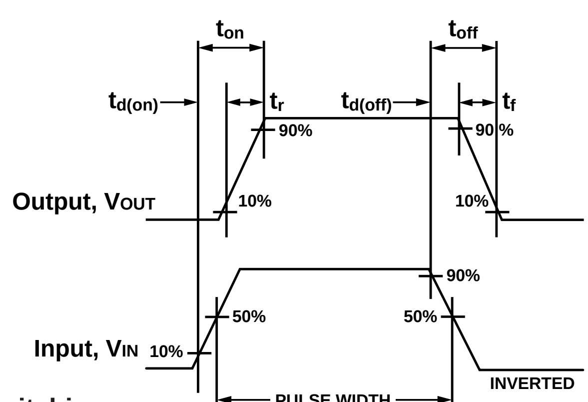
Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = –250µA	–1.0	—	—	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	—	—	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30V, V_{GS} = 0V	—	—	–1.0	µA
		V_{DS}=–15V, V_{GS}=0, T_J=70°C	—	—	–5.0	
On-State Drain Current(1)	$I_{D(on)}$	$V_{DS} \geq$ –5V, V_{GS} = –10V	–30	—	—	A
Drain-Source On-State Resistance(1)	$R_{DS(on)}$	V_{GS} = –10V, I_D = –11A	—	11.5	14	mΩ
		V_{GS} = –4.5V, I_D = –8.5A	—	15.5	23	
Forward Transconductance(1)	g_{fs}	V_{DS} = –15V, I_D = –11A	—	37	—	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = –15V, V_{GS} = –10V I_D = –11A	—	73	120	nC
Gate-Source Charge	Q_{gs}		—	12	—	
Gate-Drain Charge	Q_{gd}		—	11	—	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –15V, R_L = 15Ω $I_D \approx$ –1A, V_{GEN} = –10V R_G = 6Ω	—	7	25	ns
Rise Time	t_r		—	11	25	
Turn-Off Delay Time	$t_{d(off)}$		—	210	250	
Fall Time	t_f		—	76	100	
Input Capacitance	C_{iss}	V_{DS} = –15V, V_{GS} = 0V f = 1.0 MHz	—	3500	—	pF
Ouput Capacitance	C_{oss}		—	700	—	
Reverse Transfer Capacitance	C_{rss}		—	370	—	
Source-Drain Diode						
Maximum Diode Forward Current	I_S		—	—	–2.1	A
Diode Forward Voltage	V_{SD}	I_S = –2.1A, V_{GS} = 0V	—	—	–1.2	V
Source-Drain Reverse Recovery Time	t_{rr}	I_F = -2.1A, di/dt = 100A/µs	—	49	90	ns

Note:
(1) Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%



Switching Test Circuit



Switching Waveforms

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

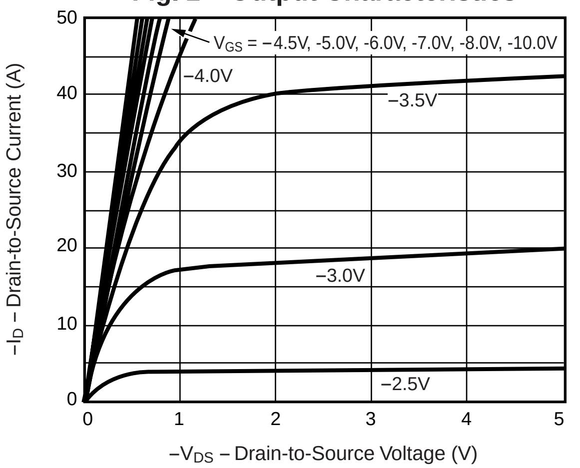


Fig. 2 – Transfer Characteristics

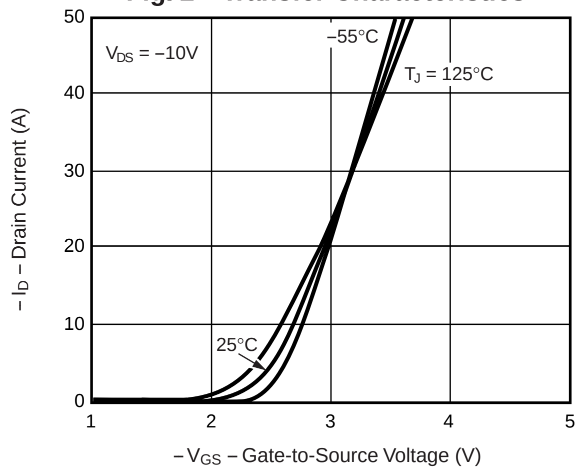


Fig. 3 – Threshold Voltage vs. Temperature

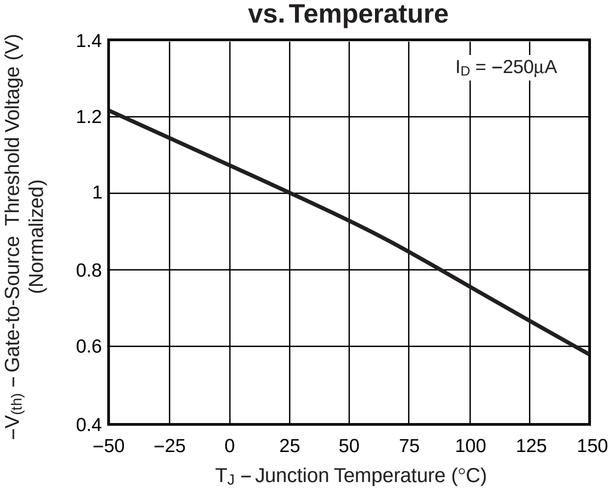


Fig. 4 – On-Resistance vs. Drain Current

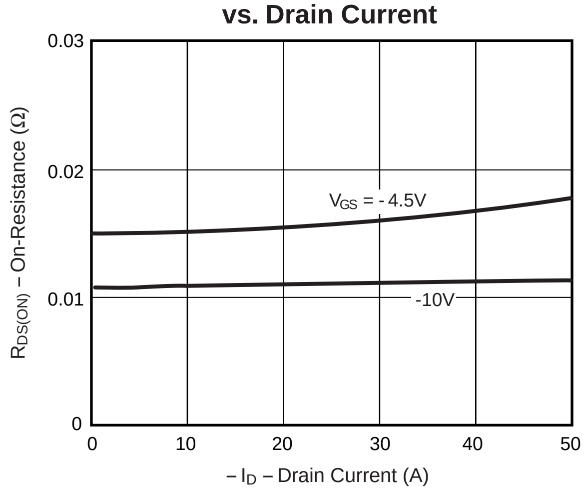


Fig. 5 – On-Resistance vs. Junction Temperature

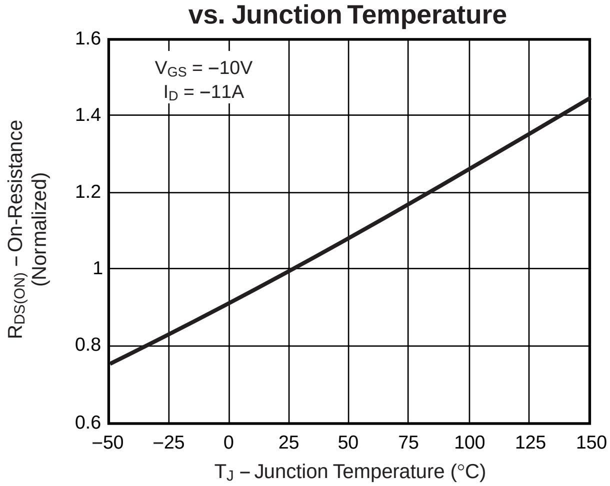
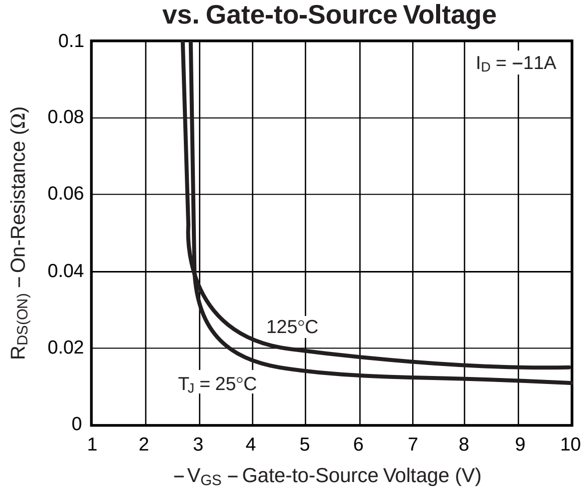


Fig. 6 – On-Resistance vs. Gate-to-Source Voltage



P-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 7 – Gate Charge

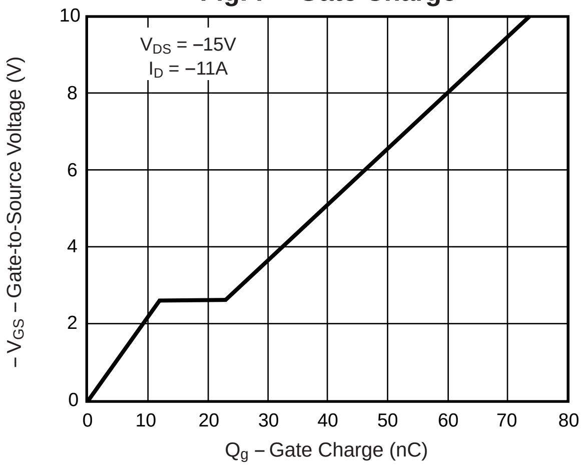


Fig. 8 – Capacitance

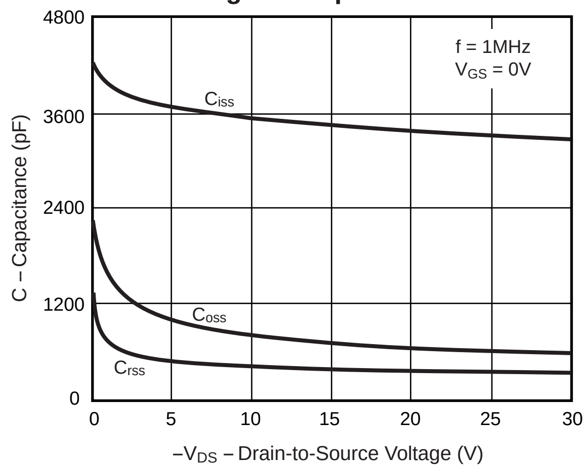


Fig. 9 – Source-Drain Diode Forward Voltage

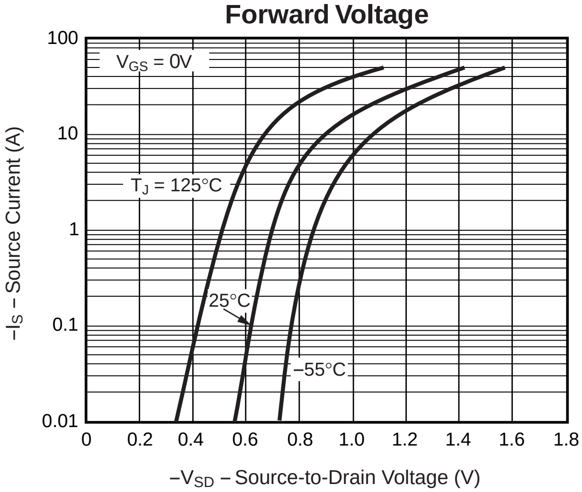


Fig. 10 – Transient Thermal Impedance

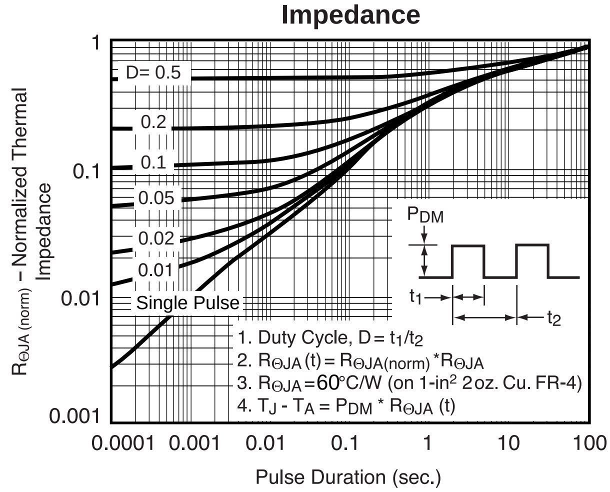


Fig. 11 – Power vs. Pulse Duration

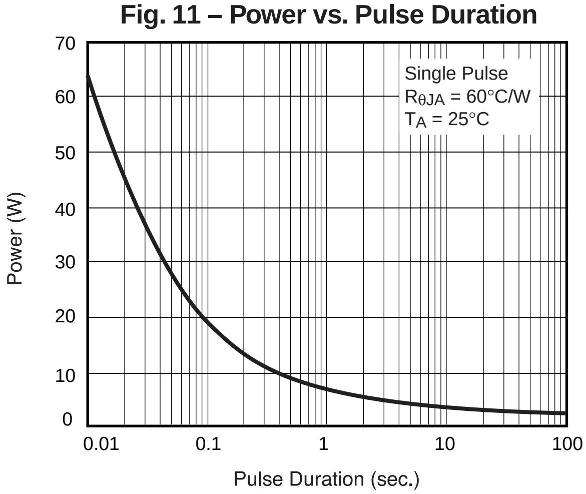


Fig. 12 – Maximum Safe Operating Area