

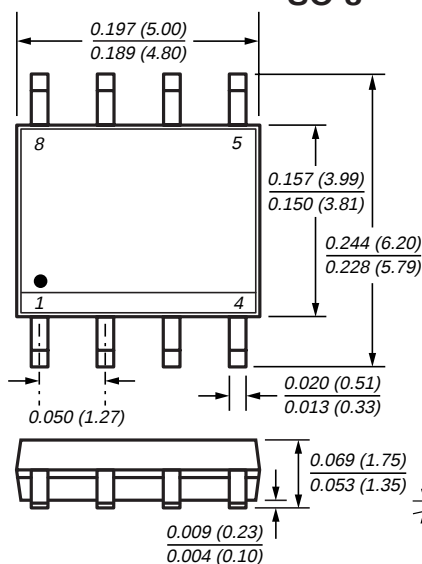
N-Channel Enhancement-Mode MOSFET

Low $V_{GS(th)}$ V_{DS} 20V $R_{DS(on)}$ 30m Ω I_D 7.2A

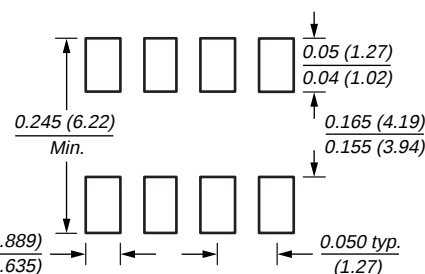
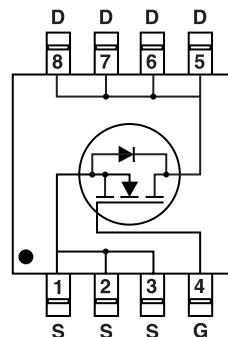
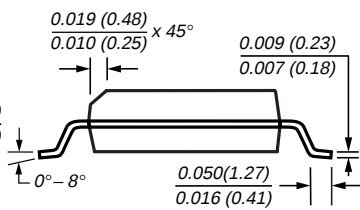
TRENCH
GENFET®

New Product

SO-8



Dimensions in inches
and (millimeters)



Mechanical Data

Case: SO-8 molded plastic body

Terminals: Leads solderable per MIL-STD-750, Method 2026

High temperature soldering guaranteed:
250°C/10 seconds at terminals

Mounting Position: Any

Weight: 0.5g

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Fast Switching
- Logic Level
- Ideal for DC/DC converters

Maximum Ratings and Thermal Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	
Continuous Drain Current at $T_J = 150^\circ\text{C}^{(1)}$, $T_A = 25^\circ\text{C}$	I_D	7.2	A
Pulsed Drain Current	I_{DM}	20	
Maximum Power Dissipation ⁽¹⁾	P_D	2.5 1.6	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Maximum Junction-to-Ambient ⁽¹⁾ Thermal Resistance	$R_{\theta JA}$	50	$^\circ\text{C/W}$

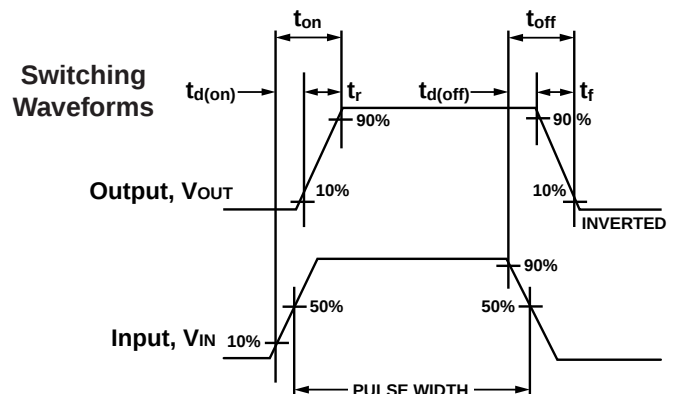
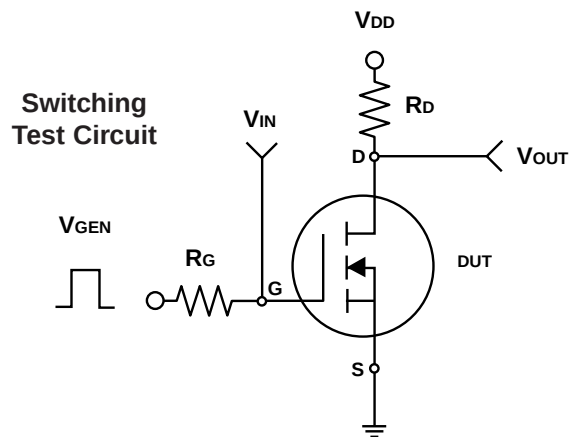
N-Channel Enhancement-Mode MOSFET

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	20	—	—	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.6	—	—	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±8V	—	—	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V, V _{GS} = 0V	—	—	1.0	μA
On-State Drain Current ⁽²⁾	I _{D(on)}	V _{DS} ≥ 5V, V _{GS} = 4.5V	20	—	—	A
Drain-Source On-State Resistance ⁽²⁾	R _{DS(on)}	V _{GS} = 4.5V, I _D = 7.2A	—	22	30	mΩ
		V _{GS} = 2.5V, I _D = 6.2A	—	28	40	
Forward Transconductance ⁽²⁾	g _{fs}	V _{DS} = 10V, I _D = 7.2A	—	24	—	S
Dynamic						
Total Gate Charge	Q _g	V _{DS} = 10V, V _{GS} = 4.5V I _D = 7.2A	—	13	20	nC
Gate-Source Charge	Q _{gs}		—	2.3	—	
Gate-Drain Charge	Q _{gd}		—	3	—	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10V, R _L = 10Ω I _D ≈ 1A, V _{GEN} = 4.5V R _G = 6Ω	—	11	22	ns
Rise Time	t _r		—	15	30	
Turn-Off Delay Time	t _{d(off)}		—	43	65	
Fall Time	t _f		—	22	35	
Input Capacitance	C _{iSS}	V _{GS} = 0V	—	1240	—	pF
Output Capacitance	C _{oSS}	V _{DS} = 10V	—	200	—	
Reverse Transfer Capacitance	C _{rSS}	f = 1.0MHz	—	120	—	
Source-Drain Diode						
Max. Diode Forward Current	I _S	—	—	—	1.7	A
Diode Forward Voltage ⁽²⁾	V _{SD}	I _S = 1.7A, V _{GS} = 0V	—	0.7	1.3	V

Notes: (1) Surface mounted on FR4 board, $t \leq 10$ sec.

(2) Pulse test; pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$



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Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 1 – Output Characteristics

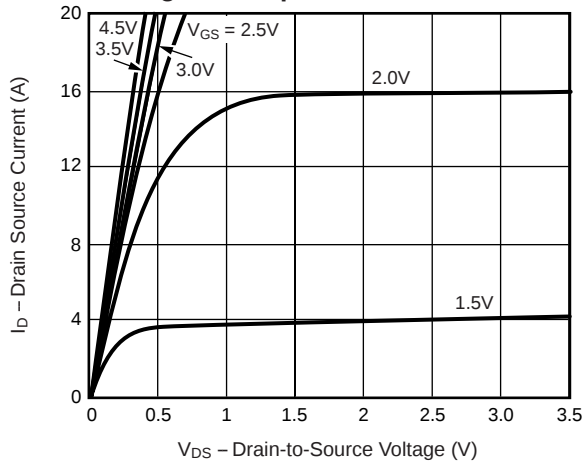
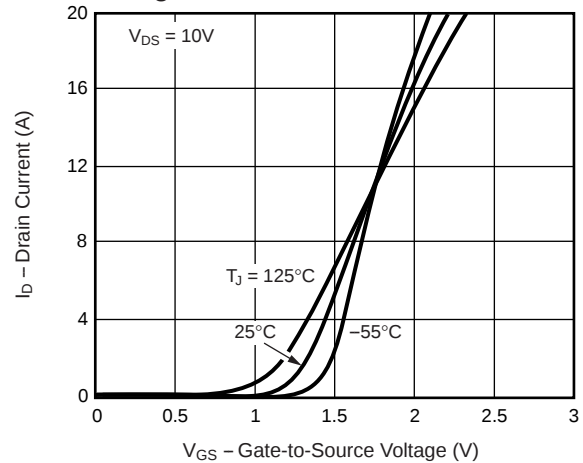
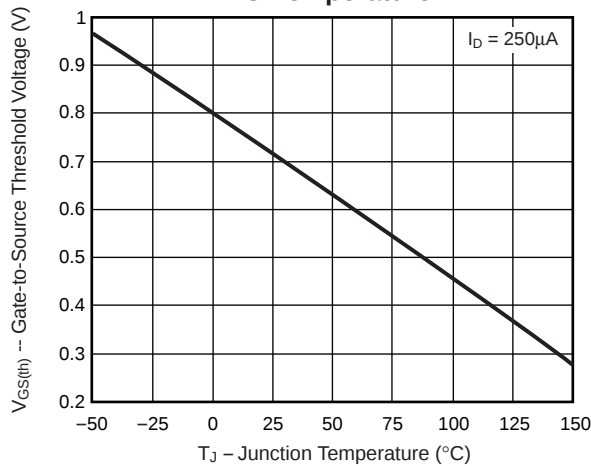


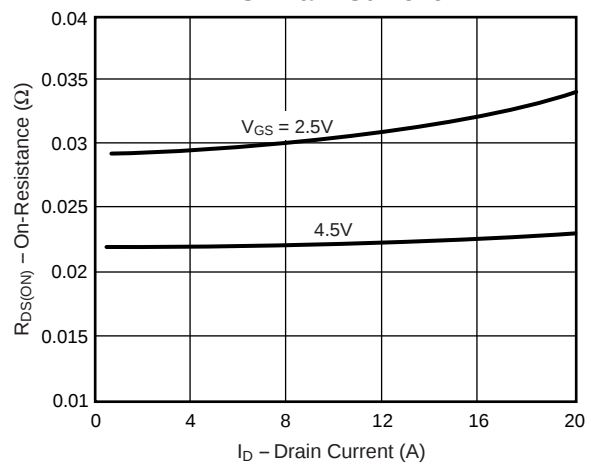
Fig. 2 – Transfer Characteristics



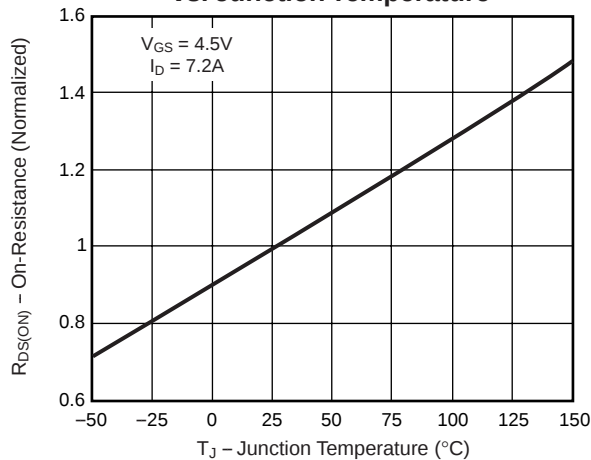
**Fig. 3 – Threshold Voltage
vs. Temperature**



**Fig. 4 – On-Resistance
vs. Drain Current**



**Fig. 5 – On-Resistance
vs. Junction Temperature**



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Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

**Fig. 6 – On-Resistance
vs. Gate-to-Source Voltage**

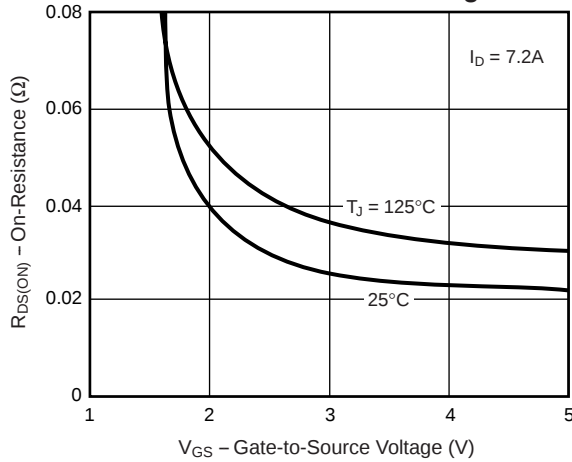


Fig. 7 – Gate Charge

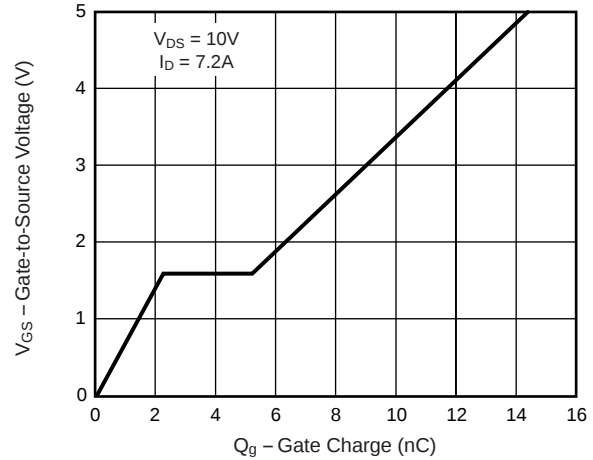
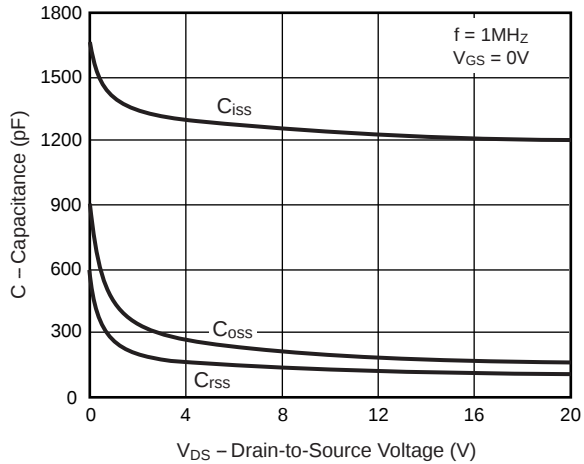
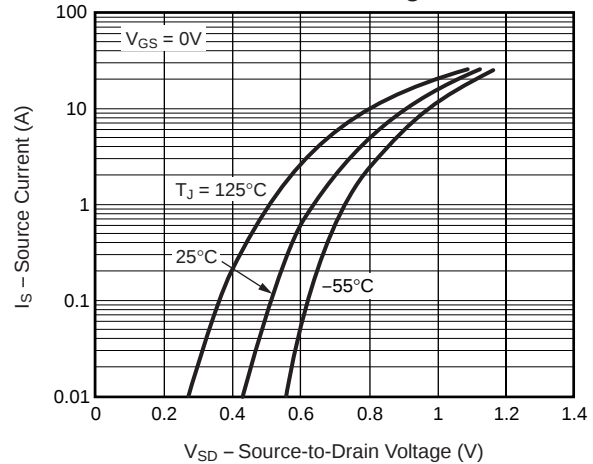


Fig. 8 – Capacitance



**Fig. 9 – Source-Drain Diode
Forward Voltage**



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Fig. 10 – Breakdown Voltage vs. Junction Temperature

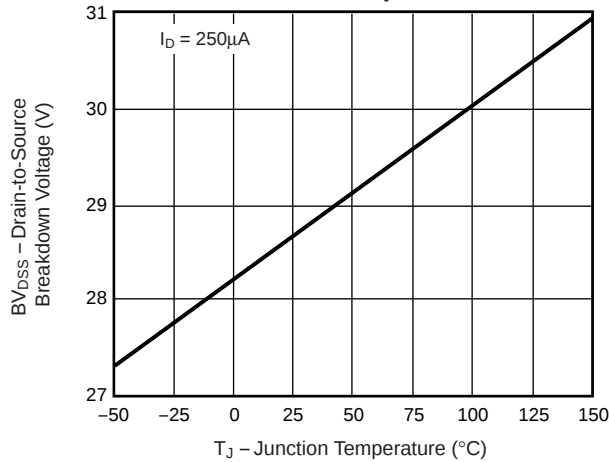


Fig. 11 – Transient Thermal Impedance

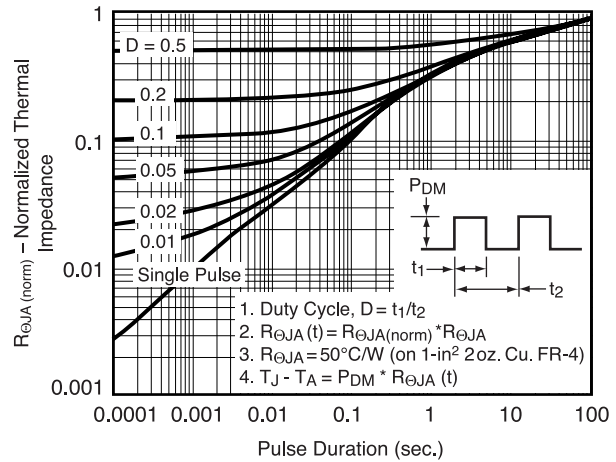


Fig. 12 – Power vs. Pulse Duration

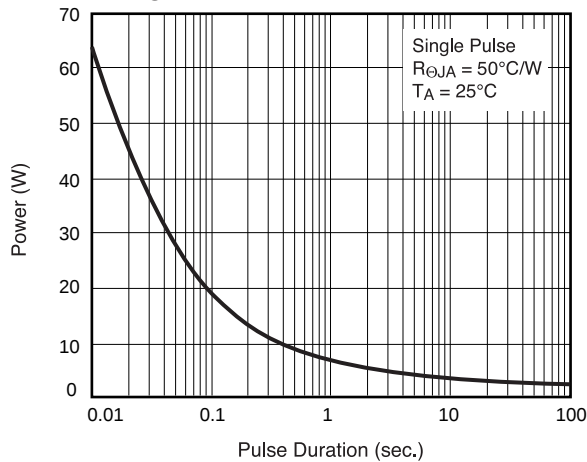


Fig. 13 – Maximum Safe Operating Area

