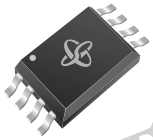
GENERAL SEMICONDUCTOR®

GF6968A

Common-Drain Dual N-Channel MOSFET

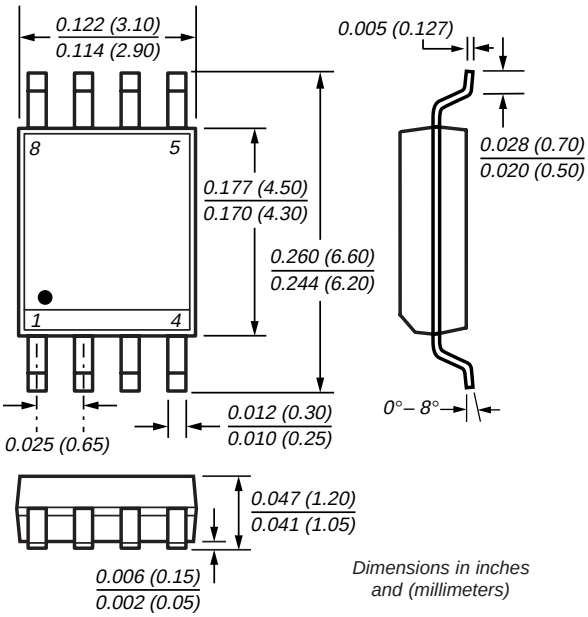
Low $V_{GS(th)}$ V_{DS} 20V **$R_{DS(ON)}$** 22mΩ **I_D** 6.2A



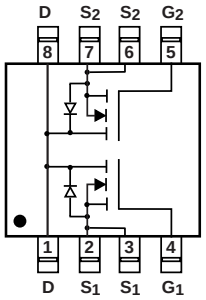
TRENCH GENFET®

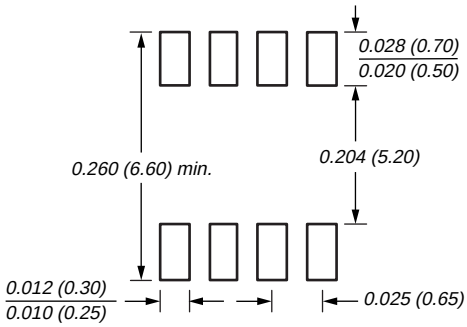
New Product

TSSOP-8



Dimensions in inches and (millimeters)





Mounting Pad Layout

Mechanical Data

Case: TSSOP-8 Package

Terminals: Leads solderable per MIL-STD-750, Method 2026

High temperature soldering guaranteed: 250°C/10 seconds at terminals

Mounting Position: Any

Weight: 0.5g

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Specially Designed for Li-ion battery packs use
- Designed for battery-switch applications

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current (T_J = 150°C)(1)		I_D	6.2	A
Pulsed Drain Current		I_{DM}	30	A
Maximum Power Dissipation(1)	T_A = 25°C T_A = 70°C	P_D	1.5 0.96	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Maximum Junction-to-Ambient(1) Thermal Resistance		$R_{\theta JA}$	83	°C/W

Notes: (1) Surface mounted on FR4 board, t ≤ 10 sec.

4/11/01

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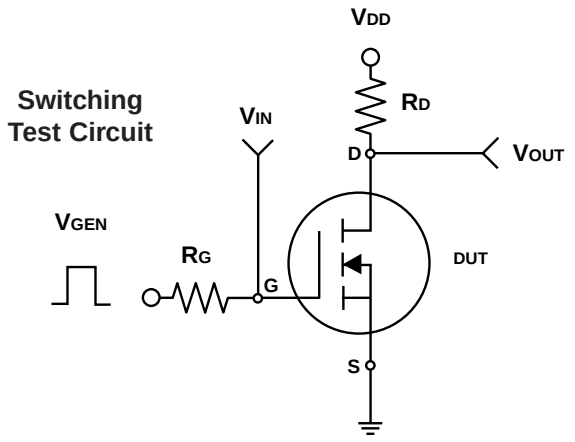
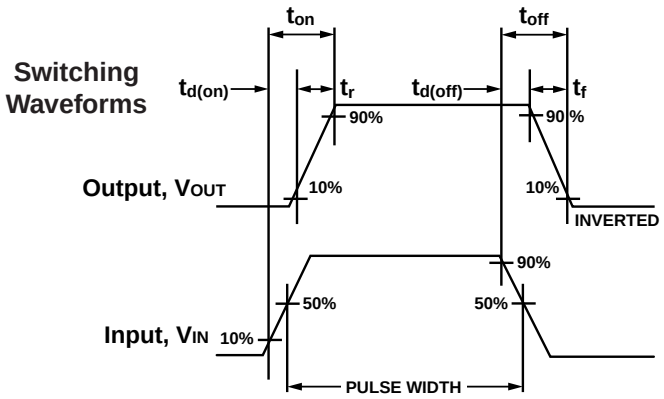
Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	20	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	0.6	–	–	V
Gate Body Leakage	I_{GSS}	V_{GS} = ± 12V, V_{DS} = 0V	–	–	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V	–	–	1	µA
On-State Drain Current[1]	$I_{D(on)}$	V_{DS} ≥ 5V, V_{GS} = 4.5V	30	–	–	A
Drain-Source On-State Resistance[1]	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 6.2A	–	17.5	22	mΩ
		V_{GS} = 2.5V, I_D = 5.3A	–	25	30	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10V, I_D = 6.2A	–	26.5	–	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 10V, V_{GS} = 4.5V I_D = 6.2A	–	14	20	nC
Gate-Source Charge	Q_{gs}		–	2.2	–	
Gate-Drain Charge	Q_{gd}		–	3	–	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, R_L = 10Ω I_D = 1A, V_{GEN} = 4.5V R_G = 6Ω	–	11	30	ns
Turn-On Rise Time	t_r		–	15	50	
Turn-Off Delay Time	$t_{d(off)}$		–	43	100	
Fall Time	t_f		–	22	50	
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V f = 1.0 MHz	–	1240	–	pF
Output Capacitance	C_{oss}		–	200	–	
Reverse Transfer Capacitance	C_{rss}		–	120	–	
Source-Drain Diode						
Maximum Diode Forward Current	I_S	—	–	–	1.7	A
Diode Forward Voltage	V_{SD}	I_S = 6.2A, V_{GS} = 0V	–	0.8	1.2	V

Note: (1) Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%





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Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

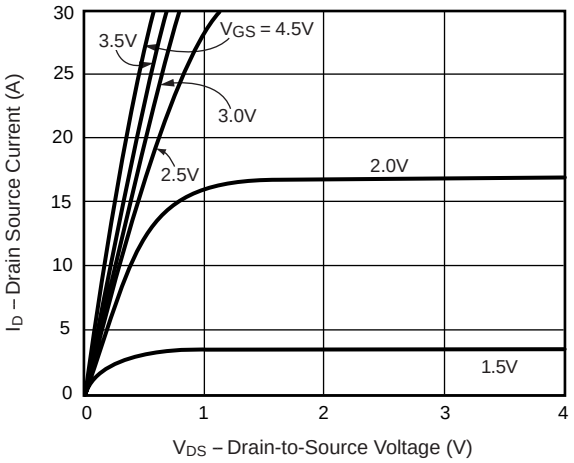

Fig. 2 – Transfer Characteristics

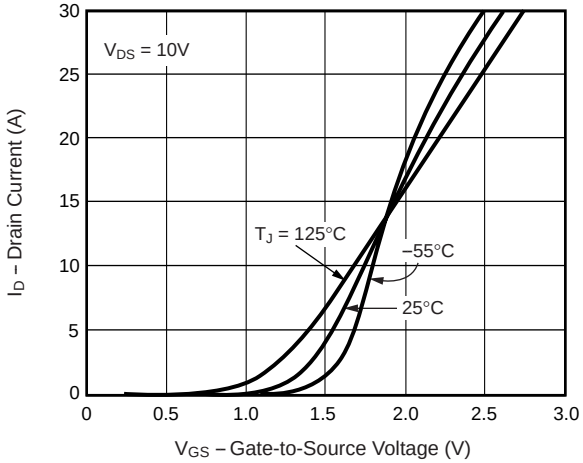

Fig. 3 – Threshold Voltage vs. Temperature

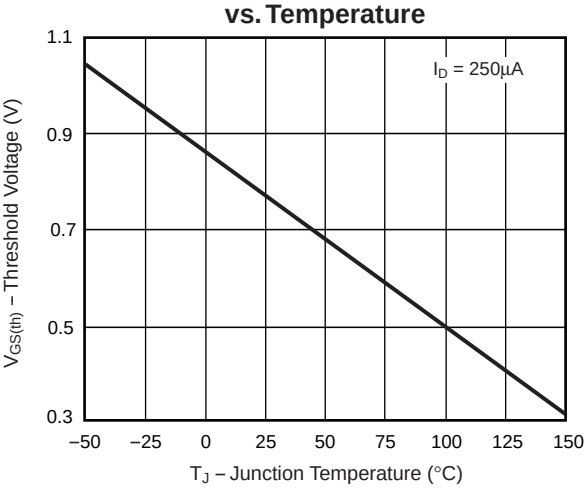

Fig. 4 – On-Resistance vs. Drain Current

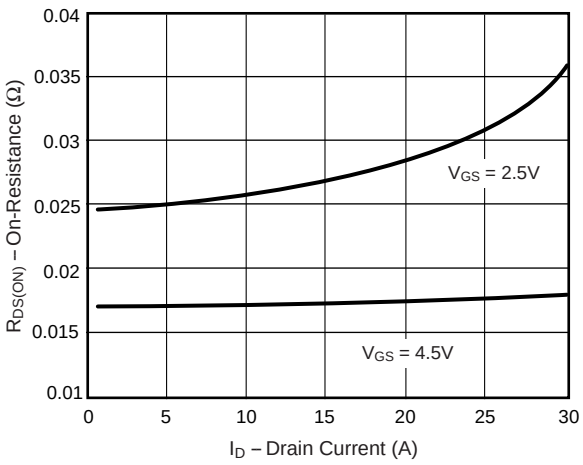

Fig. 5 – On-Resistance vs. Junction Temperature

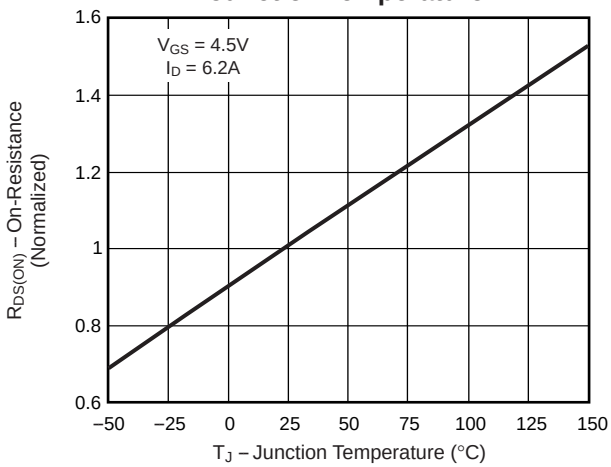

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Fig. 6 – On-Resistance vs. Gate-to-Source Voltage

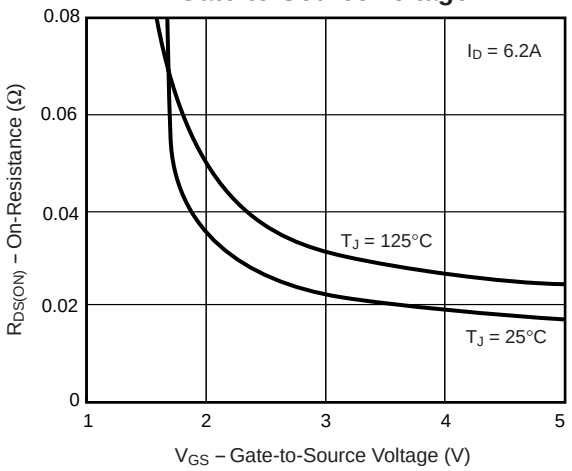

Fig. 7 – Gate Charge

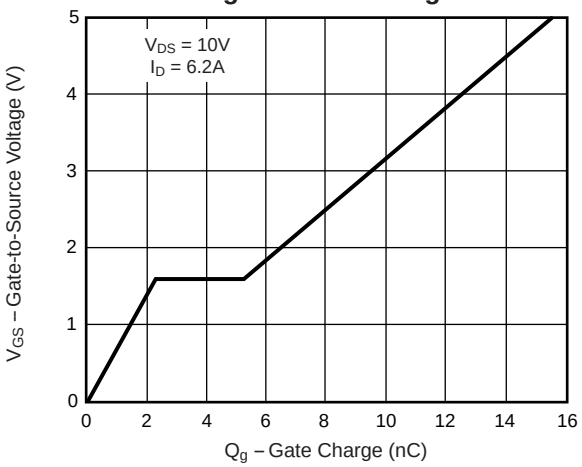

Fig. 8 – Capacitance

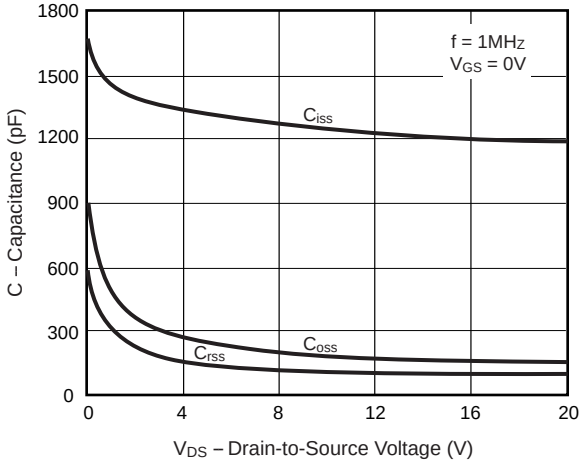

Fig. 9 – Source-Drain Diode Forward Voltage

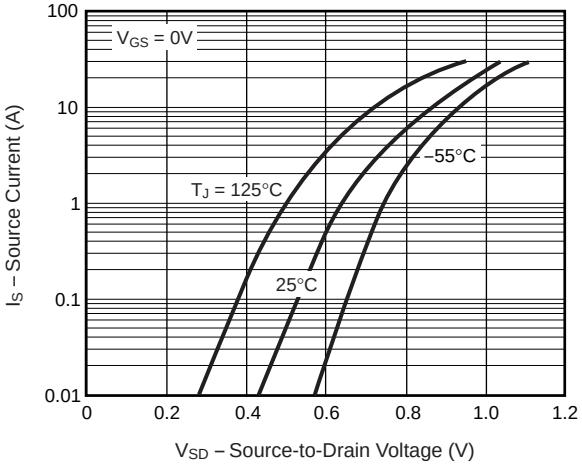

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Fig. 10 – Breakdown Voltage vs. Junction Temperature

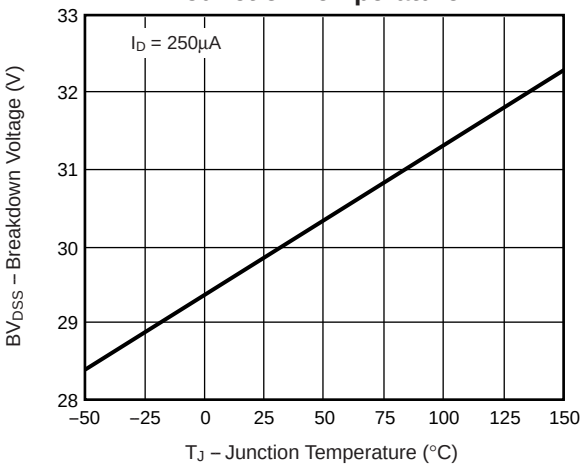

Fig. 11 – Transient Thermal Impedance

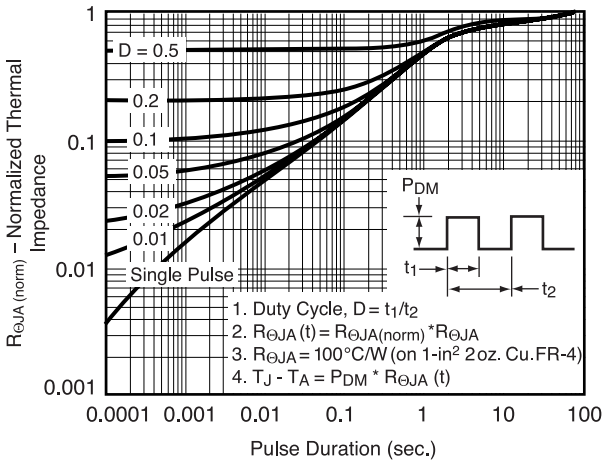

Fig. 12 – Power vs. Pulse Duration

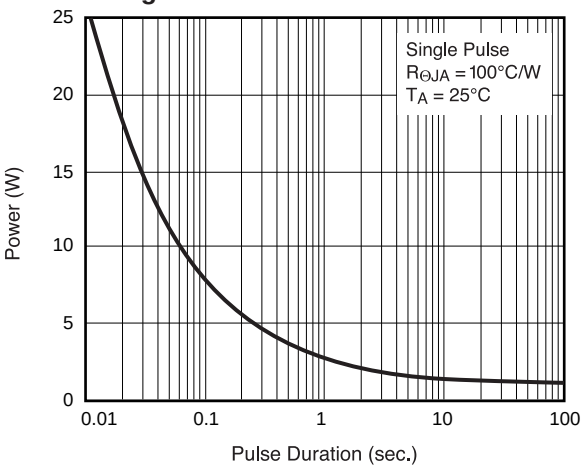

Fig. 13 – Maximum Safe Operating Area