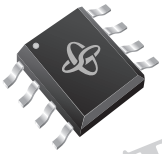
GENERAL SEMICONDUCTOR®

GF2524



TRENCH GENFET®

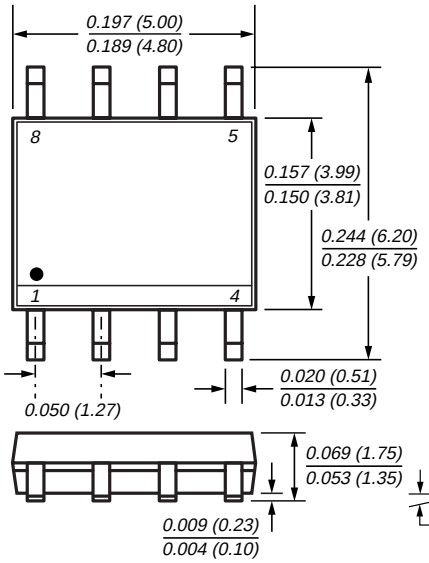
New Product

Asymmetric N-Channel Enhancement-Mode MOSFET

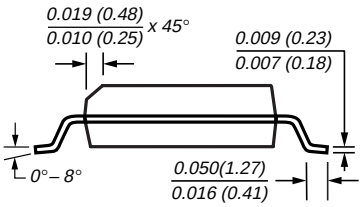
MOSFET 1: V_{DS} 30V $R_{DS(ON)}$ 37mΩ I_D 5.8A

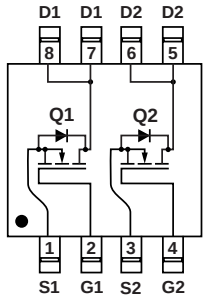
MOSFET 2: V_{DS} 30V $R_{DS(ON)}$ 18mΩ I_D 7.8A

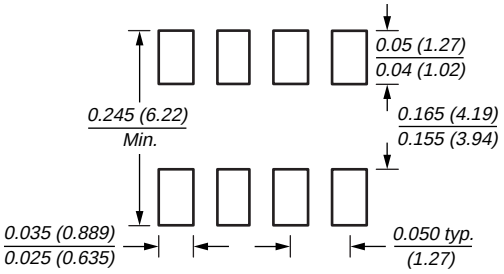
SO-8



Dimensions in inches and (millimeters)







Mounting Pad Layout

Mechanical Data

Case: SO-8 molded plastic body

Terminals: Leads solderable per MIL-STD-750, Method 2026

High temperature soldering guaranteed: 250°C/10 seconds at terminals

Mounting Position: Any

Weight: 0.5g

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Specially Designed for Low Voltage DC/DC Converters
- Fast Switching for High Efficiency
- High efficiency, optimized for PWM.

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	MOSFET-1	MOSFET-2	Unit
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current T_J = 150°C(1)		I_D	5.8	7.8	A
Pulsed Drain Current		I_{DM}	20	30	
Continuous Source Current (Diode Conduction)(1)		I_S	1.7	1.7	
Maximum Power Dissipation(1)	T_A = 25°C T_A = 70°C	P_D	2 1.3	2 1.3	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C
Maximum Junction-to-Ambient(1) Thermal Resistance		$R_{\theta JA}$	62.5	62.5	°C/W

4/11/01

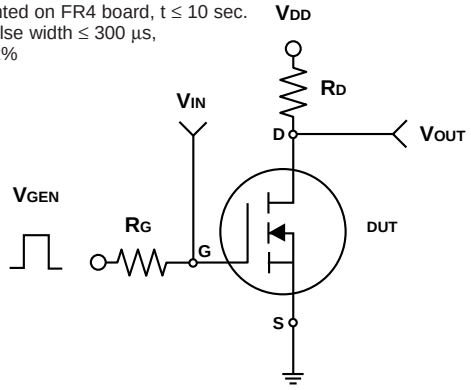
Asymmetric N-Channel Enhancement-Mode MOSFET

Electrical Characteristics (T_J = 25°C unless otherwise noted)

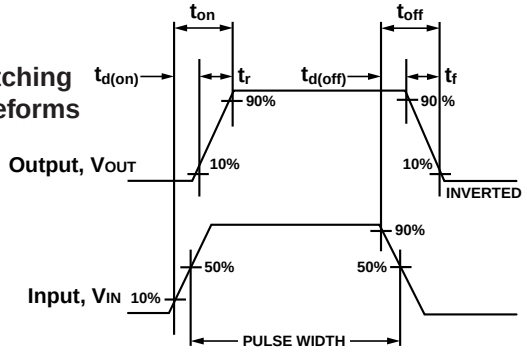
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Static							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	Q1, Q2	30	–	–	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	Q1, Q2	1.0	–	3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q1, Q2	–	–	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	Q1, Q2	–	–	1	µA
On-State Drain Current(2)	$I_{D(on)}$	V_{DS} ≥ 5V, V_{GS} = 10V	Q1 Q2	20 30	– –	– –	A
Drain-Source On-State Resistance(2)	$R_{DS(on)}$	V_{GS} = 10V, I_D = 5.8A V_{GS} = 10V, I_D = 7.8A V_{GS} = 4.5V, I_D = 4.7A V_{GS} = 4.5V, I_D = 6.3A	Q1 Q2 Q1 Q2	– – – –	23.5 15.5 32.5 20.5	37 18 55 28	mΩ
Forward Transconductance(2)	g_{fs}	V_{DS} = 15V, I_D = 5.8A V_{DS} = 15V, I_D = 7.8A	Q1 Q2	– –	16 27	– –	S
Diode Forward Voltage	V_{SD}	I_S = 1.7A, V_{GS} = 0V	Q1, Q2	–	0.75	1.2	V
Dynamic							
Total Gate Charge	Q_g	**Q1** V_{DS} = 15V, V_{GS} = 5V I_D = 5.8A **Q2** V_{DS} = 15V, V_{GS} = 5V I_D = 10A	Q1 Q2	– –	8.1 20	11 27	nC
Gate-Source Charge	Q_{gs}		Q1 Q2	– –	2.1 5.8	– –	
Gate-Drain Charge	Q_{gd}		Q1 Q2	– –	2.8 6.3	– –	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15V, R_L = 15Ω, I_D ≈ 1A, V_{GEN} = 10V, R_G = 6Ω	Q1 Q2	– –	7 10	14 20	ns
Rise Time	t_r		Q1 Q2	– –	6 10	12 20	
Turn-Off Delay Time	$t_{d(off)}$		Q1 Q2	– –	25 51	40 77	
Fall Time	t_f		Q1 Q2	– –	8 21	16 35	
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0V f = 1.0 MHz	Q1 Q2	– –	840 1885	– –	pF
Output Capacitance	C_{oss}		Q1 Q2	– –	150 325	– –	
Reverse Transfer Capacitance	C_{rss}		Q1 Q2	– –	80 180	– –	

Notes: (1) Surface mounted on FR4 board, t ≤ 10 sec.
(2) Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%

Switching Test Circuit



Switching Waveforms



Asymmetric N-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

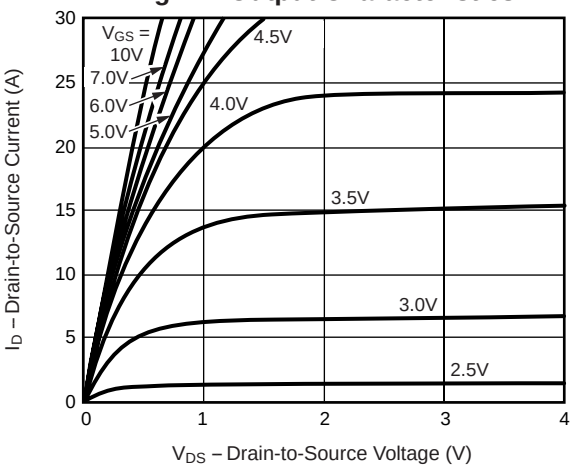


Fig. 2 – Transfer Characteristics

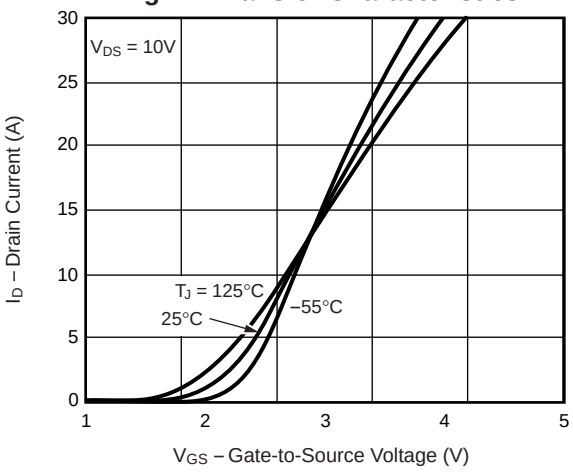


Fig. 3 – Threshold Voltage vs. Temperature

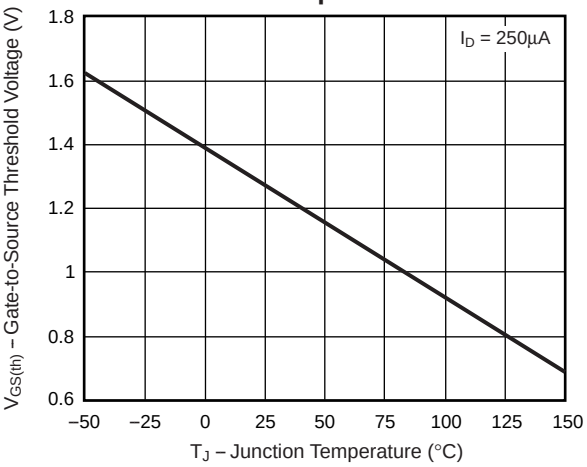


Fig. 4 – On-Resistance vs. Drain Current

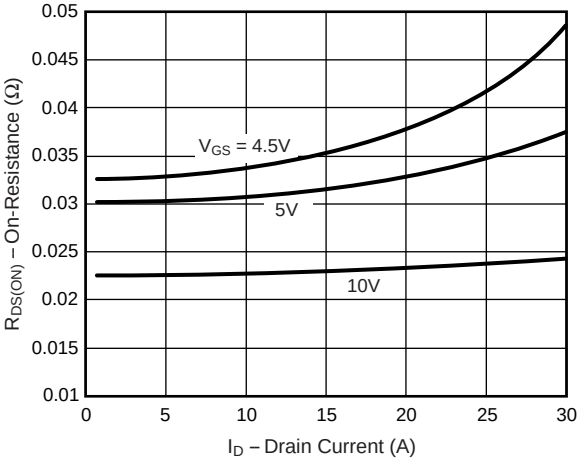
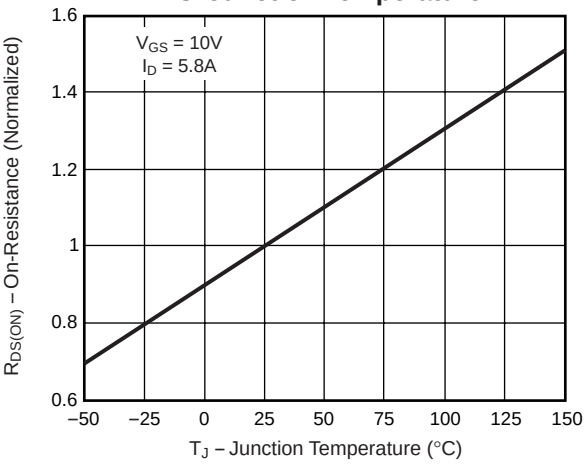


Fig. 5 – On-Resistance vs. Junction Temperature



Asymmetric N-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 6 – On-Resistance vs. Gate-to-Source Voltage

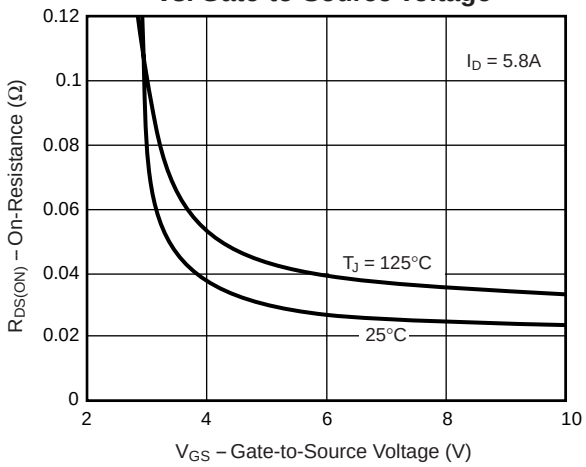


Fig. 7 – Gate Charge

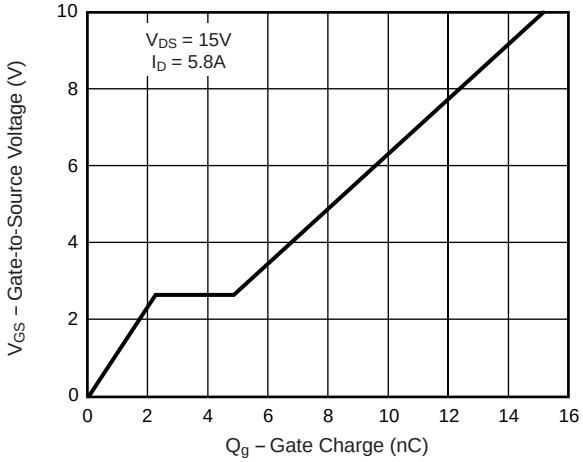


Fig. 8 – Capacitance

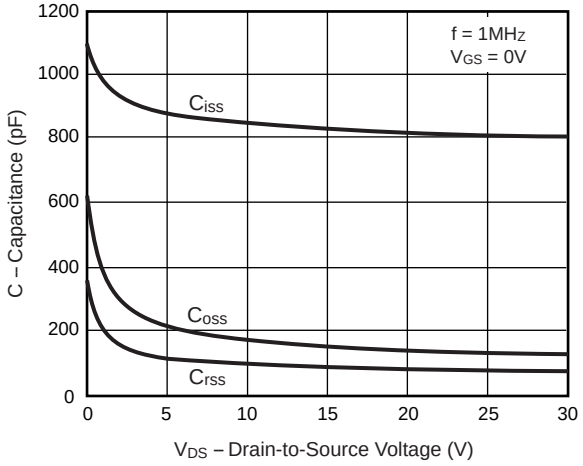
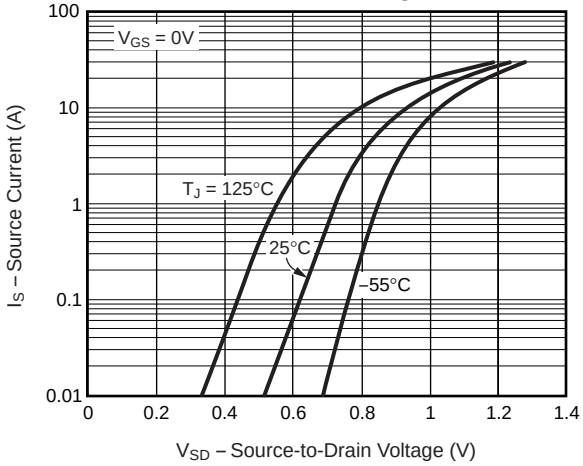


Fig. 9 – Source-Drain Diode Forward Voltage



Asymmetric N-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 10 – Breakdown Voltage vs. Junction Temperature

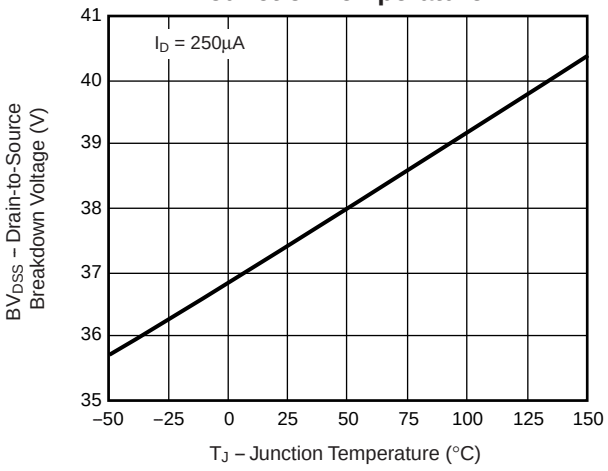


Fig. 11 – Thermal Impedance

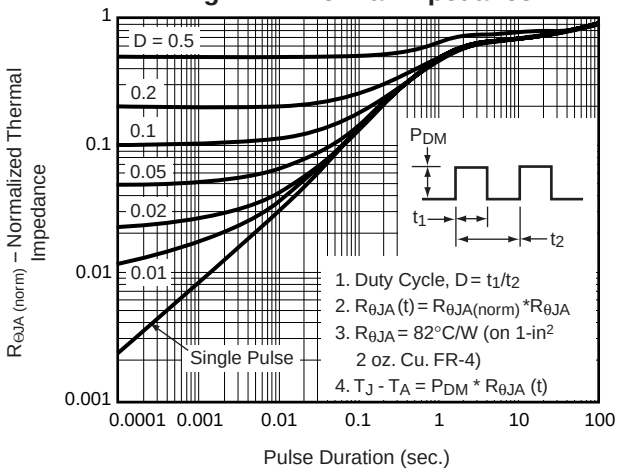


Fig. 12 – Power vs. Pulse Duration

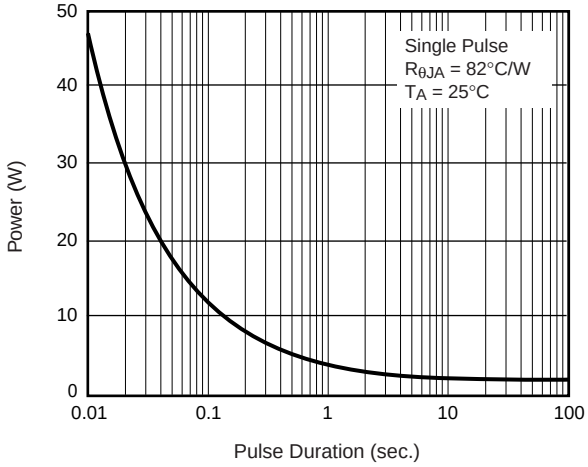
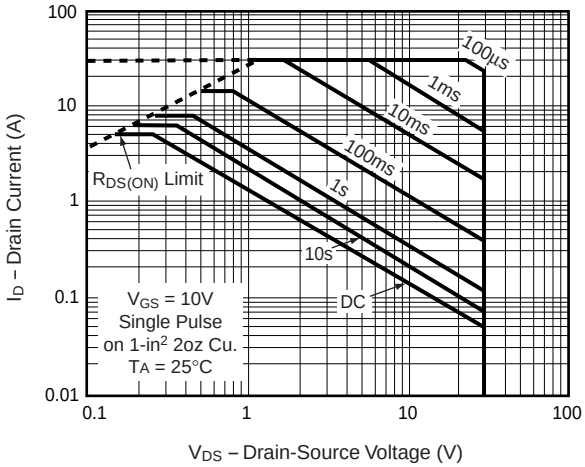


Fig. 13 – Maximum Safe Operating Area



Asymmetric N-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

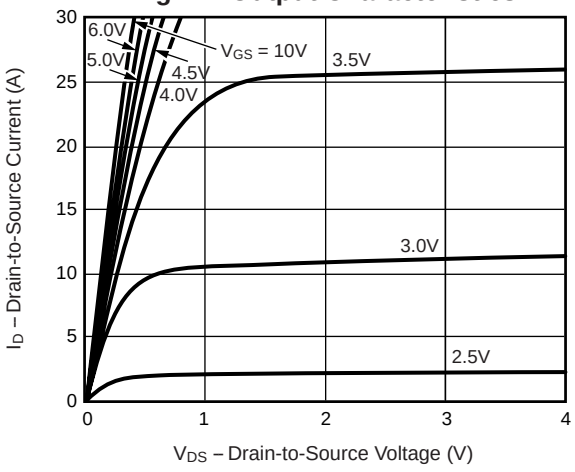
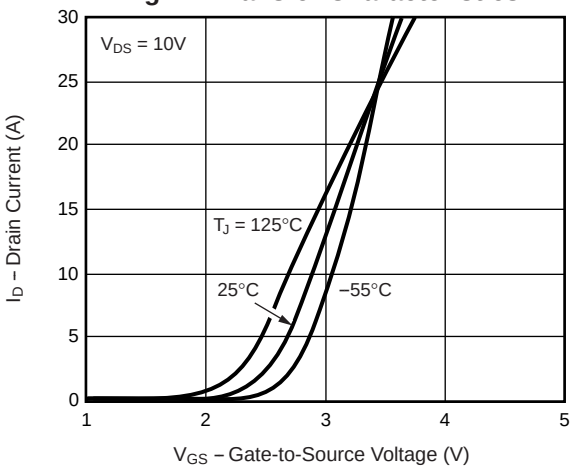


Fig. 2 – Transfer Characteristics



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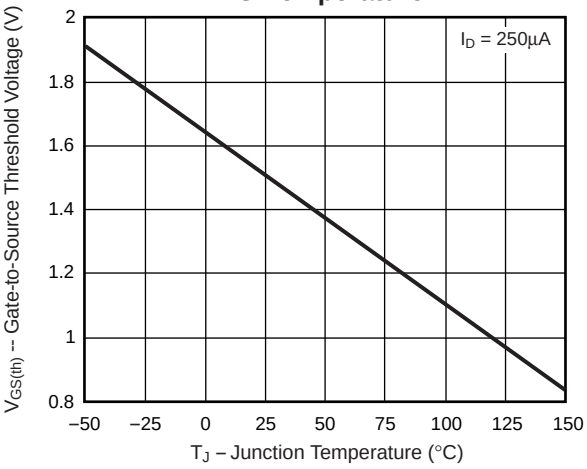


Fig. 4 – On-Resistance vs. Drain Current

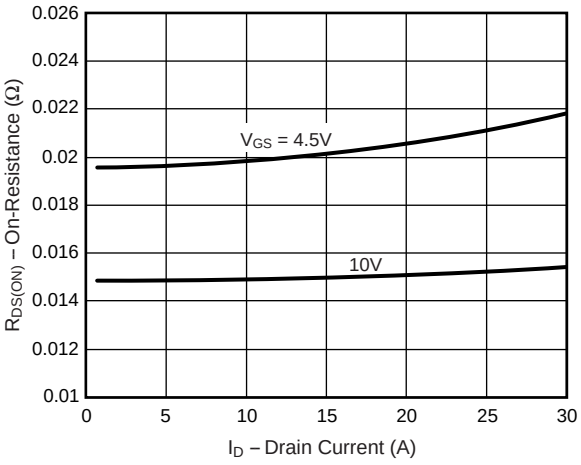
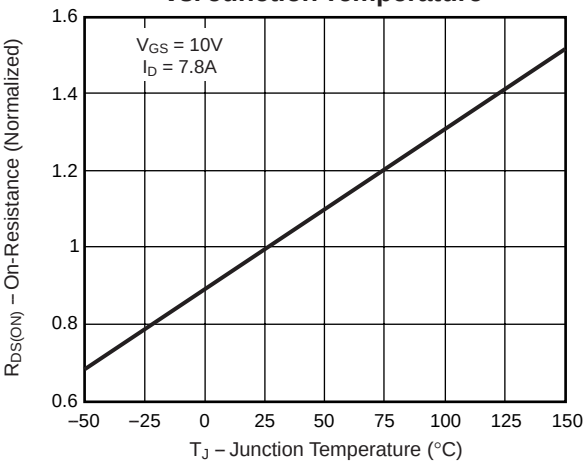


Fig. 5 – On-Resistance vs. Junction Temperature



Asymmetric N-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 6 – On-Resistance vs. Gate-to-Source Voltage

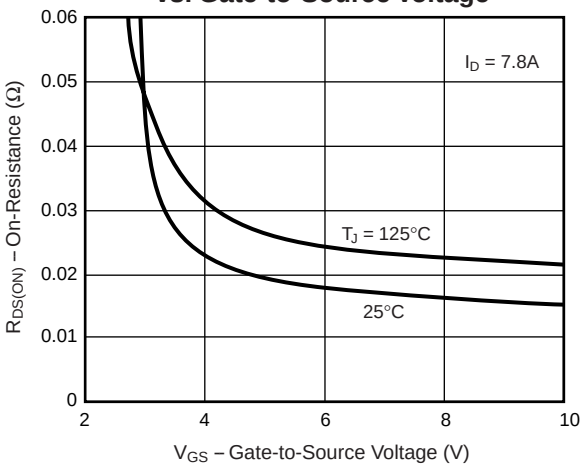


Fig. 7 – Gate Charge

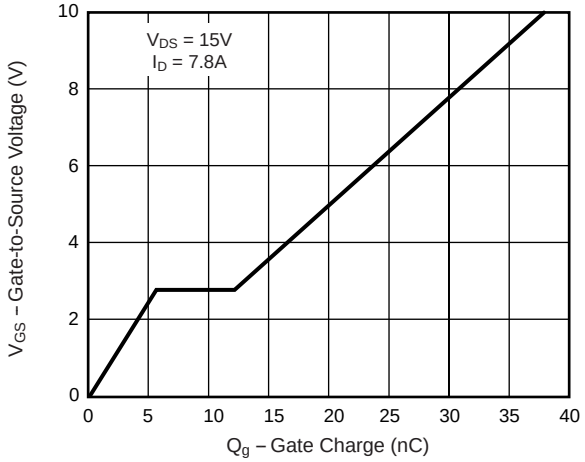
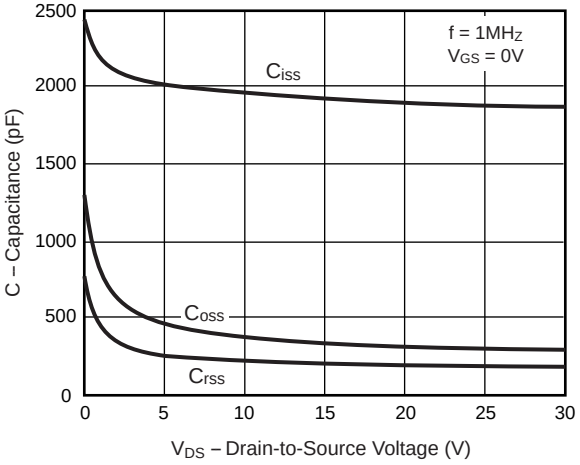


Fig. 8 – Capacitance



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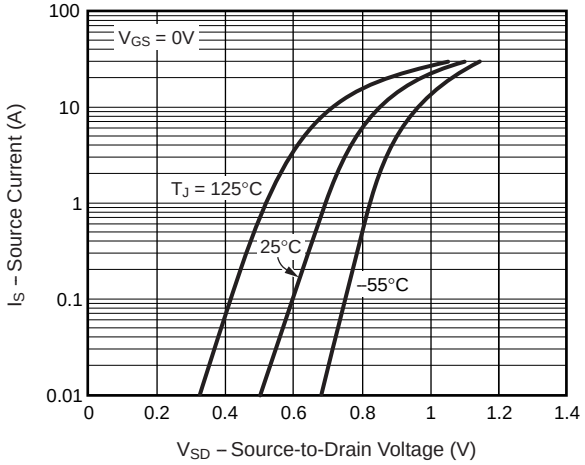


Asymmetric N-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 10 – Breakdown Voltage vs. Junction Temperature

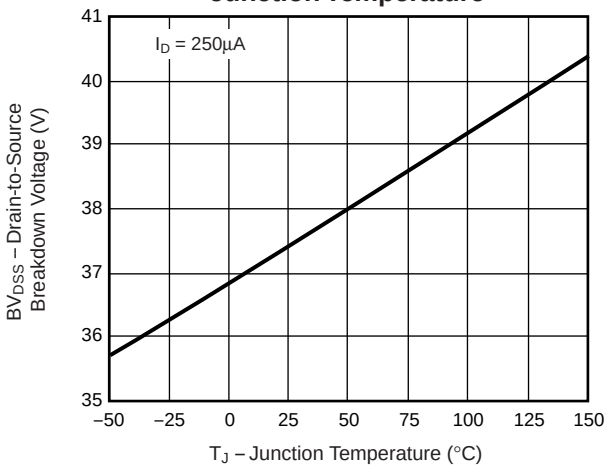
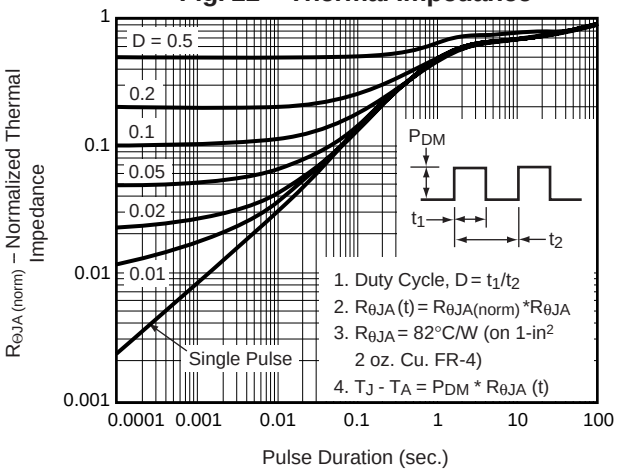


Fig. 11 – Thermal Impedance



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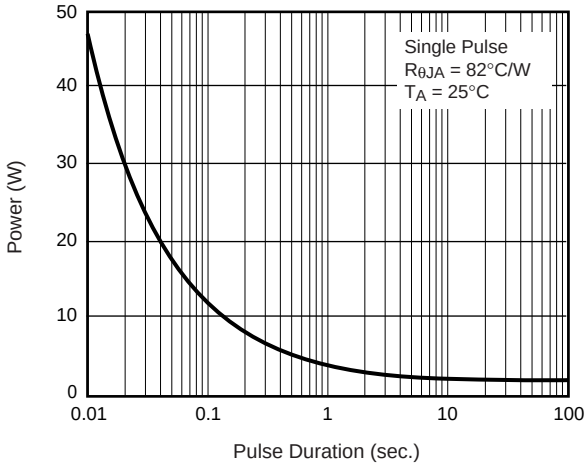

Fig. 13 – Maximum Safe Operating Area