agere systems

**Product Brief**
**June 2001**

# Gigabit Ethernet/Fast Ethernet POS-PHY Bridge

## Overview

The gigabit Ethernet (GbE)/fast Ethernet POS-PHY bridge enables system solutions to be created for two different applications. The first application involves transporting GbE frames or 10 Mbits/s/100 Mbits/s Ethernet frames over existing SONET/SDH rings or point-to-point connections. The second application involves transporting GbE or 10/100 Ethernet frames to and from the switch fabric. The SONET/SDH transport is provided using a combination of SONET/SDH and GbE/fast Ethernet standard products, together with an FPGA and stand-alone SDRAM devices. The transport over the switch fabric is provided using Agere Systems Inc.'s *PayLoadPlus*™ network processor chip set, GbE/fast Ethernet standard products together with an FPGA.

One of the benefits of this solution is the unification of all WAN and PSTN service deliveries over the same infrastructure, platforms, and fiber-access interfaces. Virtual private networks (VPNs) can also be implemented over optical networks having the reliability built into SONET/SDH systems. The solution allows transport of GbE/fast Ethernet traffic to and from the switch fabric.

The solution provided by Agere is an end-to-end hardware solution. This includes interconnection to both the switch fabric and the Ethernet networks, encapsulation of Ethernet frames into POS (packet-over-SONET) frames, ingress and egress packet buffering, error checking, and optional flow control across the fiber link and into the Ethernet network.

An intellectual property (IP) *VHDL** core is provided from Agere that targets *ORCA*® Series FPGAs and performs the GbE (or Ethernet/fast Ethernet) encapsulation into POS frames to interface to the Agere *PayLoadPlus* network processor chip set or to a SONET/SDH framer (for SONET/SDH systems). This IP core is provided along with all of the needed implementation scripts, test benches, and documentation to allow easy modification of the core to meet differing customer needs.

* *VHDL* is a registered trademark of Gateway Design Automation Corporation.

The supplied solution has been implemented for OC-48c networks but the architecture has been designed to allow for speed increases of the switch fabric (or SONET/SDH) and GbE networks by using faster standard products with modifications to the IP core solution.

## GbE/Fast Ethernet *PayLoadPlus* POS-PHY Bridge Features

The first application of the POS-PHY bridge is to encapsulate GbE/fast Ethernet frames into packet over SONET-physical layer level 3 (POS-PHY L3) format for connecting to Agere's *PayLoadPlus* network processor chip set. This allows transport of GbE/fast Ethernet traffic to and from the switch fabric. Figure 1 is a block diagram of this application.

- The network processor chip set consists of three devices; the fast pattern processor (FPP), the route switch processor (RSP), and the Agere system interface (ASI):
  - — The FPP provides the ingress data path and performs traffic data classification at wire speed rates. Data is identified, queued, and stored in external DRAM in complete protocol data units (PDUs) during first-pass processing. Second-pass processing is performed on complete PDUs and passed to the RSP with classification decisions.
  - — The RSP performs PDU modifications and applies traffic management algorithms on egress data.
  - — The ASI provides the host system interface for passing external function calls, local control register access, and policing management port functions.
- Provides asynchronous FIFO decoupled interfaces between the MAC transmit/receive FIFO ports and the FPP/RSP ingress/egress FIFO ports.
- Provides a communication interface between the ASI configuration bus and the control register CPU interface provided by the MAC devices.

## GbE/Fast Ethernet *PayLoadPlus* POS-PHY Bridge Features (continued)

- The GbE/fast Ethernet *PayLoadPlus* POS-PHY bridge solution consists of the following products:
  - — Agere's *PayLoadPlus* network processor chip set.
  - — A dual-channel GbE MAC device or octal 10/100 MACs.
  - — Agere's physical layer (SERDES) devices.
  - — An *ORCA* Series 4 FPGA (typically an OR4E6) with a *VHDL* IP core to implement the required interface functions. The programmability of these devices allows for easy modifications to the base architecture or the incorporation of other system functions in the same device.
- Base architecture allows modifications for switch fabric speed improvements to OC-192, Ethernet speed improvements to 10 GbE, and for increased GbE channels per OC-48 link.

## GbE/Fast Ethernet SONET/SDH POS-PHY Bridge Features

Optionally, the POS-PHY bridge can be used to encapsulate GbE/fast Ethernet frames into the SONET/SDH protocol using packet-over SONET physical layer level 3 (POS-PHY L3) format. In the future, interfaces for UTOPIA 3+ (PLATO) will also be available for interfacing to the TADM042G5 or TDAT042G5 devices. Figure 2 is a block diagram of this application.

- Performs all SONET/SDH section, line, and path termination functions.
- Encapsulates the GbE frame using either point-to-point protocol (PPP using byte-sync HDLC), simplified data link (SDL), or generic framing procedure (GFP).
- Provides two OC-24c POS interfaces to the SONET/SDH optical network, with each OC-24c carrying one of the two GbE data channels.
- Optionally, each GbE interface can be transported using two OC-12c POS links. Minor modifications to the current IP block are required for this solution and will be available as a follow-on IP core.
- Each SONET/SDH GbE/fast Ethernet POS-PHY bridge solution consists of the following products:
  - — Agere's TADM042G5 OC-48/Quad OC-12 SONET add/drop MUX interface device (for point-to-point connections, the TDAT042G5 device is used) or any industry-standard SONET/SDH framer with POS-PHY L3 interface.
  - — A dual-channel GbE MAC device or octal 10/100 MACs.
  - — Agere's physical layer (SERDES) devices.
  - — OC-48 MUX/deMUX (TTRN012G5 and TRCV012G5) and laser interface devices.
  - — Agere's LG1627BXC OC-48 SONET/SDH compliant lasers.
  - — An industry standard SDRAM.
  - — An *ORCA* Series 4 FPGA (typically an OR4E4) with a VHDL IP core to implement the required interface functions. The programmability of these devices allow for easy modifications to the base architecture or the incorporation of other system functions in the same device.
- Base architecture allows modifications for SONET/SDH speed improvements to OC-192, Ethernet speed improvements to 10 GbE, and for increased GbE channels per OC-48 SONET/SDH link.

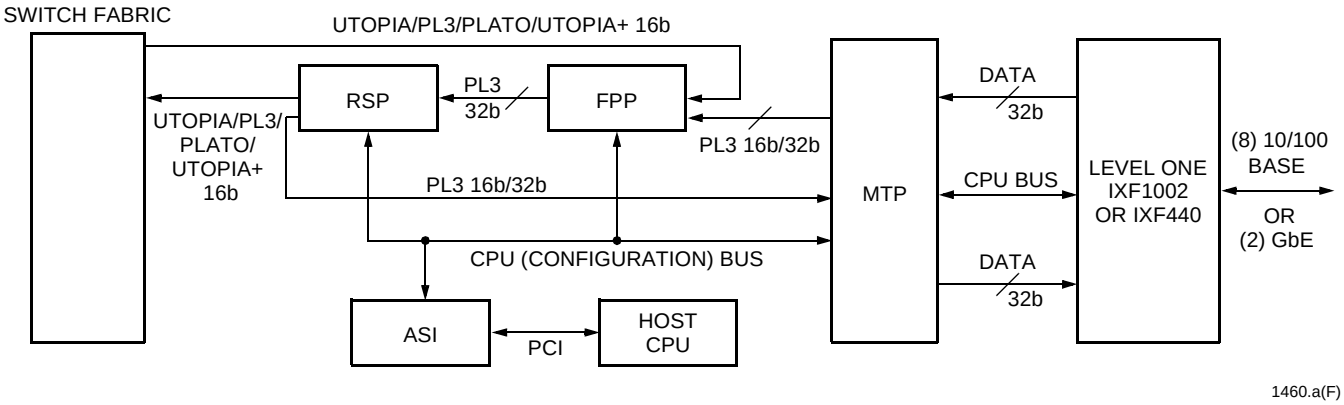


**Figure 1. GbE/Fast Ethernet POS-PHY Bridge Interfacing to *PayLoadPlus***

## GbE/Fast Ethernet *PayLoadPlus* POS-PHY Bridge Features (continued)

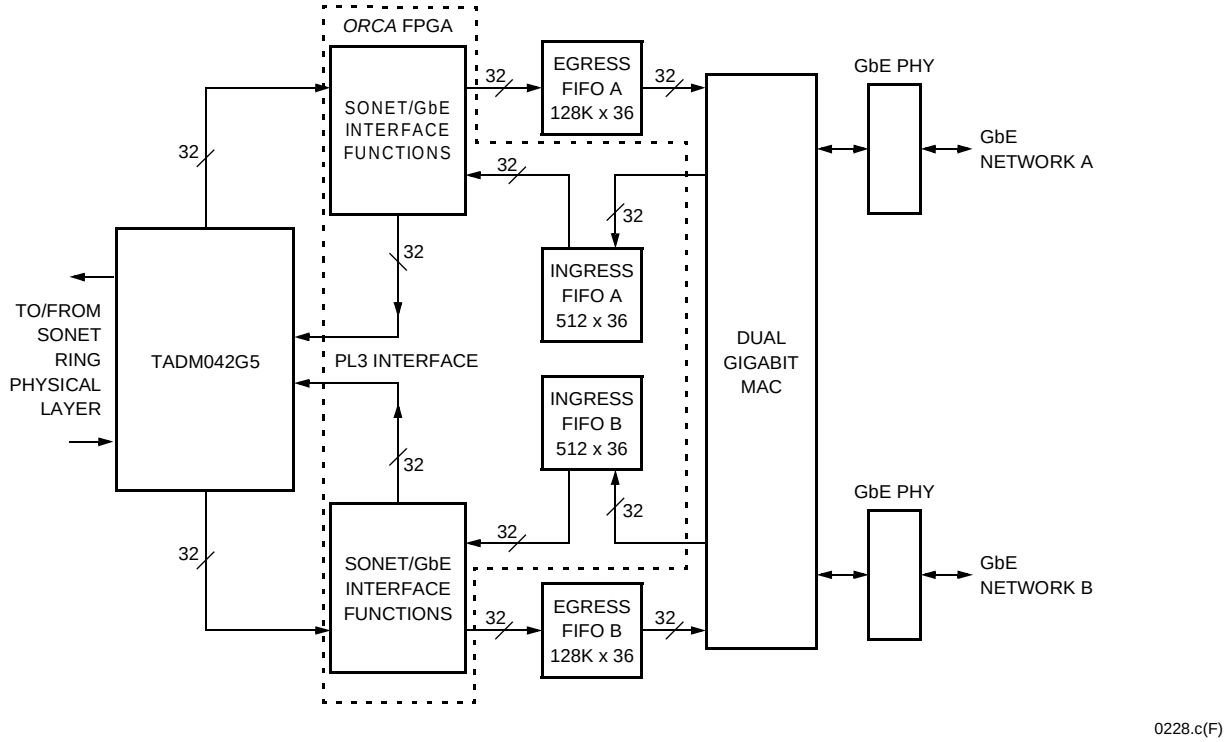


**Figure 2. GbE over SONET Block Diagram**

## Description

The detailed implementation of the *PayLoadPlus* system is shown in Figure 1. The FPGA portion of the design performs the interface function between the GbE/fast Ethernet controller devices and the *PayLoadPlus* network processor chip set.

The *PayLoadPlus* network processor chip set consists of three devices, the fast pattern processor (FPP), the route switch processor (RSP), and the Agere system interface (ASI). The FPP provides the ingress data path and performs traffic data classification at wire speed rates. Data is identified, queued, and stored in external DRAM in complete protocol data units (PDUs) during first-pass processing. Second-pass processing is performed on complete PDUs and passed to the RSP with classification decisions. The RSP performs PDU modifications and applies traffic management algorithms on egress data. The ASI provides the host system interface for passing external function calls, local control register access, and policing management port functions.

The dual-GbE/quad-10/100 Mbits/s Ethernet MAC performs interface functions to the Ethernet networks, including the handling of congestion by using industry-standard techniques such as PAUSE commands and XON/XOFF flow control. The physical layer devices interface to the Ethernet network physical transport medium.

The IP core in the FPGA devices performs all of the handshaking between the GbE/fast Ethernet media access controller (MAC) and the *PayLoadPlus* chip set (FPP and RSP) or the SONET/SDH device. Also included in the FPGA core is the handling of rate mismatches between the interconnected networks, control of the data buffering and flow control between the networks, and the discarding of errored packets received from the MAC before transmission across the SONET/SDH fiber or switch fabric interface. Other user-defined functions can also be easily integrated into any remaining gates of the FPGA devices.

## Description (continued)

For the SONET/SDH system, the FPGA connects via the POS-PHY L3 interface to a SONET/SDH device performing the needed SONET/SDH interface functions. These include section, line, and path overhead functions, pointer processing, automatic protection switch interfaces, and cross-connect support for transmit and receive of data engine payload functions, such as PPP, using HDLC or SDL, and POS-PHY L2 and L3 (or UTOPIA L2 and L3) physical interfaces, including packet support through POS extensions.

All devices are provisioned, monitored, and controlled through microprocessor interfaces to allow for easy in-system modifications. Low-level software drivers are also available for many of the standard products to ease system integration of these devices.

## Other Information

Product briefs, data sheets, application notes, and other information on many of the products used in the above system solutions are available from Agere. This solution is also highlighted on the networks and communications website at:

**http://www.agere.com/netcom**

## Ordering Information

Contact your local Agere sales representative for ordering information. The IP core is a member of the Smart Silicon family of Agere IP cores, and an IP core license agreement is required for the *VHDL* IP kit. The license agreement is for unlimited reuse of the solution in your company, but will limit the implementation of the IP core described above to Agere devices, either as standard products, standard-cell ASICs, FPGAs, or FPSCs (combined FPGA/standard-cell ASIC devices).

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