209-Bump BGA
Commercial Temp
Industrial Temp

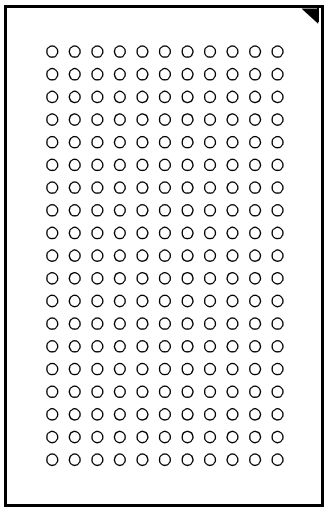
18Mb Σ2x2B4 DDR Separate I/O SRAM

250 - 333 MHz
1.8 V V_{DD}
1.8 V and 1.5 V I/O

Features

- SigmaRAM™ JEDEC standard pinout and package
- Dual Double Data Rate interface
- Echo Clock outputs track data output drivers
- Byte Write controls sampled at data in time
- 2 user-programmable chip enable inputs for easy depth expansion
- Burst of 4 Read and Write
- 1.8 V +150/–100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ mode pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 209-bump, 14 mm x 22 mm, 1 mm bump pitch BGA package
- Pin compatible with future 32M, 64M and 128M devices

	- 333	-300	-250
tKHKH	3.0 ns	3.3 ns	4 ns
tKHQV	1.6 ns	1.8 ns	2.1 ns



Bottom View

209-Bump, 14 mm x 22 mm BGA
1 mm Bump Pitch, 11 x 19 Bump Array

SigmaRAM Family Overview

GS8180D18B are built in compliance with the SigmaRAM pinout standard for Separate I/O synchronous SRAMs. They are 18,874,368-bit (18Mb) SRAMs. These are the first in a family of wide, very low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

Separate I/O SigmaRAMs are offered in a number of configurations. Some emulate and enhance other synchronous separate I/O SRAMs. A higher performance SDR (Single Data Rate) Burst of 2 version is also offered. The logical differences between the protocols employed by these RAMs hinge mainly on various combinations of address bursting, output data registering, and write cueing. Like the Common I/O family of SigmaRAMs, Separate I/O SigmaRAMs allow a user to implement the interface protocol best suited to the task at hand.

Clocking and Addressing Schemes

A Σ2x2B4 SigmaRAM is a synchronous device. It employs two input register clock inputs, K and $\overline{K}$. K and $\overline{K}$ are differential inputs to a single differential clock input buffer. The device also allows the user to manipulate the output register clock inputs quasi independently with the C and $\overline{C}$ clock inputs. C and $\overline{C}$ are also differential inputs. If the C clocks are tied high, the K clocks are routed internally to fire the output registers instead. Each Σ2x2B4 SigmaRAM also supplies Echo Clock outputs, CQ and $\overline{CQ}$, that are synchronized with read data output. When used in a Source Synchronous clocking scheme these Echo Clock outputs can be used to fire input registers at the data's destination.

Because Separate I/O Σ2x2B4 RAMs always transfer data in four packets, A0 and A1 are internally set to 0 for the first read or write transfer, and automatically incremented by 1 for the next transfers. Since the LSBs are tied off internally, the address field of a Σ2x2B4 RAM is always two address pins less than the advertised index depth (e.g., the 1M x 18 has a 256K addressable index).

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8180D18 Pinout

1M x 18 Separate I/O—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	Db1	Db2	A	E1	A (16M)	MCL	A (8M)	E2	A	NC	NC
B	Db3	Db4	$\overline{Bb}$	NC	A	$\overline{W}$	A	NC	NC	NC	NC
C	Db5	Db6	NC	NC	NC (128M)	$\overline{R}$	A	NC	$\overline{Ba}$	NC	NC
D	Db7	Db8	V_{SS}	VREF	NC	MCL	NC	VREF	V_{SS}	NC	NC
E	Db9	Qb1	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
F	Qb3	Qb2	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC
G	Qb5	Qb4	V_{DDQ}	V_{DDQ}	V_{DD}	EP1	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
H	Qb7	Qb6	V_{SS}	V_{SS}	V_{SS}	EP2	V_{SS}	V_{SS}	V_{SS}	NC	NC
J	Qb9	Qb8	V_{DDQ}	V_{DDQ}	V_{DD}	M4	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
K	CQ2	$\overline{CQ2}$	K	$\overline{K}$	V_{SS}	MCL	V_{SS}	$\overline{C}$	C	$\overline{CQ1}$	CQ1
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	M2	V_{DD}	V_{DDQ}	V_{DDQ}	Qa8	Qa9
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	M3	V_{SS}	V_{SS}	V_{SS}	Qa6	Qa7
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	Qa4	Qa5
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	Qa2	Qa3
R	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	Qa1	Da9
T	NC	NC	V_{SS}	VREF	NC	MCL	NC	VREF	V_{SS}	Da8	Da7
U	NC	NC	NC	A	NC (64M)	A	NC (32M)	A	NC	Da6	Da5
V	NC	NC	A (2M)	A	A	MCL	A	A	A (4M)	Da4	Da3
W	NC	NC	TMS	TDI	A	MCL	A	TDO	TCK	Da2	Da1

Rev 11

11 x 19 Bump BGA—14 x 22 mm2 Body—1 mm Bump Pitch—MS-028vBC

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Pin Description Table

Pin Location	Symbol	Description	Type	Comments
A3, A5, A7, A9, B5, B7, U4, U6, U8, V3, V4, V5, V6, V7, V8, V9, W5, W7	A	Address	Input	All Versions
C7	A	Address	Input	x18 Versions
K3	K	Clock	Input	Active High
K4	$\overline{K}$	Clock	Input	Active Low
K9	C	Output Register Clock	Input	Active High
K8	$\overline{C}$	Output Register Clock	Input	Active Low
K1, K11	CQ	Echo Clock	Output	Active High
K2, K10	$\overline{CQ}$	Echo Clock	Output	Active Low
W11, W10, V11, V10, U11, U10, T11, T10, R11	Da1 - Da9	Byte a Data Input	Input	—
A1, A2, B1, B2, C1, C2, D1, D2, E1	Db1 - Db9	Byte b Data Input	Input	x18 Version
A10, A11, B10, B11, C10, C11, D10, D11, E11 R2, P2, P1, N2, N1, M2, M1, L2, L1 E10, F10, F11, G10, G11, H10, H11, J10, J11 W1, W2, V1, V2, U1, U2, T1, T2, R1	NC	No Connect	—	x18 Version
R10, P10, P11, N10, N11, M10, M11, L10, L11	Qa1 - Qa9	Byte a DataOutput	Output	—
E2, F2, F1, G2, G1, H2, H1, J2, J1	Qb1 - Qb9	Byte b DataOutput	Output	x18 Version
B6	$\overline{W}$	Write Enable	Input	Active Low
C9, B3	$\overline{Ba}$, $\overline{Bb}$	Byte Enable	Input	Active Low, x18 Version
B8, C4	NC	No Connect	Input	x18 Version
C6	$\overline{R}$	Read Enable	Input	Active Low
A4, A8	E1 & E2	Chip Enable	Input	Programmable Active High or Low
G6, H6	EP1 & EP2	Chip Enable Program Pin	Input	—
F6	ZQ	Output Impedance Control	Input	—
W9	TCK	Test Clock	Input	Active High
W4	TDI	Test Data In	Input	—
W8	TDO	Test Data Out	Output	—
W3	TMS	Test Mode Select	Input	—
L6, M6, J6	M2, M3 & M4	Mode Control Pins	Input	—
N6	MCH	Must Connect High	Input	Active High
A6, D6, K6, P6, T6, W6	MCL	Must Connect Low	Input	Active Low

Pin Description Table

Pin Location	Symbol	Description	Type	Comments
B4, B9, C3, C5, C8, D5, D7, T5, T7, U3, U5, U7, U9	NC	No Connect	—	All Versions
E5, E6, E7, G5, G7, J5, J7, L5, L7, N5, N7, R5, R6, R7	V_{DD}	Core Power Supply	Input	1.8 V Nominal
E3, E4, E8, E9, G3, G4, G8, G9, J3, J4, J8, J9, L3, L4, L8, L9, N3, N4, N8, N9, R3, R4, R8, R9	V_{DDQ}	Output Driver Power Supply	Input	1.8 V or 1.5 V Nominal
D4, D8, T4, T8	VREF	Input Buffer Reference Voltage	Input	—
D3, D9, F3, F4, F5, F7, F8, F9, H3, H4, H5, H7, H8, H9, K5, K7, M3, M4, M5, M7, M8, M9, P3, P4, P5, P7, P8, P9, T3, T9	V_{SS}	Ground	Input	—

Note: NC = Not Connected to die or any other pin

Background

Separate I/O SigmaRAMs have been designed to be closely related to Common I/O SigmaRAMs in pinout and overall architecture. The similarities give Separate I/O SigmaRAMs a cost advantage by allowing users and vendors to reuse supporting infrastructure and design elements. Separate I/O SigmaRAMs come in Single and two Double Data Rate configurations. Because they are designed to operate with both the input data pins and the output data pins operating at full speed all the time, Separate I/O SigmaRAMs produce twice the bandwidth of Common I/O SRAMs of the same speed and output bus width. But because the bandwidth of a memory device is set by the architecture and performance of the core array, the bandwidth available from each port of a Separate I/O SRAM is half the bandwidth available from the single port of an otherwise equivalent Common I/O SRAM.

Separate I/O SRAMs, from a system architecture point of view, are attractive in applications where alternating reads and writes are needed. Therefore, the SigmaRAM Separate I/O interface and truth table are optimized for alternating reads and writes. Separate I/O SRAMs are unpopular in applications where multiple reads or multiple writes are needed because burst read or write transfers from Separate I/O SRAMs cut the RAM's bandwidth in half.

SigmaRAM Bandwidth

Configuration			Clock Freq (MHz)	Address Freq (MHz)	Data Freq (MHz)	Data Bandwidth			
						x18	x36	x72	Units
Common I/O	SDR	Σ1x1	333	333	333	6	12	24	Gb/s
Common I/O	DDR	Σ1x2	333	333	**666**	12	24	48	Gb/s
Separate I/O	SDR	Σ2x1B2	333	333	333	12	24	-	Gb/s
Separate I/O	DDR	Σ2x2B2	**167**	333	333	12	24	-	Gb/s
Separate I/O	DDR	Σ2x2B4	333	333	**666**	24	48	-	Gb/s

A Separate I/O SigmaRAM can begin an alternating sequence of reads and writes with either a read or a write. In order for any separate I/O SRAM that shares a common address between it's two ports to keep both ports running all the time, the RAM must implement some sort of burst transfer protocol. The burst must be at least long enough to cover the time the opposite port is receiving instructions on what to do next. The rate at which a RAM can accept a new random address is the most fundamental performance metric for the RAM. Each of the three Separate I/O SigmaRAMs support the same address rate because random

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address rate is determined by the internal performance of the RAM and they are all based on the same internal circuits. Differences between the truth tables of the different Separate I/O SigmaRAMs, or any other Separate I/O SRAMs, follow from differences in how the RAM's interface is contrived to interact with the rest of the system. Each mode of operation has it's own advantages and disadvantages. The user should consider the nature of the work to be done by the RAM to evaluate which version is best suited to the application at hand.

Sigma 2xn Mode Selection Truth Table Standard

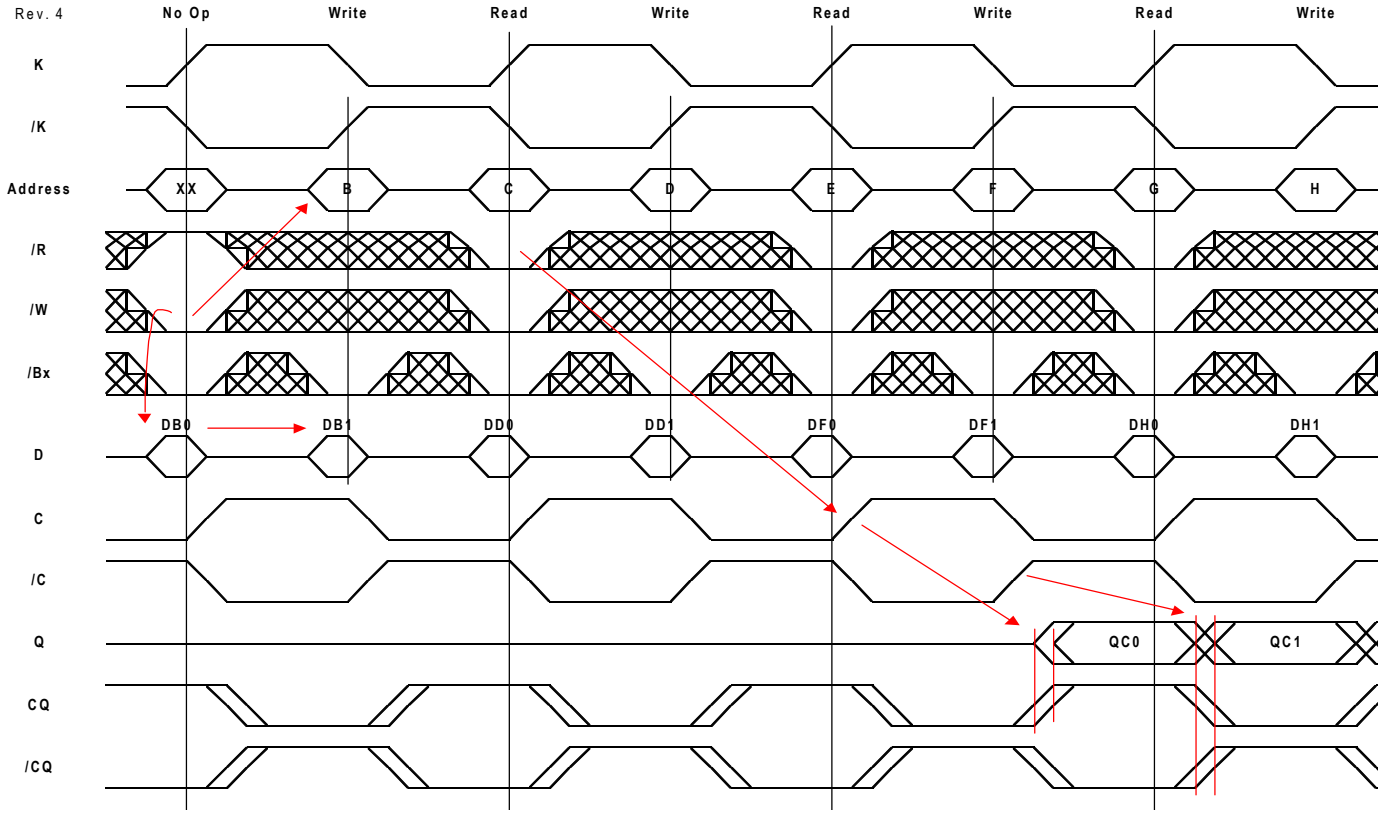
M2	M3	M4	Name	Function	In This Data Sheet?
0	0	0		RFU	n/a
0	0	1		RFU	n/a
0	1	0		RFU	n/a
0	1	1	Σ2x2B4	Double Data Rate - Burst of 4	Yes
1	0	0		RFU	n/a
1	0	1		RFU	n/a
1	1	0	Σ2x1B2	Late Write, Pipelined Read	No
1	1	1	Σ2x2B2	Double Data Rate - Burst of 2	No

Although the Separate I/O SigmaRAM family of pinouts has been designed to support Single and Double Data Rate options, not all SigmaRAM implementations will support both protocols. The following timing diagrams provide a quick comparison between the SDR and DDR protocol options available in the context of the Separate SigmaRAM standard. This particular data sheet covers theDouble Data Rate Burst of 4 (Σ2x2B4) Separate I/O SigmaRAM.

The character of the applications for fast synchronous SRAMs in networking systems are extremely diverse. SigmaRAMs have been developed to address the diverse needs of the networking market in a manner that can be supported with a unified development and manufacturing infrastructure. SigmaRAMs address each of the bus protocol options commonly found in networking systems.

Separate I/O SigmaRAM Family Mode Comparison

Σ2x2B2 - Double Data Rate, Burst of 2



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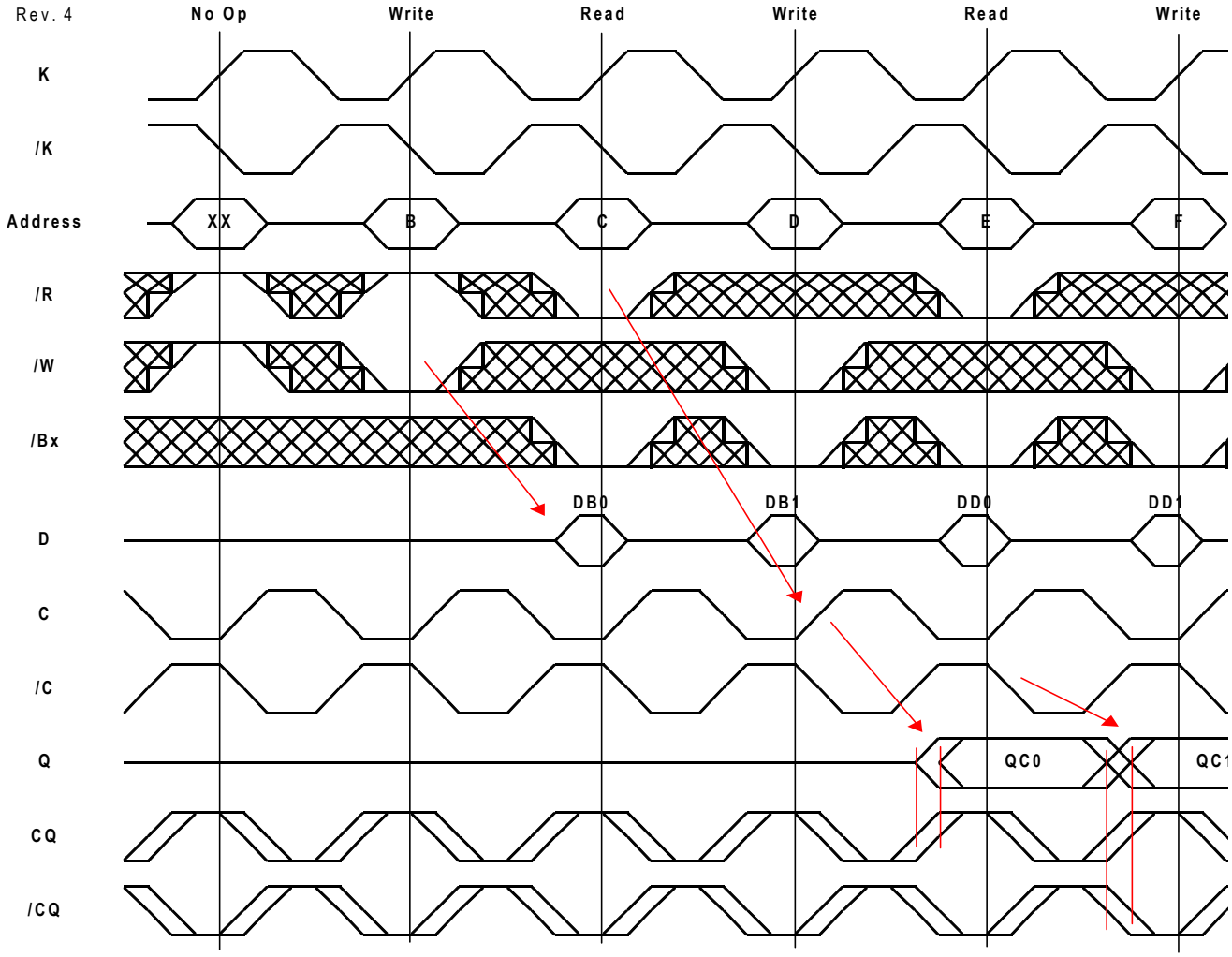
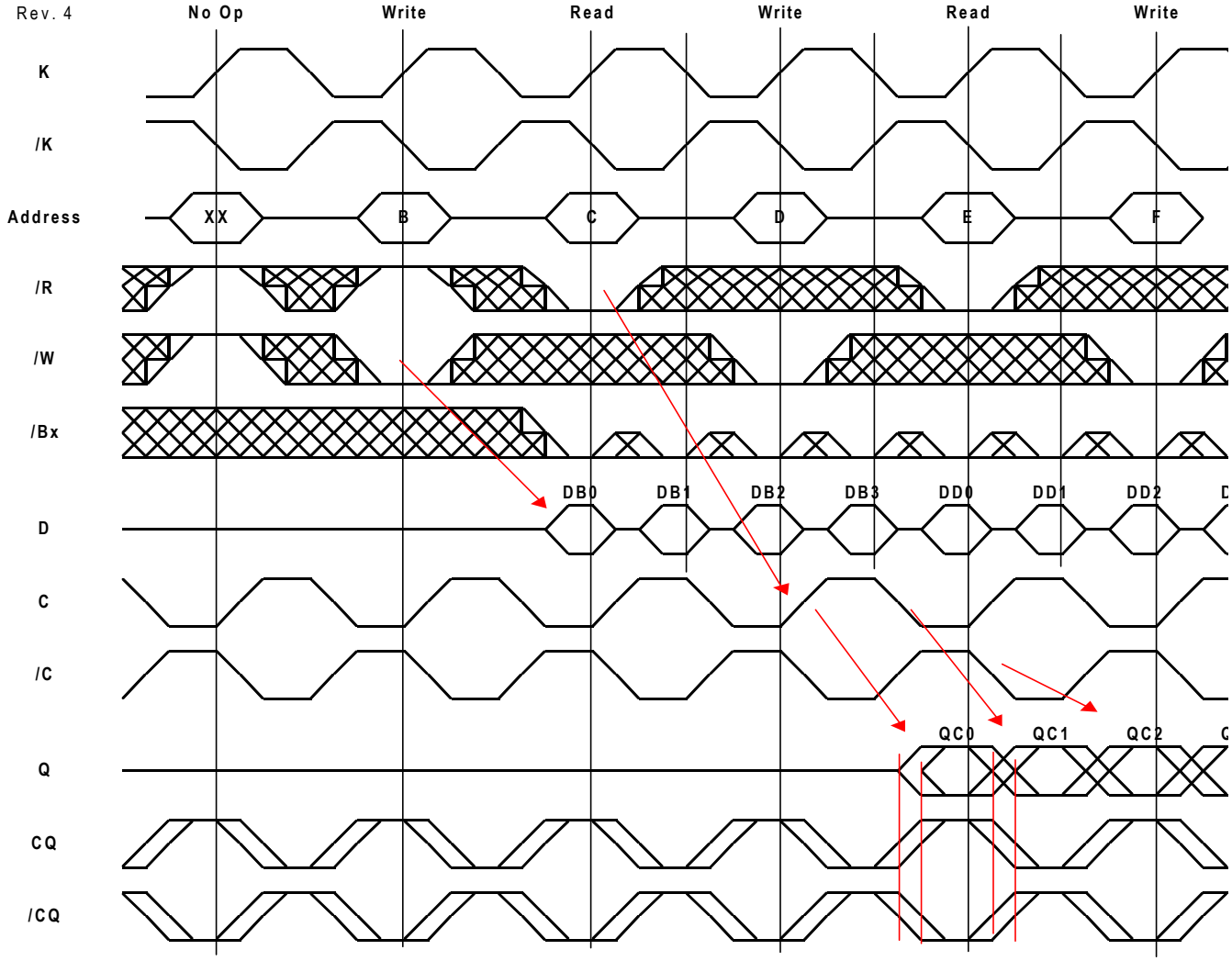
Σ2x1B2 - Single Data Rate, Burst of 2



Σ2x2B4 - Double Data Rate, Burst of 4



Alternating Read-Write Operations

Separate I/O SigmaRAMs follow a few simple rules of operation.
- Read or Write commands issued on one port are never allowed to interrupt a operation in progress on the other port.
- Read or Write data transfers in progress may not be interrupted and re-started.
- A Read of a given address location immediately after the location has just been written produces the just-written data. (i.e. SigmaRAMs are “coherent”.)
- $\overline{R}$ and $\overline{W}$ high always deselects the RAM but does not disable the CQ or $\overline{CQ}$ output pins.

-ONLY deactivation of the RAM via E1 and/or E2 (a Bank Deselect) deactivates the Echo Clock Outputs.

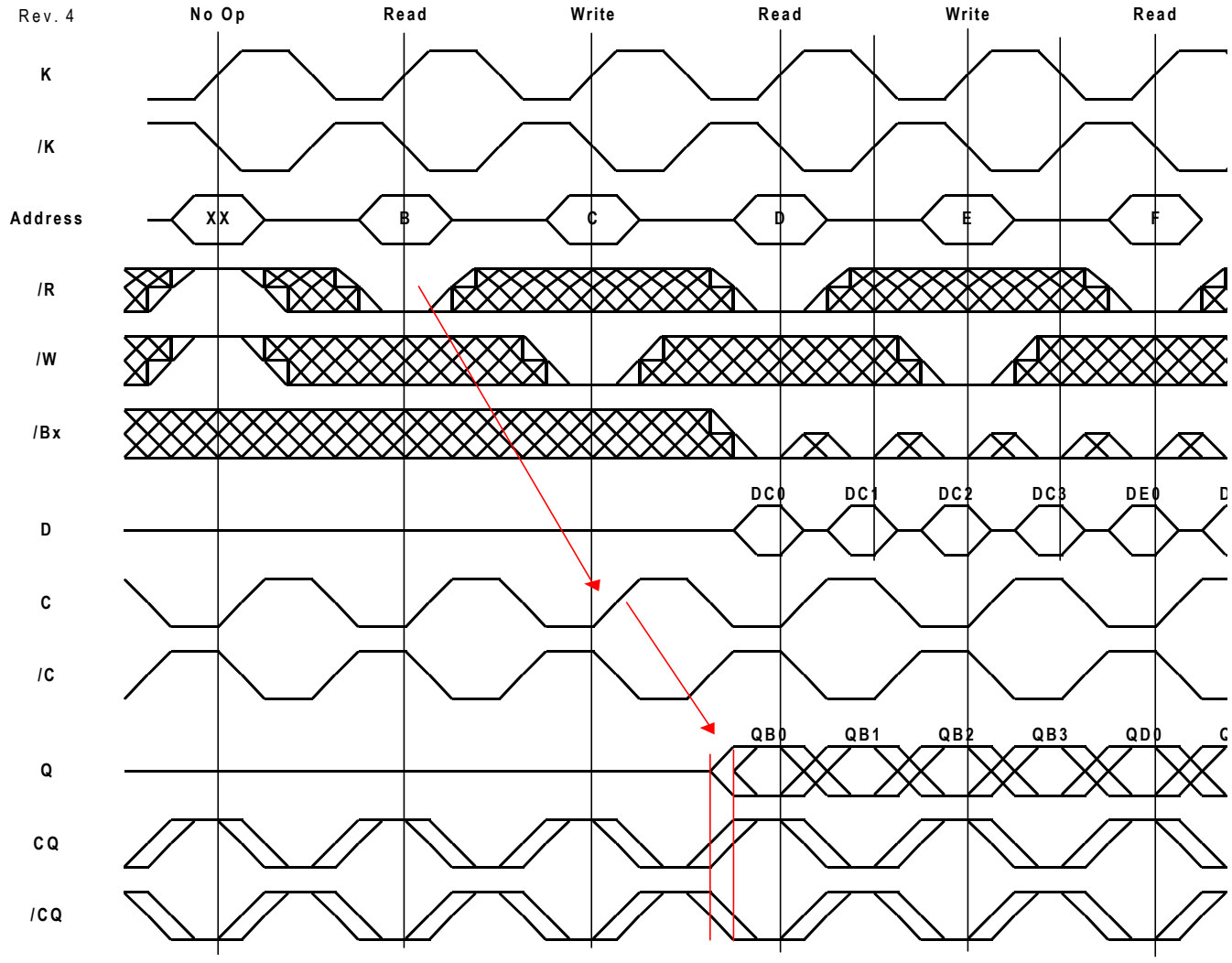
- All address, data, and control inputs (with the exception of EP1, EP2, and the mode pins, M2–M4) are sampled on clock edges.

In order to enforce these rules, each RAM combines present state information with command inputs. See the Truth Table for details.

Σ2x2B4 SigmaRAM DDR Read

The status of the Address Input, $\overline{W}$, $\overline{R}$, E1 and E2 pins are sampled at each rising edge of K. $\overline{W}$ and $\overline{R}$ high causes chip disable. A low on the Read Enable-bar pin, $\overline{R}$, begins a read cycle. $\overline{W}$ is always ignored if $\overline{R}$ is sampled low. $\overline{R}$ is always ignored if the previous command loaded was a read command. The four resulting data output transfers begin after the next rising edge of the K clock. Data is clocked out by next four rising and falling edges of the C clock. "Bank Select" device activation is accomplished by asserting both of the Chip Enable inputs (E1, and E2) true. A Bank Selected RAM will produce active Echo Clock (CQ and $\overline{CQ}$) outputs. Deassertion of any one of the Enable inputs (E1 or E2) will "Bank Deselect" the device and tri-state the Echo Clock outputs.

Σ2x2B4 Double Data Rate Separate I/O SigmaRAM First Read



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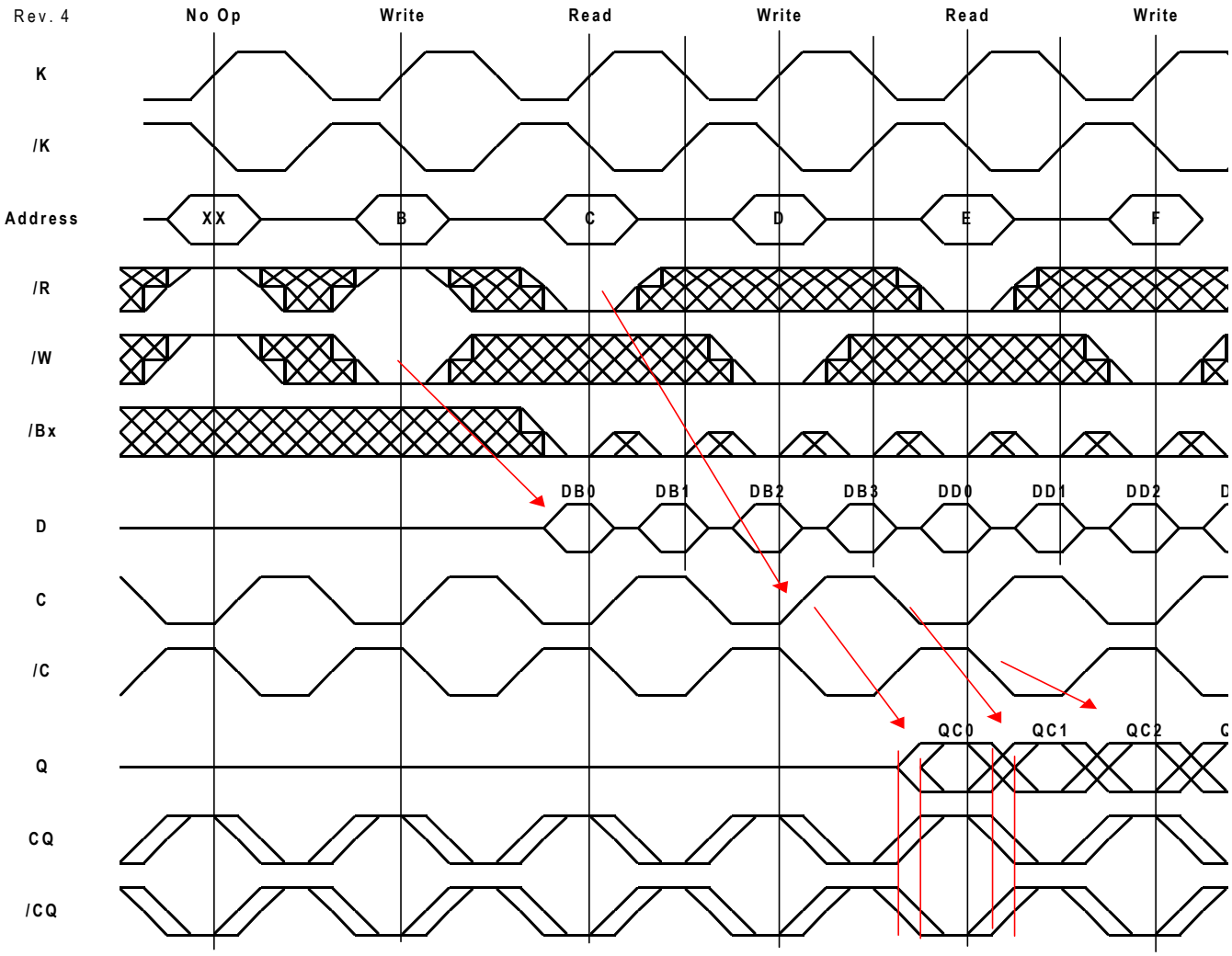
Σ2x2B4 SigmaRAM DDR Write

The status of the Address Input, $\overline{W}$, $\overline{R}$, E1 and E2 pins are sampled at each rising edge of K. $\overline{W}$ and $\overline{R}$ high causes chip disable. A low on the Write Enable-bar pin, $\overline{W}$, and a high on the Read Enable-bar pin, $\overline{R}$, begins a write cycle. $\overline{W}$ is always ignored if $\overline{R}$ is sampled low. $\overline{W}$ is always ignored if the previous command was a write command. Data is clocked in by the next rising edge of K, the rising edge of $\overline{K}$ after that, the rising edge of K and finally by the next rising edge of $\overline{K}$. "Bank Select" device activation is accomplished by asserting both of the Chip Enable inputs (E1, and E2) true. A Bank Selected RAM will produce active Echo Clock (CQ and $\overline{CQ}$) outputs. Deassertion of any one of the Enable inputs (E1 or E2) will "Bank Deselect" the device and inhibit write cycles.

Σ2x2B4 Double Data Rate Separate I/O SigmaRAM First Write



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Special Functions

Byte Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g. $\overline{B}a$ controls Da0 - Da9 inputs) will inhibit the storage of that particular byte, leaving the whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 4 beat data transfer. The x18 version of the RAM, for example, may write 72 bits in association with each address loaded. Any 9 bit byte may be masked in any write sequence.

Example x18 RAM Write Sequence using Byte Write Enables

Data In Sample Time	$\overline{B}a$	$\overline{B}b$	Da1 - Da9	Db1 - Db9
Beat 1	0	1	Data In	Don't Care
Beat 2	1	0	Don't Care	Data In
Beat 3	0	0	Data In	Data In
Beat 4	1	0	Don't Care	Data In

Resulting Write Operation

Byte 1 Da1 - Da9	Byte 2 Db1 - Db9	Byte 3 Da1 - Da9	Byte 4 Db1 - Db9	Byte 5 Da1 - Da9	Byte 6 Db1 - Db9	Byte 7 Da1 - Da9	Byte 8 Db1 - Db9
Written	Unchanged	Unchanged	Written	Written	Written	Unchanged	Written

Output Register Control

Separate I/O SigmaRAMs offer two mechanisms for controlling the output data registers. Typically control is handled by the Output Register Clock inputs C and $\overline{C}$. The Output Register Clock inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K clock. If the C and $\overline{C}$ clock inputs are tied high, the RAM reverts to K and $\overline{K}$ control of the outputs, allowing the RAM to function as a conventional pipelined read SRAM.

Echo Clock

SigmaRAMs feature Echo Clocks, CQ1,CQ2, $\overline{CQ1}$, and $\overline{CQ2}$ that track the performance of the output drivers. The Echo Clocks are delayed copies of the Output Register clock, C and $\overline{C}$. Echo Clocks are designed to track changes in output driver delays due to variance in die temperature and supply voltage. The Echo Clocks are designed to fire with the rest of the data output drivers. SigmaRAMs provide both in-phase, or true, Echo Clock outputs (CQ1 and CQ2) and inverted Echo Clock outputs ($\overline{CQ1}$ and $\overline{CQ2}$).

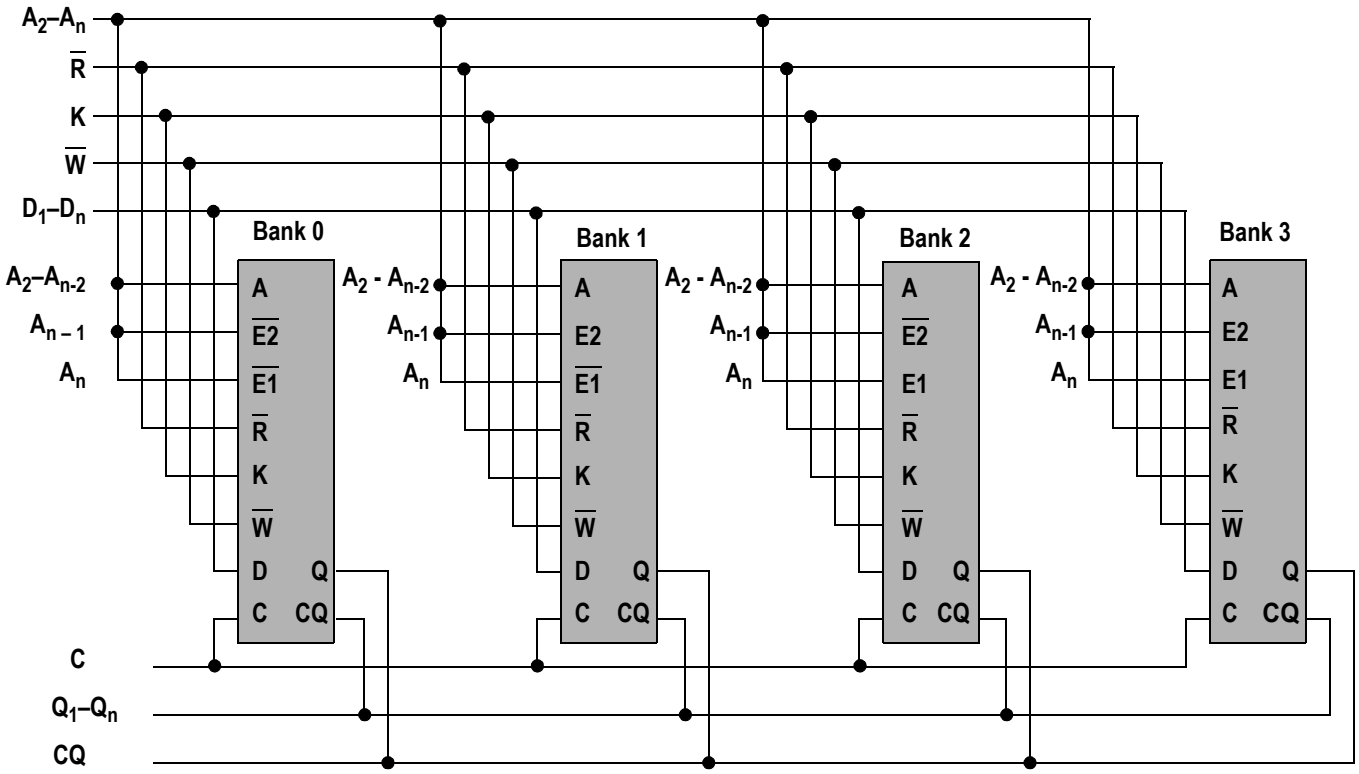
It should be noted that deselection of the RAM via E1 and E2 also deselects the Echo Clock output drivers. Echo Clocks are always active unless deselected by E1 or E2. The deselection of Echo Clock drivers is always pipelined to the same degree as output data. **Neither inhibiting reads via holding R high, nor deselection of the RAM via holding R and W high will deactivate the Echo Clocks.**

Programmable Enables

SigmaRAMs feature two user-programmable chip enable inputs, E1 and E2. The sense of the inputs, whether they function as active low or active high inputs, is determined by the state of the programming inputs, EP1 and EP2. For example, if EP1 is held at V_{DD}, E1 functions as an active high enable. If EP1 is held to V_{SS}, E1 functions as an active low chip enable input.

Programmability of E1 and E2 allows four banks of depth expansion to be accomplished with no additional logic. By programming the enable inputs of four SigmaRAMs in binary sequence (00, 01, 10, 11) and driving the enable inputs with two address inputs, four SigmaRAMs can be made to look like one larger RAM to the system.

Example Four Bank Depth Expansion Schematic

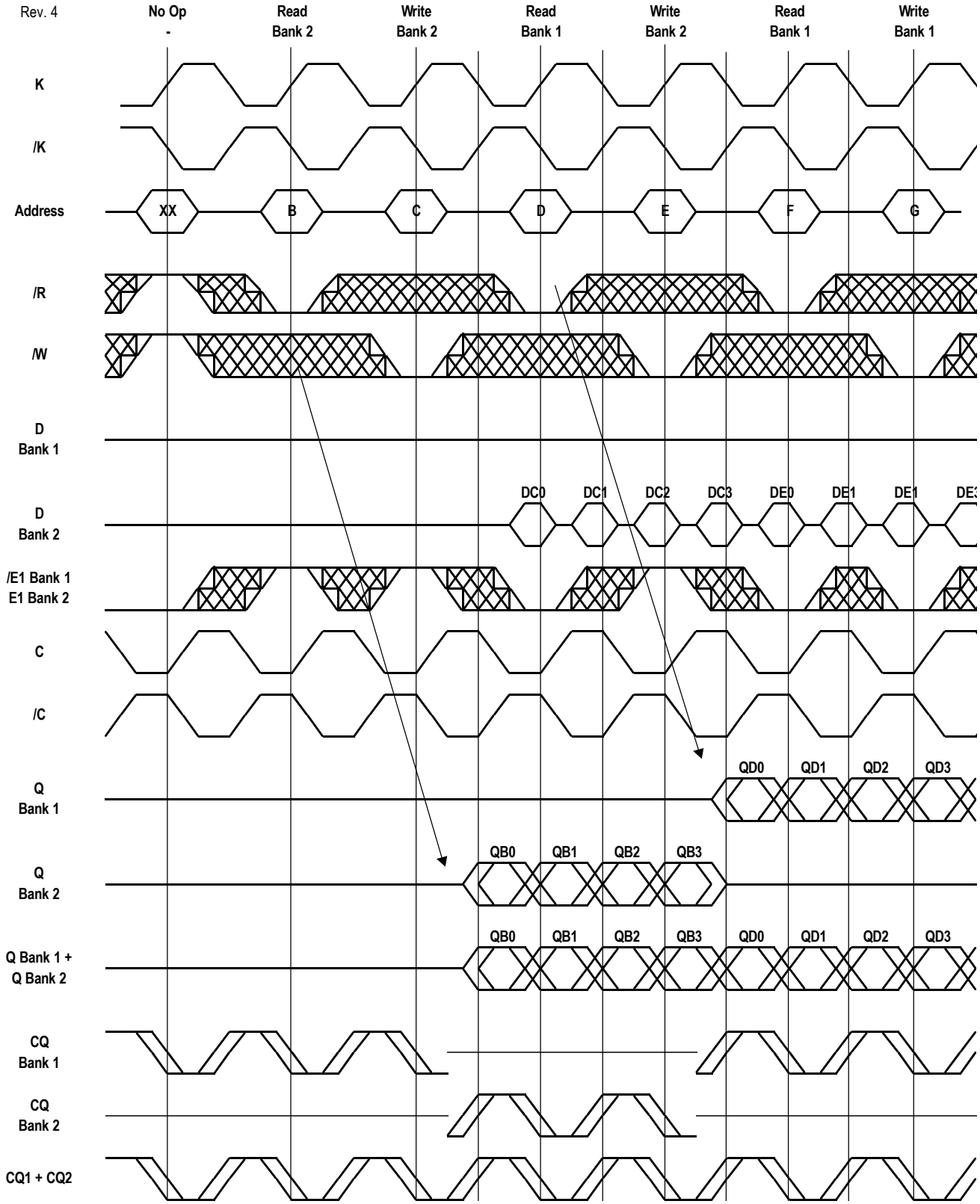


Bank Enable Truth Table

	EP1	EP2	E1	E2
Bank 0	VSS	VSS	Active Low	Active Low
Bank 1	VSS	VDD	Active Low	Active High
Bank 2	VDD	VSS	Active High	Active Low
Bank 3	VDD	VDD	Active High	Active High

Note: For simplicity K, C and CQ are shown single ended and Bx, is not shown.

Σ2x2B4 SigmaRAM Depth Expansion



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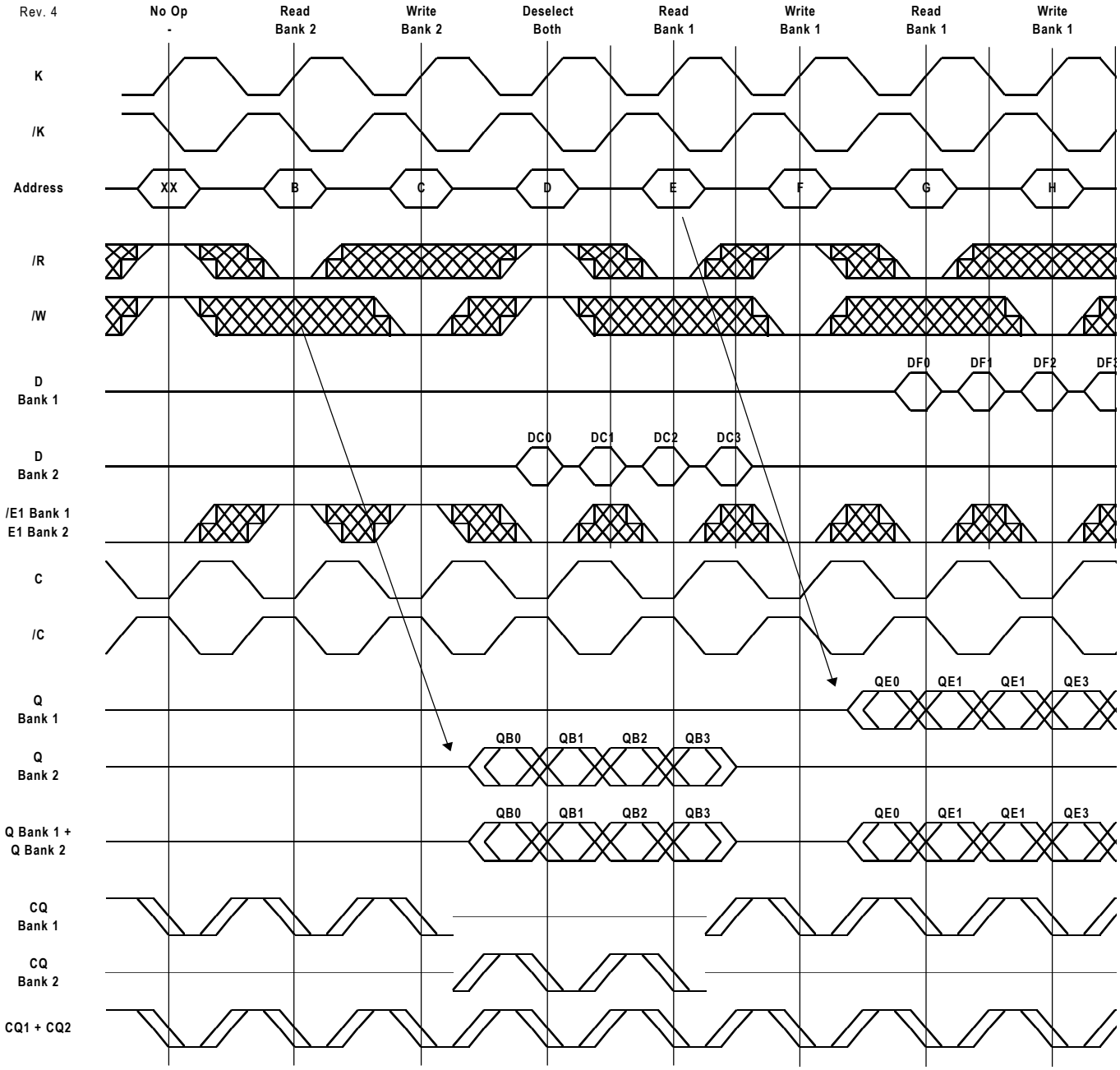
It should be noted that deselection of the RAM via E1 and E2 also deselects the Echo Clock output drivers. The deselection of Echo Clock drivers is always pipelined to the same degree as output data. Deselection of the RAM via $\overline{R}$ does not deactivate the Echo Clocks.

In some applications it may be appropriate to pause between banks—to deselect both RAMs with $\overline{R}$ before resuming read operations. An $\overline{R}$ deselect at a bank switch will allow at least one clock to be issued from the new bank before the first read cycle in the bank. Although the following drawing illustrates a $\overline{R}$ read pause upon switching from Bank 1 to Bank 2, a Write to Bank 2 would have the same effect, causing the RAM in Bank 2 to issue at least one clock before it is needed.

Σ2x2B4 Bank Switch with Deselect



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AutoFLX™ Output Driver Impedance Control

HSTL I/O SigmaRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to V_{SS} via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a vendor specified tolerance is between 150Ω and 300Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps. Impedance updates for "0s" occur whenever the SRAM is driving "1s" for the same DO's (and vice-versa for "1s") or the SRAM is in HI-Z. The SRAM requires 32K start-up cycles, selected or deselected, after V_{DD} reaches its operating range to reach its programmed output driver impedance.

Separate I/O Σ2x2B4 SigmaRAM Truth Table

K	Previous State	Control Inputs			Next State	D (t_n +1)	D (t_n + 1½)	D (t_n + 2)	D (t_n + 2½)	Q CQ (t_n +1)	Q CQ (t_n + 1½)	Q CQ (t_n + 2)	Q CQ (t_n + 2½)
		E	$\overline{R}$	$\overline{W}$									
↑	Deselect, Bank Deselect,	F	1	1	Bank Deselect	X		—		Hi-Z		—	
↑	Deselect Write	F	1	X	Bank Deselect	X		—		Hi-Z		—	
↑	Deselect Read	F	X	1	Bank Deselect	X		—		Hi-Z		—	
↑	Write	F	1	X	Bank Deselect	D2	D3	—		Hi-Z		—	
↑	Read	F	X	1	Bank Deselect	X		—		Q2 CQ2	Q3 CQ3	—	
↑	Deselect, Bank Deselect	F	1	0	Deselect Write	X		X		Hi-Z		—	
↑	Deselect Read	F	X	0	Deselect Write	X		X		Hi-Z		—	
↑	Read	F	X	0	Deselect Write	X		X		Q2 CQ2	Q3 CQ3	—	
↑	Deselect, Bank Deselect, Deselect Write	F	0	X	Deselect Read	X		—		Hi-Z		Hi-Z	
↑	Write	F	0	X	Deselect Read	D2	D3	—		Hi-Z		Hi-Z	
↑	Deselect, Bank Deselect	T	1	1	Deselect	X		—		Hi-Z CQ0	Hi-Z CQ1	—	
↑	Deselect Write	T	1	X	Deselect	X		—		Hi-Z CQ0	Hi-Z CQ1	—	
↑	Deselect Read	T	X	1	Deselect	X		—		Hi-Z		—	
↑	Write	T	1	X	Deselect	D2	D3	—		Hi-Z CQ0	Hi-Z CQ1	—	
↑	Read	T	X	1	Deselect	X		—		Q2 CQ2	Q3 CQ3	—	
↑	Deselect, Bank Deselect	T	1	0	Write	D0	D1	D2	D3	Hi-Z CQ0	Hi-Z CQ1	—	
↑	Deselect Read	T	X	0	Write	D0	D1	D2	D3	Hi-Z		—	
↑	Read	T	X	0	Write	D0	D1	D2	D3	Q2 CQ2	Q3 CQ3	—	
↑	Deselect, Bank Deselect	T	0	X	Read	X		—		Q0 CQ0	Q1 CQ1	Q2 CQ2	Q3 CQ3
↑	Deselect Write	T	0	X	Read	X		—		Q0 CQ0	Q1 CQ1	Q2 CQ2	Q3 CQ3
↑	Write	T	0	X	Read	D2	D3	—		Q0 CQ0	Q1 CQ1	Q2 CQ2	Q3 CQ3

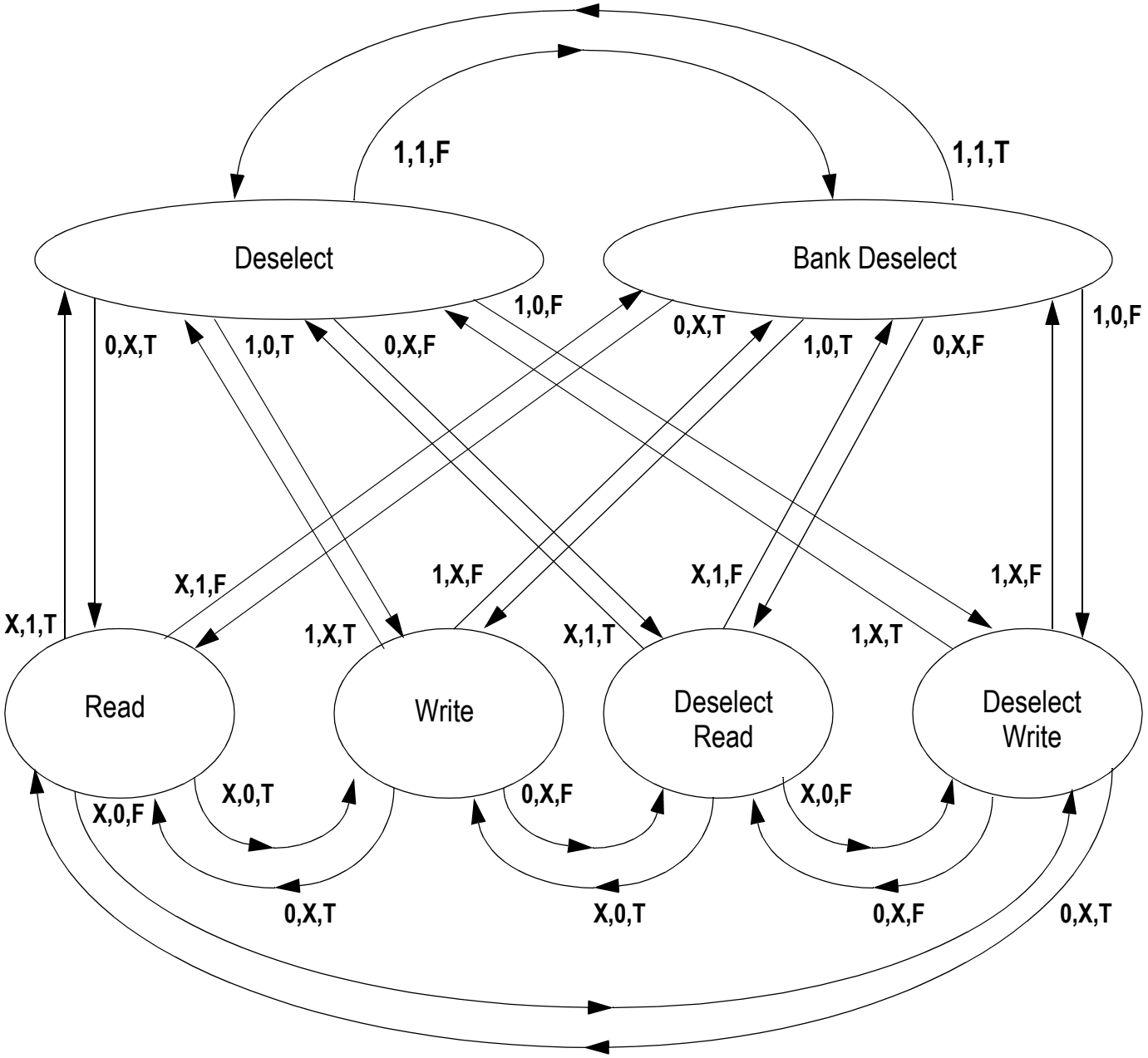
Notes:
1. X = Don't Care, H = High, L = Low. E = T (True) if E1 or E2 are False.
2. D0, D1, D2 and D3 are the first through fourth data input transfers in a write.
3. Q0, Q1, Q2 and Q3 are the first through fourth data output transfers in a read.
4. CQ0, CQ1, CQ2 and CQ3 are the echo clocks associated with the first through fourth data transfers.
5. "—" indicates that the input needed or driver state is determined by a subsequent operation.

  D

x18 Byte Write Enable Truth Table

$\overline{Ba}$	$\overline{Bb}$	Da1 - Da9	Db1 - Db9
0	0	Don't Care	Don't Care
1	0	Data In	Don't Care
0	1	Don't Care	Data In
1	1	Data In	Data In

Σ2x2B4 SigmaRAM Control State Diagram



Key: X,X,X = $\overline{R}$, $\overline{W}$, E where E = T (True) if E1 and E2 are True

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 2.5	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.5 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.5 V max.)	V
I_{IN}	Input Current on Any Pin	+/–100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/–100	mA dc
T_J	Maximum Junction Temperature	125	°C
T_{STG}	Storage Temperature	–55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.95	V	
1.8V I/O Supply Voltage	V_{DDQ}	1.7	1.8	V_{DD}	V	1
1.5V I/O Supply Voltage	V_{DDQ}	1.4	1.5	1.6V	V	1
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	2

Notes:

1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 1.4 V ≤ V_{DDQ} ≤ 1.6 V (i.e., 1.5 V I/O) and 1.7 V ≤ V_{DDQ} ≤ 1.95 V (i.e., 1.8 V I/O) and quoted at whichever condition is worst case.
2. The power supplies need to be powered up in the following sequence: V_{DD}, V_{DDQ}, V_{REF}, followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
DC Input Logic High	V_{IH} (dc)	V_{REF} + 200		mV	
DC Input Logic Low	V_{IL} (dc)		V_{REF} - 200	mV	
DC Clock Input Differential Voltage	V_{DIF} (dc)	400		mV	
V_{REF} DC Voltage	V_{REF} (dc)	V_{DDQ} (min) / 2	V_{DDQ} (max) / 2	V	

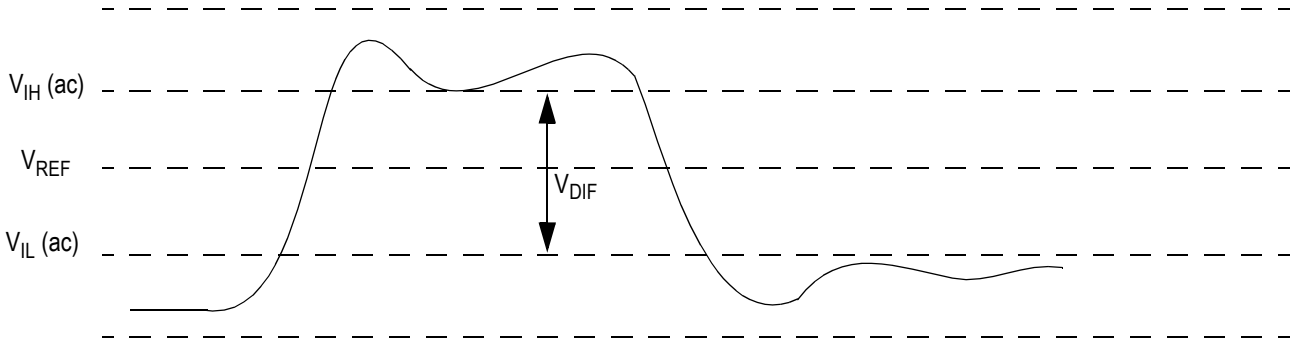
1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. SRAM performance is a function of clock input differential voltage (V_{DIF}).
3. To guarantee AC characteristics, V_{IH},V_{IL},Trise and Tfall of inputs and clocks must be within 10% of each other.
4. For devices supplied with HSTL I/O input buffers.Compatible with both 1.8V and 1.5V I/O drivers.
5. See AC Input Definition drawing below.

HSTL I/O AC Input Characteristics

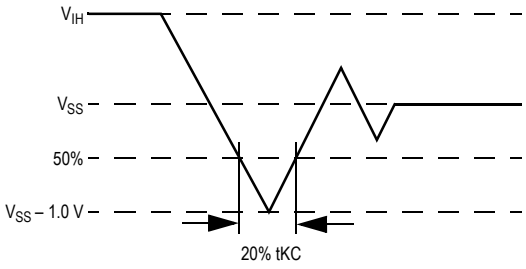
Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	V_{IH} (ac)	V_{REF} + 400		mV	3,4
AC Input Logic Low	V_{IL} (ac)		V_{REF} - 400	mV	3,4
AC Clock Input Differential Voltage	V_{DIF} (ac)	800		mV	2,3
V_{REF} Peak to Peak AC Voltage	V_{REF} (ac)		5% V_{REF} (DC)	mV	1

1. The peak to peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. SRAM performance is a function of clock input differential voltage (V_{REF}). The RAM can be operated with a single ended clocking with either K or $\overline{K}$ tied to V_{REF}.
3. To guarantee AC characteristics, V_{IH},V_{IL},Trise and Tfall of inputs and clocks must be within 10% of each other.
4. For devices supplied with HSTL I/O input buffers.Compatible with both 1.8V and 1.5V I/O drivers.
5. See AC Input Definition drawing below.

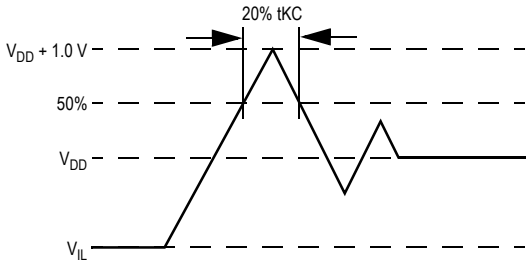
HSTL I/O AC Input Definitions



Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 3.3 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	6	7	pF

Note: This parameter is sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	TBD	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	TBD	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	TBD	°C/W	3

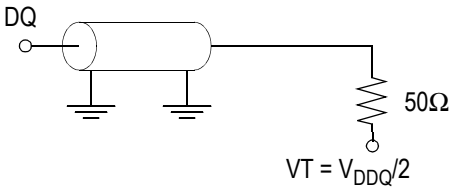
Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87.
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1.

AC Test Conditions

Parameter	Conditions
Input high level	V_{DDQ}
Input low level	0 V
Max. input slew rate	2 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

Notes:
1. Test conditions as specified with output loading as shown unless otherwise noted.

AC Test Load Diagram



RQ = 250 Ω (HSTL I/O)

Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max	Notes
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–2 uA	2 uA	
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ 0 V ≤ $V_{IN} \leq V_{IL}$	–100 uA –2 uA	2 uA 2 uA	
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DDQ}	–2 uA	2 uA	

Programmable Impedance HSTL Output Driver DC Electrical Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	V_{OH}	$V_{DDQ / 2}$	V_{DDQ}	V	1,3
Output Low Voltage	V_{OL}	Vss	$V_{DDQ / 2}$	V	2,3

1. I_{OH} = (V_{DDQ} / 2) / (RQ / 5) +/- 15% @ V_{OH} = V_{DDQ} / 2 (for: 150Ω ≤ RQ ≤ 300Ω).
2. I_{OL} = (V_{DDQ} / 2) / (RQ / 5) +/- 15% @ V_{OL} = V_{DDQ} / 2 (for: 150Ω ≤ RQ ≤ 300Ω).
3. Parameter tested with RQ=250Ω and V_{DDQ} = 1.5 V or 1.8V

Operating Currents

Parameter	Org	Symbol	-333		-300		-250		Test Conditions
			0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	0°C to 70°C	–40°C to +85°C	
Operating Current		IDD	650 mA	TBD mA	600 mA	TBD mA	525 mA	TBD mA	$\overline{E1} \le V_{IL}$ Max. tKHKH ≥ tKHKH Min. All other inputs $V_{IL} \ge V_{IN} \ge V_{IH}$
		IDDQ							
Chip Disable Current		ISB1	250 mA	TBD mA	240 mA	TBD mA	225 mA	TBD mA	$\overline{E1} \ge V_{IH}$ Min. tKHKH ≥ tKHKH Min. All other inputs $V_{IL} \ge V_{IN} \ge V_{IH}$
		ISBQ1							
Bank Deselect Current		ISB2	250 mA	TBD mA	240 mA	TBD mA	225 mA	TBD mA	E2 or E3 False tKHKH ≥ tKHKH Min. All other inputs $V_{IL} \ge V_{IN} \ge V_{IH}$
		ISBQ2							
CMOS Deselect Current		IDD3	150 mA						Device Deselected All inputs V_{SS} + 0.10 V $\ge V_{IN} \ge$ V_{DD} – 0.10 V

Note: Power measured with output pins floating.

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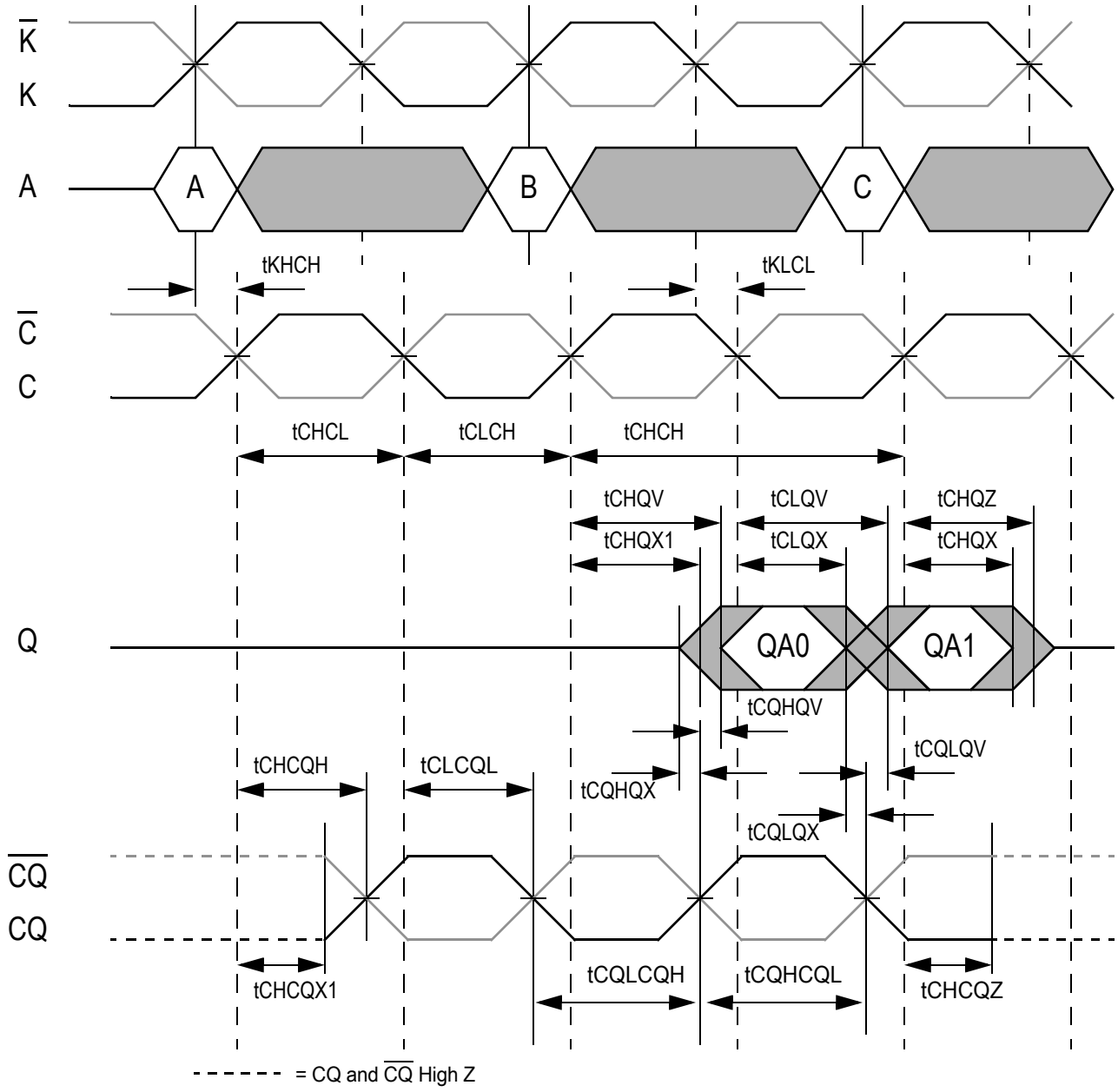
AC Electrical Characteristics

Parameter	Symbol	-333		-300		-250		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Input Clock Cycle Time	tKHKH	3.0	—	3.3	—	4.0	—	ns	—
Output Clock Cycle Time	tCHCH	3.0	—	3.3	—	4.0	—	ns	—
Input Clock HIGH Time	tKHKL	1.2	—	1.3	—	1.6	—	ns	—
Output Clock HIGH Time	tCHCL	1.2	—	1.3	—	1.6	—	ns	—
Input Clock LOW Time	tKLKH	1.2	—	1.3	—	1.6	—	ns	—
Output Clock LOW Time	tCLCH	1.2	—	1.3	—	1.6	—	ns	—
Input Clock High to Output Clock High Time	tKHCH	0	2.0	0	2.2	0	2.6	ns	—
Input Clock Low to Output Clock Low Time	tKLCL	0	2.0	0	2.2	0	2.6	ns	—
Output Clock High to Output Valid	tCHQV	—	1.6	—	1.8	—	2.1	ns	—
Output Clock Low to Output Valid	tCLQV	—	1.6	—	1.8	—	2.1	ns	—
Output Clock High to Output in High-Z	tCHQZ	0.5	1.6	0.5	1.8	0.5	2.1	ns	1
Output Clock Low to Output Invalid	tCLQX	0.5	—	0.5	—	0.5	—	ns	—
Output Clock High to Output Invalid	tCHQX	0.5	—	0.5	—	0.5	—	ns	—
Output Clock High to Output in Low-Z	tCHQX1	0.5	—	0.5	—	0.5	—	ns	1
Output Clock High to Echo Clock Low-Z	tCHCQX1	0.5	—	0.5	—	0.5	—	ns	2, 4
Output Clock High to Echo Clock High	tCHCQH	0.5	1.5	0.5	1.7	0.5	2.0	ns	4
Output Clock Low to Echo Clock Low	tCLCQL	0.5	1.5	0.5	1.7	0.5	2.0	ns	4
Echo Clock High to Output Invalid	tCQHQX	–0.2	—	–0.2	—	–0.25	—	ns	2
Echo Clock Low to Output Invalid	tCQLQX	–0.2	—	–0.2	—	–0.25	—	ns	2
Echo Clock High to Output Valid	tCQHQV	—	0.2	—	0.2	—	0.25	ns	2
Echo Clock Low to Output Invalid	tCQLQX	–0.2	—	–0.2	—	–0.25	—	ns	2
Echo Clock Low to Output Valid	tCQLQV	—	0.2	—	0.2	—	0.25	ns	2
Input Clock High to Echo Clock High-Z	tKHCQZ	0.5	1.5	0.5	1.7	0.5	2.0	ns	1, 2
Output Clock High to Echo Clock High-Z	tCHCQZ	0.5	1.5	0.5	1.7	0.5	2.0	ns	1, 2
Echo Clock High Time	tCQHCQL	tCHCL +/- 100 ps						ns	5
Echo Clock Low Time	tCQLCQH	tCLCH +/- 100 ps						ns	5
Echo Clock High Time	tCQHCQL2	tKHKL +/- 100 ps						ns	5
Echo Clock Low Time	tCQLCQH2	tKLKH +/- 100 ps						ns	5
Input Clock High to Output Valid	tKHQV	—	1.6	—	1.8	—	2.1	ns	—
Input Clock Low to Output Valid	tKLQV	—	1.6	—	1.8	—	2.1	ns	—
Input Clock High to Output in High-Z	tKHQZ	0.5	1.6	0.5	1.8	0.5	2.1	ns	1

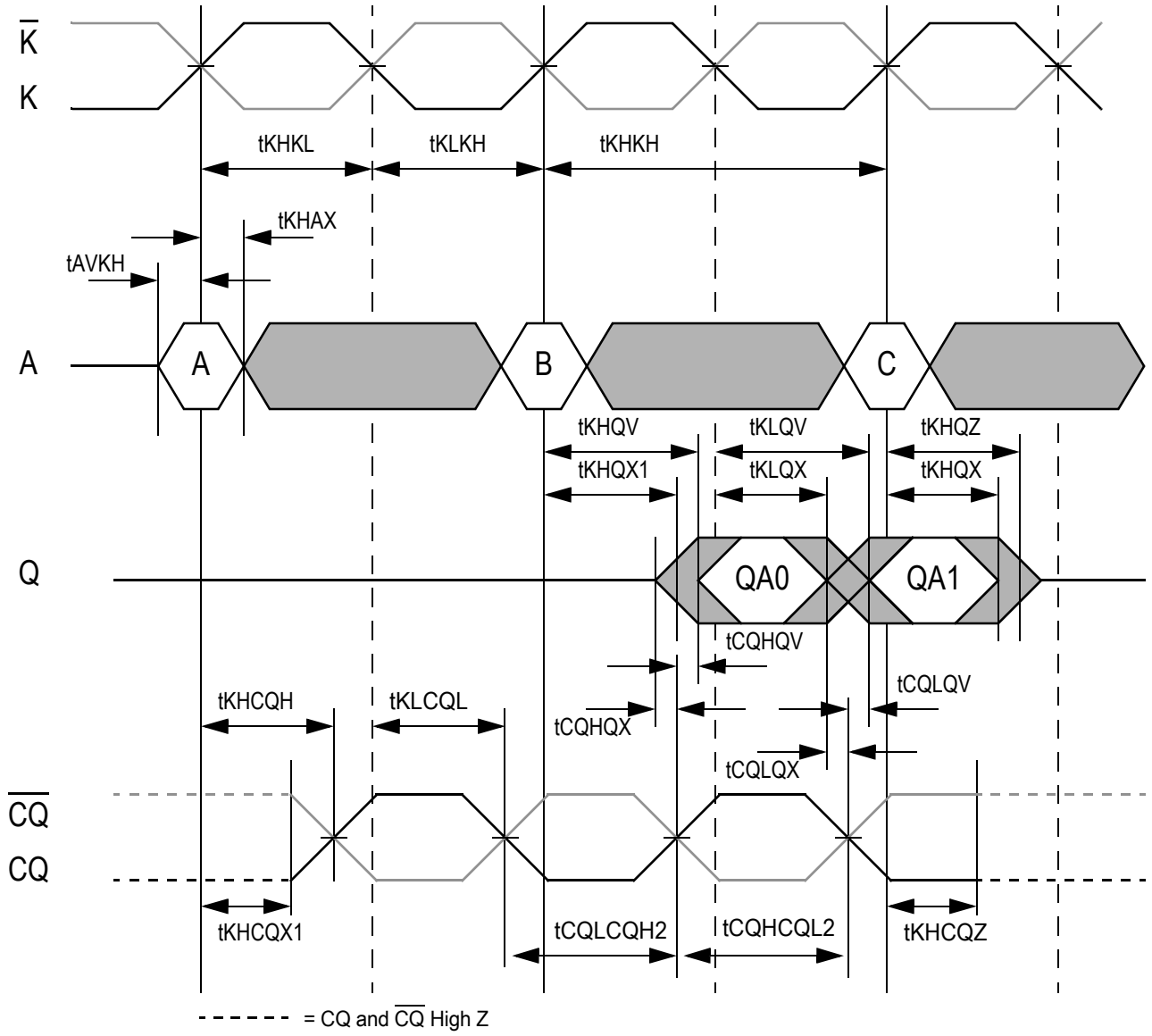
Parameter	Symbol	-333		-300		-250		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Input Clock High to Output Invalid	tKHQX	0.5	—	0.5	—	0.5	—	ns	—
Input Clock Low to Output Invalid	tKLQX	0.5	—	0.5	—	0.5	—	ns	—
Input Clock High to Output in Low-Z	tKHQX1	0.5	—	0.5	—	0.5	—	ns	1
Input Clock High to Echo Clock Low-Z	tKHCQX1	0.5	—	0.5	—	0.5	—	ns	2, 4
Input Clock High to Echo Clock High	tKHCQH	0.5	1.5	0.5	1.7	0.5	2.0	ns	4
Input Clock Low to Echo Clock Low	tKLCQL	0.5	1.5	0.5	1.7	0.5	2.0	ns	4
Address Valid to Input Clock High	tAVKH	0.6	—	0.7	—	0.8	—	ns	—
Input Clock High to Address Don't Care	tKHAX	0.4	—	0.4	—	0.5	—	ns	—
$\overline{R}$, $\overline{W}$ or E Input Valid to Input Clock High	tIVKH	0.6	—	0.7	—	0.8	—	ns	—
Input Clock High to $\overline{R}$, $\overline{W}$ or E Don't Care	tKHIX	0.4	—	0.4	—	0.5	—	ns	—
Data In and $\overline{Bx}$ Valid to Input Clock High	tDVKH	0.32	—	0.35	—	0.40	—	ns	—
Input Clock High to Data In and $\overline{Bx}$ Don't Care	tKHDX	0.27	—	0.30	—	0.35	—	ns	—
Data In and $\overline{Bx}$ Valid to Input Clock Low	tDVKL	0.32	—	0.35	—	0.40	—	ns	
Input Clock Low to Data In and $\overline{Bx}$ Don't Care	tKLDX	0.27	—	0.30	—	0.35	—	ns	

Notes:
1. Measured at 100 mV from steady state. Not 100% tested.
2. Guaranteed by design. Not 100% tested.
3. For any specific temperature and voltage tCHCQZ < tCHCQX1 and tKHCQZ < tKHCQX1.
4. Tested using AC Test Load B

Timing Parameter Key - Read Cycle Timing Using C and $\overline{C}$ to Control Output Data

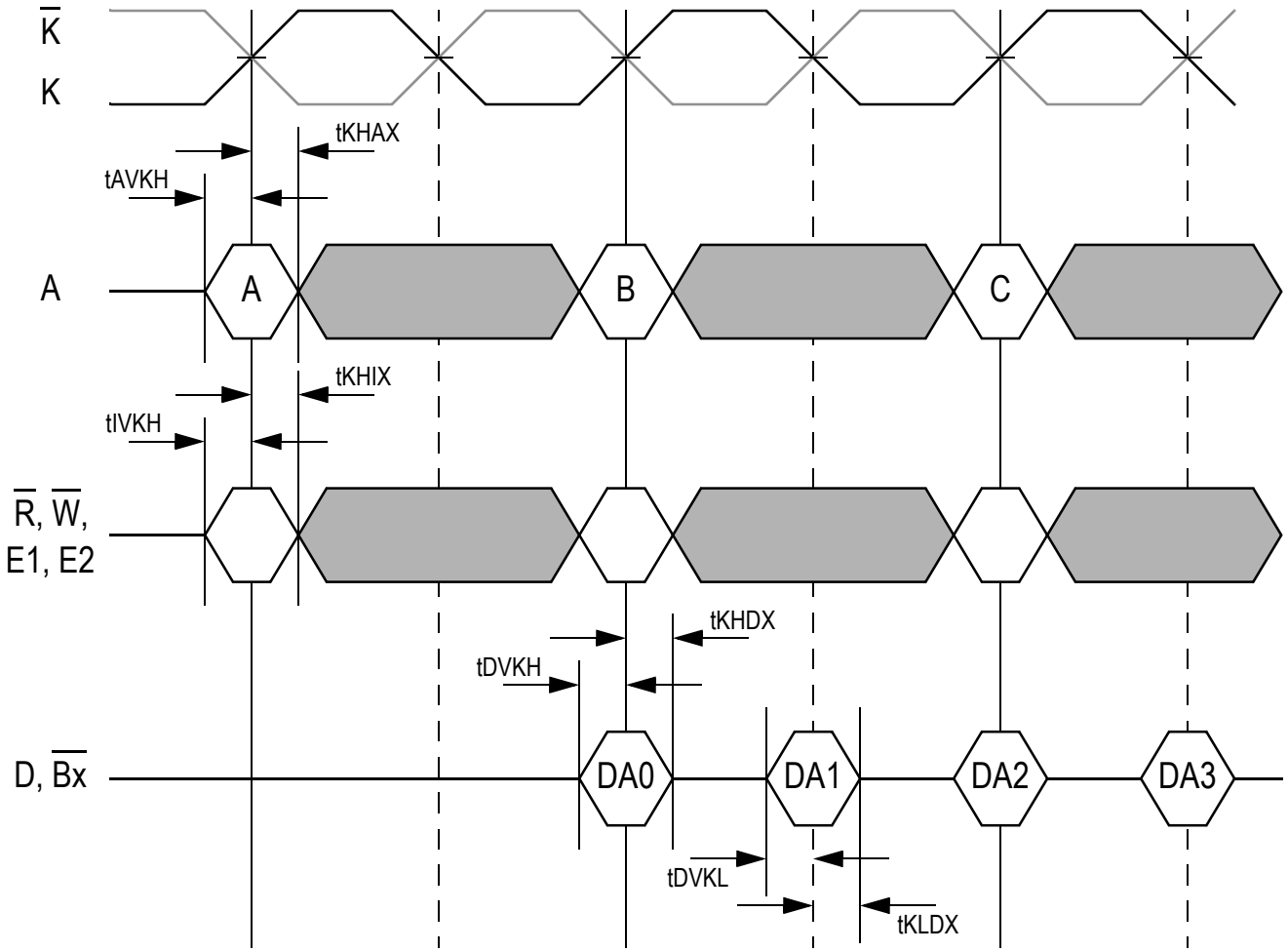


Timing Parameter Key—Read Cycle Timing Using K and $\overline{K}$ to Control Output Data



Note: When K and $\overline{K}$ are used to control output data, C and $\overline{C}$ should be tied "high" (not shown).

Timing Parameter Key—Control and Data In Timing



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JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DDQ}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to V_{DD}. TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

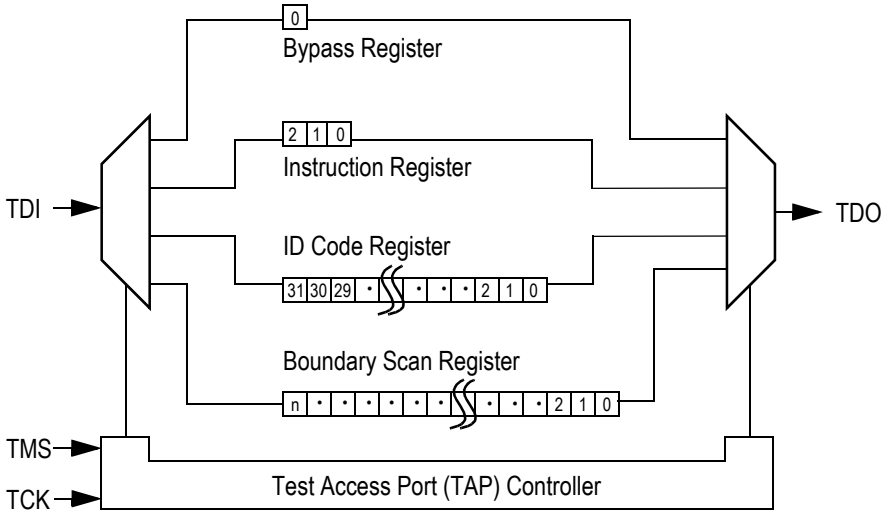
Bypass Register

The Bypass Register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x72																																
x18	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	1

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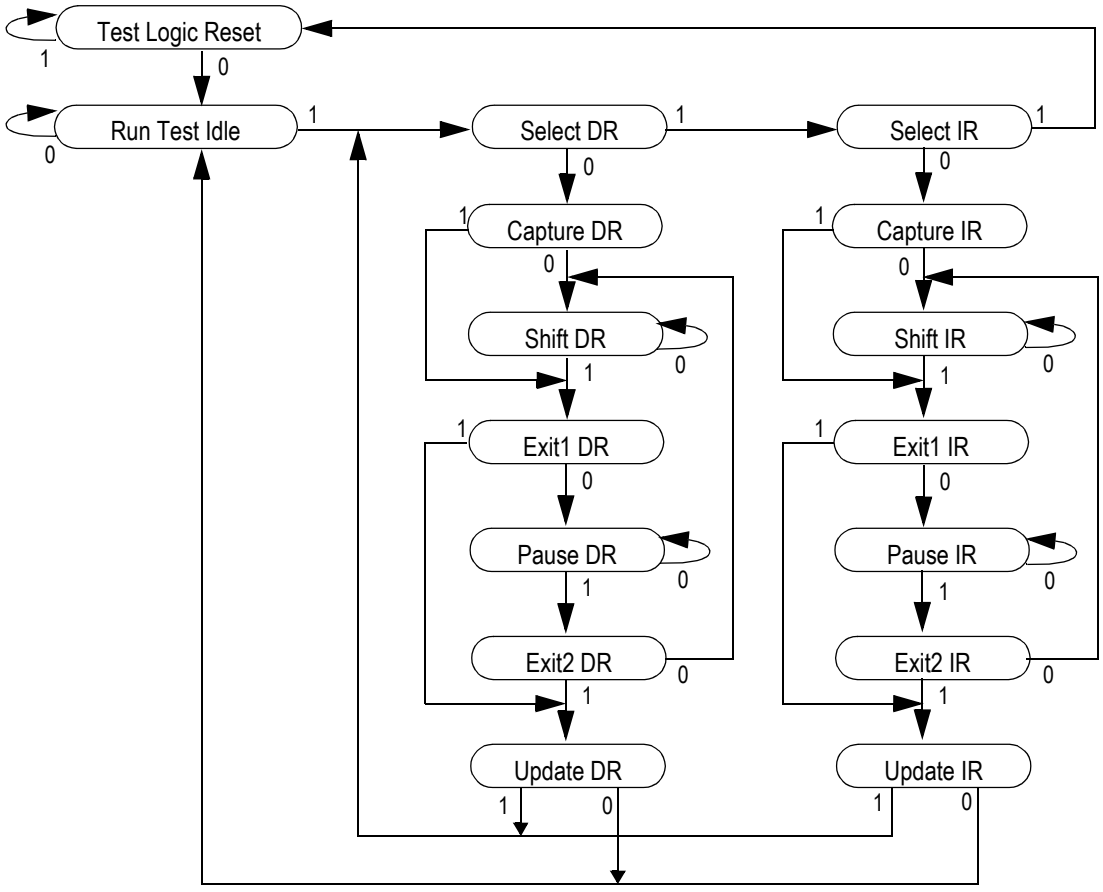
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads. This device will not perform INTEST but can perform the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state, the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register, the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Some Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the BSDL file. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAP's input data capture set-up plus hold time (tTS plus tTH). The RAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the Boundary Scan Register between the TDI and TDO pins. The Update-DR controller state transfers the contents of boundary scan cells into the holding register of each cell associated with an output pin on the RAM.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the state of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are sampled and transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state. Boundary Scan Register contents may then be shifted serially through the register using the Shift-DR command or the controller can be skipped to the Update-DR command. When the controller is placed in the Update-DR state, a RAM that has a fully compliant EXTEST function drives out the value of the Boundary Scan Register location associated with which each output pin.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z/PRELOAD

The SAMPLE-Z instruction operates exactly like SAMPLE/PRELOAD except that loading the SAMPLE-Z instruction forces all the RAM's output drivers, except TDO, to an inactive drive state (high-Z).

RFU

These instructions are reserved for future use. In this device they replicate the BYPASS instruction.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z/ PRELOAD	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all Data and Clock output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1

  D

JTAG TAP Instruction Set Summary

SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI Private	101	GSI Private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in Test-Logic-Reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

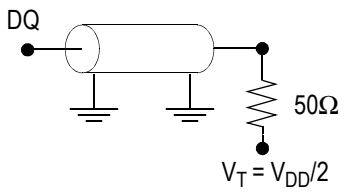
Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input High Voltage	V_{IHT}	0.65 * V_{DD}	V_{DD}+0.3	V	1
Test Port Input Low Voltage	V_{ILT}	–0.3	0.35 * V_{DD}	V	1
TMS, TCK and TDI Input Leakage Current	I_{INTH}	–100	2	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INTL}	–2	2	uA	3
TDO Output Leakage Current	I_{OLT}	–2	2	uA	4
Test Port Output High Voltage	V_{OHT}	V_{DDQ} – 100 mV	—	V	5, 6
Test Port Output Low Voltage	V_{OLT}	—	100 mV	V	7

Notes:
1. Input Under/overshoot voltage must be –1 V < Vi < V_{DD} + 1 V with a pulse width not to exceed 20% tTKC.
2. $V_{DD} \geq V_{IN} \geq V_{IL}$
3. $0 V \leq V_{IN} \leq V_{IL}$
4. Output Disable, V_{OUT} = 0 to V_{DD}
5. The TDO output driver is served by the V_{DD} supply.
6. I_{OH} = –100 uA
7. I_{OL} = +100 uA

JTAG Port AC Test Conditions

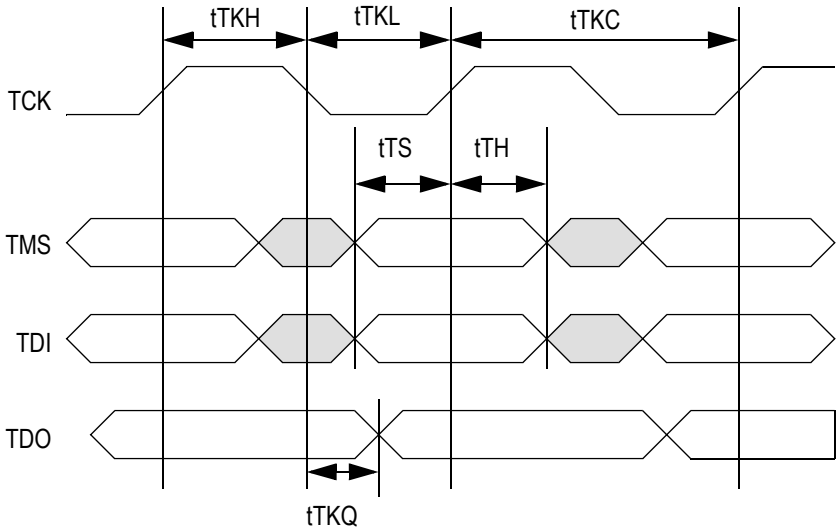
Parameter	Conditions
Input high level	V_{DD} – 200 mV
Input low level	200 mV
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DD}/2$

JTAG Port AC Test Load



Notes:
1. Include scope and jig capacitance.
2. Test conditions as as shown unless otherwise noted.

JTAG Port Timing Diagram



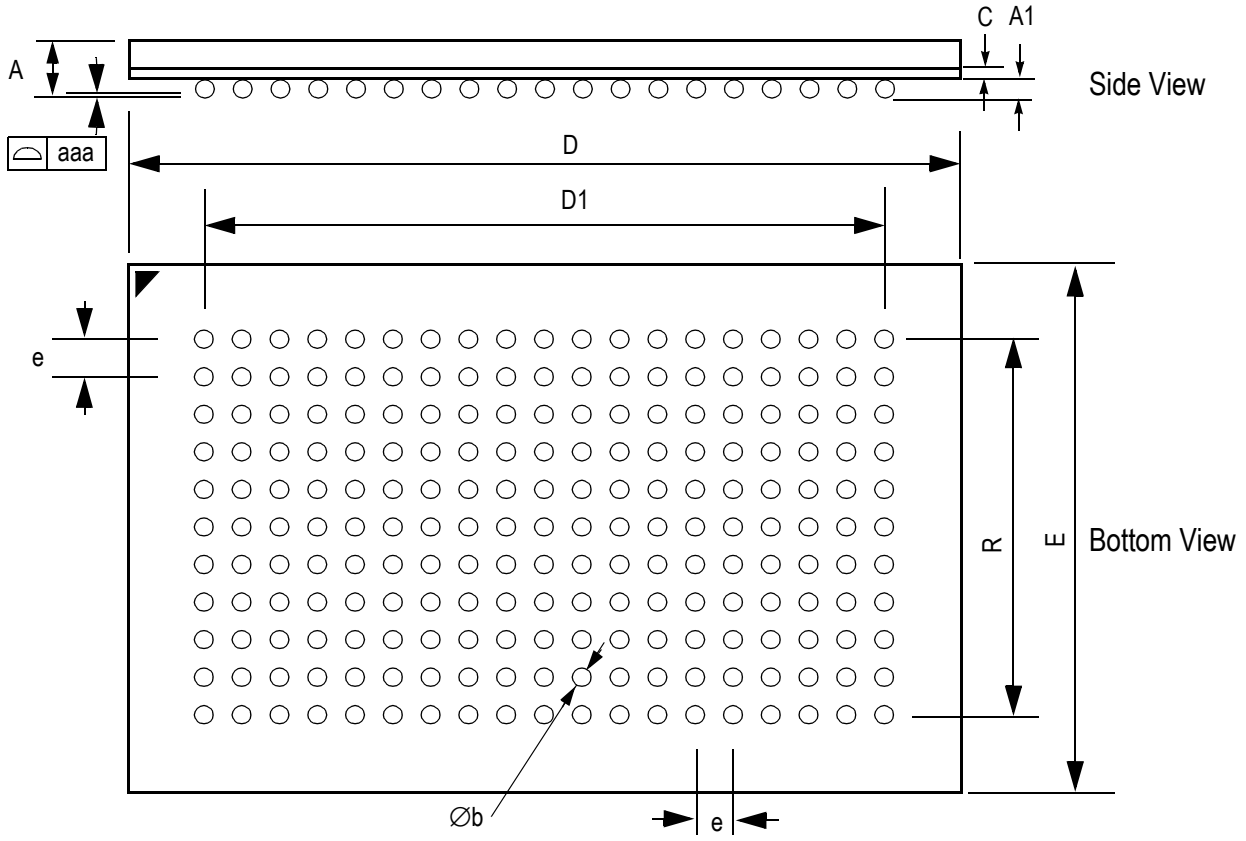
JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

  D

209 BGA Package Drawing

14 mm x 22 mm Body, 1.0 mm Bump Pitch, 11 x 19 Bump Array



Symbol	Min	Typ	Max	Units
A			1.70	mm
A1	0.40	0.50	0.60	mm
Øb	0.50	0.60	0.70	mm
c	0.31	0.36	0.38	mm
D	21.9	22.0	22.1	mm
D1		18.0 (BSC)		mm
E	13.9	14.0	14.1	mm
E1		10.0 (BSC)		mm
e		1.00 (BSC)		mm
aaa		0.15		mm
Rev 1.0				

Ordering Information—GSI SigmaRAM

Org	Part Number[1]	Type	Package	Speed (MHz)	T_A[3]
1M x 18	GS8180D18B-333	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	333	C
1M x 18	GS8180D18B-300	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	300	C
1M x 18	GS8180D18B-250	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	250	C
1M x 18	GS8180D18B-333I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	333	I
1M x 18	GS8180D18B-300I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	300	I
1M x 18	GS8180D18B-250I	Separate I/O ΣRAM	1 mm Pitch, 209-Pin BGA	250	I

Notes:
1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS818x36B-300T.
2. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.

