HDTV
Cable Equaliser
GD14510
Advance Information

General Description

The GD14510 High Definition TV Equaliser is designed for point-to-point cable transmission systems for HDTV signals according to SMPTE292.

The device provides a fully integrated solution for a 1485 Mbit/s adaptive cable equaliser for up to typically 100 metres of Belden 8281 or equivalent cable. The adaptive curve follows the classic √f cable loss characteristic and compensates for more than 20 dB loss at 750 MHz, keeping jitter less than typ. 100 ps_{P-P} after 100 metres of Belden 8281.

Baseline wander caused by pathological signals is minimised with a low cut-off frequency, AC-coupled input buffer. Worst case signals repeated continuously over a TV-line do not introduce any errors for cable lengths less than 100 metres.

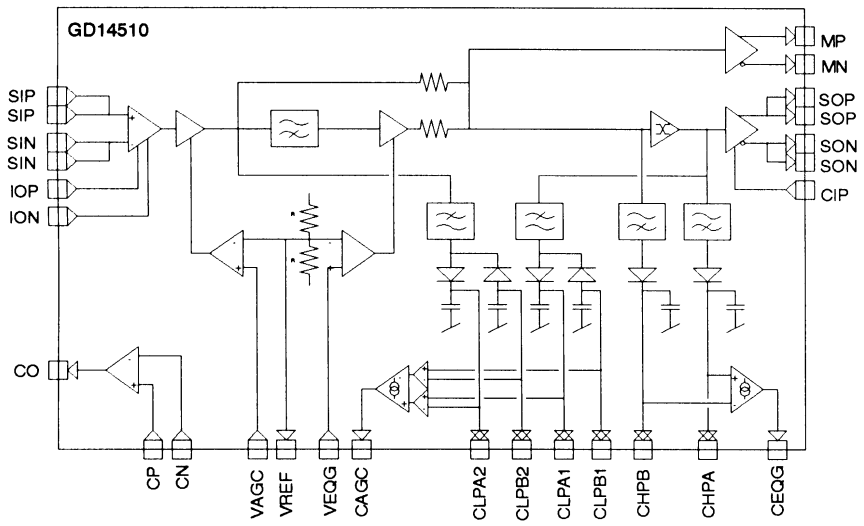
The high-speed data input is differential and compatible with PECL levels.

The output is a differential Open Collector 75 Ω cable driver with a sink capability of 30 mA. The drive current may be adjusted in the range 20 mA - 30 mA by the current control pin CIP, which also can be used to shut down the output. The output can be configured as a 50 Ω differential PECL output to drive an optical transmitter module.

Data input and output are connected via loop-through transmission lines to minimise stub related reflections with better than 15dB return loss @1485 MHz.

An uncommitted Comparator is available for use in signal strength detection.

The GD14510 is fabricated in Siemens' B6HF Technology and is packaged in a 40 pin Leaded Multilayer Ceramic package (MLC) with cavity down.



Features

- Nominal data-rate 1485 Mbit/s NRZI.
- Differential Data input and output with Loop-Through connection for better than 15dB return loss @1485MHz.
- Residual Jitter in accordance with SMPTE292.
- Open Collector 75 Ω cable driver output with external termination resistors.
- Mute capability in output buffer.
- External capacitors for adjustment of time constants
- 5 V supply operation. Power dissipation 500 mW typ.
- 40 Pin Multilayer Ceramic Leaded - package with transmission lines.

Applications

- HDTV Studio equipment.

Reference Standards

- SMPTE 292M (May 7, 1995): Bit-Serial Digital Interface for HDTV
- SMPTE RP184 (April 1, 1995): Measurement of Jitter...

Function detail

The GD14510 adaptive cable equaliser has several functional blocks allowing a number of modes of operation.

IO's

The differential input buffer of the GD14510 is externally AC-coupled and connected as a high-pass single-ended to differential converter with cut-off frequency around 500Hz. The low cut-off frequency eliminates the problems of baseline wander caused by pathological signals, since these are DC balanced over a time span of roughly 100 µs. Any DC offset due to process variations can be compensated at the IOP and ION pins. The input can also be used as a PECL compatible differential input. Refer to Figure "External Circuits" for details regarding external circuitry.

The cable driver is a differential open collector output. The sink current is set at the CIP pin. I_{CIP}=-1.2mA corresponds to $I_{SOP/SON,LOW}$=-30mA. The CIP input equivalent circuit is shown in Figure "External Circuits". Pulling CIP to VEE will mute the cable driver.

The waveform monitor outputs (pins MP and MN) are internally terminated (75Ω) CML outputs intended for AC-coupling to an oscilloscope. This allows monitoring of the equalised signal waveform prior to the limiting amplifier. A large (>10µF) coupling capacitor should be used if baseline wander is to be avoided.

Data path

The data path consists of the input buffer, a broadband amplifier, an equalising filter, a limiting amplifier and the cable driver.

The broadband gain is adjustable in the range –6dB to +3.5dB. The gain increases from .5 to 1.5 linearly when the voltage at pin VAGC increases from 2V to 3V.

The voltage at pin VEQG (to be tuned in the range 2V to 3V) controls the equalising filter.

Control system

Obviously, the device can be manually controlled by driving the voltages VAGC and VEQG. For adaptive operation, two detector systems are included: a low-pass filtered peak-peak detector part for amplitude control and a high-pass filtered rectified peak detector part for cable attenuation compensation. The low-pass control loop is intended for compensation of variations in transmitted amplitude or of variations due to broadband attenuation.

A low-pass filter followed by a peak-peak detector detects the low-frequency (<100 MHz) amplitude of the received signal. A similar system detects the amplitude of the output of the limiting amplifier thereby eliminating the data dependency of the low-pass filtered signal. Both negative and positive peaks are detected to make the scheme insensitive to any baseline wander. Thus four peaks are detected and compared as shown in Figure "Schematic". The comparator drives the control output CAGC intended for driving the control input VAGC as shown in Figure "External Circuits". The charging and storage time of the peak detectors can be adjusted by adjusting the size of the capacitors at pins CLPA1, CLPA2, CLPB1 and CLPB2 (a 20pF capacitor is included on chip for each pin). Please note that the capacitors at pins CLPA1 and CLPA2 (CLPB1 and CLPB2) must be identical (nominal value: 1nF).

Offsets in these detectors will cause the control loop to settle away from the optimum output signal waveform. Offset can be compensated by changing the pull-down resistance at pins CLPA1 and CLPA2 as shown in Figure "External Circuits" (see below).

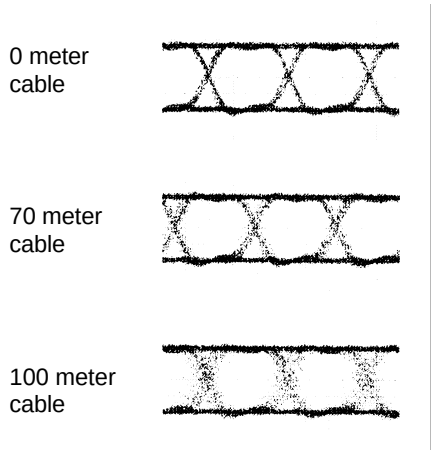
The equalising filter is controlled in a similar fashion only for this purpose the rectified high frequency (> 100MHz) content of the equalised signal is detected. This is compared to the rectified high frequency content for the output of the limiting amplifier. Using a signal of known shape and amplitude rather than a constant for reference will eliminate pattern dependency. The comparator drives the control output CEQG intended for driving the control input VEQC as shown in Figure "External Circuits". The charging and storage time of the peak detectors can be adjusted by adjusting the size of the capacitors at pins CHPA and CHPB (a 20pF capacitor is included on chip for each pin). Please note that these capacitors must be identical (nominal value: 1nF).

Offsets can be compensated by changing the pull-down resistance at pins CHPA and CHPB as shown in Figure "External Circuits". The control system will set the control voltage VEQG to make the voltage at CHPA and CHPB equal. Thus, the offset should be adjusted to make this yield a satisfactory output eye pattern at all relevant input cable lengths, while keeping VEQG within its normal operating range (see below).

The normal operating range of the control voltage pins (VAGC and VEQG) is 2V to 3V. If a satisfactory output eye-pattern with nominal amplitude cannot be established within this range, the adaptive loops will continuously drive the control voltages in the desired direction. I.e. an input voltage swing below (above) approx. 600mV_{pp} (1600mV_{pp}) will cause CAGC to be driven to VCC (VEE) leaving VAGC at approx. 4V (1V). Similarly, VEQG and CEQG is decreased if the equalised signal exhibits overshoot. Thus, if at the low gain setting (VEQG = 2V) the equalised signal still exhibits overshoot, VEQG will be driven low as CEQG is pulled to VEE.

Offset adjustment

The peak detector offsets have to be adjusted by the following procedure: apply a nominal signal (800mV_{pp}) through 0-1m cable, tune the potentiometer PL (see Figure "External Circuits") to make VAGC = 2.3V, then tune PH to make VEQG = 2.3V. Finally verify that VAGC = 2.3V and VEQG = 2.3V simultaneously. Typical cable driver outputs are shown below:



Uncommitted comparator

An uncommitted comparator is included. This can be used to mute the cable driver by driving CIP low through a series resistor. It is recommended that loss of signal (or cable too long) be detected at the CEQG control output. I.e. mute the cable driver if CEQG > 4.5V

Pin List

Mnemonic	Pin No.	Pin Type	Description (see also "Functional Details" and "Ext. circuits")
SOP SON	67910	Anl. OUT	Differential serial data output. High speed Open Collector outputs to be used with 75 Ω cable or 50 Ω termination for optical transmitter.
CIP	11	Anl. IN	DC-Current control input for SOP,SON: 1mA current into CIP generates 25 mA bias for the differential output stage. Max. setting is 1.2 mA => 30 mA output stage bias. If CIP is pulled low, the output stage will turn off.
SIP SIN	33,34 31,32	Anl. IN	Serial data input (differential). Compatible with PECL levels. Loop-Through termination: Each input is connected to two pins, one for input and the other for the termination resistor.
IOP ION	36 37	Anl. IN	Offset adjust for input stage. Connect to 10 kΩ potentiometer with wiper to VEE.
MP MN	3 4	Anl. OUT	Differential monitor output with 75 Ω internal termination to V_{CC}. Typical 100 mV_{PP} output into 75 Ω.
VREF	23	Anl. OUT	Gain adjust reference voltage for sense and decoupling only.
VEQG CEQG	24 25	Anl. IN Anl. OUT	Gain adjust input for equalising filter buffer. Control output for equaliser loop. Charge Pump buffer provides sink or source current for the integrating capacitor in the external equaliser loop filter.
CHPB CHPA	28 29	Anl. OUT Anl. OUT	Signal & Reference high-pass peak detectors for equaliser loop.
VAGC CAGC	22 21	Anl. IN Anl. OUT	Gain adjust for input buffer. Control output for AGC loop. Charge Pump buffer provides sink or source current for the integrating capacitor in the external AGC loop filter.
CLPB2 CLPB1 CLPA2 CLPA1	13 14 15 16	Anl. OUT Anl. OUT Anl. OUT Anl. OUT	Signal & Reference low-pass negative peak detectors for AGC loop. Signal & Reference low-pass positive peak detectors for AGC loop.
CP CN	39 40	Anl. IN	Comparator positive & Negative input.
CO	1	TTL OUT	Comparator output.
V_{CC}	8,18,20,27,35	PWR	+5 V Power.
V_{CCC}	38	PWR	+5 V Power for comparator
V_{EE}	5,12,17, 19,26,30	PWR	0 V Power.
V_{EEC}	2	PWR	0 V Power for comparator.

Maximum ratings

These are the limits beyond which the component may be damaged.

Symbol	Characteristic	Conditions	MIN	TYP	MAX	UNIT
V_{CC}	Positiv Supply		V_{EE} -0.5		7	V
$V_{I\ max,CIP}$	Input Voltage f. CIP		V_{EE} -0.5		V_{CC} +0.5	V
$I_{I\ max,CIP}$	Input Current f. CIP		-1.0		3.0	mA
$V_{O\ max}$	Output Voltage		V_{EE} -0.5		V_{CC} +0.5	V
$I_{O\ max}$	Output Current				40	mA
$V_{I\ max}$	Input Voltage		V_{EE} -0.5		V_{CC} +0.5	V
$I_{I\ max}$	Input Current		-1.0		1.0	mA
T_O	Operating Temp.	Junction	-55		+150	^oC
T_S	Storage Temp.		-65		+175	^oC

DC characteristics

T_{CASE} = 0^{o}C to 70^{o}C, appropriate heatsinking is required. θ_{J-C} = 9°C/W.
All voltages in the table are referred to V_{EE}

Symbol	Characteristic	Conditions	MIN	TYP	MAX	UNIT
V_{CC}	5 V Supply Voltage		4.75	5.00	5.25	V
I_{CC}	Total current from V_{CC}			100		mA
PD	Power dissipation			500		mW
$V_{C\ SIP/SIN}$	SIP/SIN Common Mode Voltage		V_{CC}-2.0		V_{CC}-0.5	V
$V_{I\ SIP/SIN}$	SIP/SIN Differential input Voltage		Note 2		1000	mV_{P-P}
$I_{OH\ SOP/SON}$	Open Collector Output HI Sink Current	Note 3	-20	-25	-30	mA
$I_{OL\ SOP/SON}$	Open Collector Output LO Sink Current	Note 3			-0.5	mA
V_{VREF}	VREF voltage	Note 1		2.5		V
$I_{OH\ CEQG/CAGC}$	Charge Pump source current	Note 4	500	1000		µA
$I_{OL\ CEQG/CAGC}$	Charge Pump sink current	Note 4	-500	-1000		µA

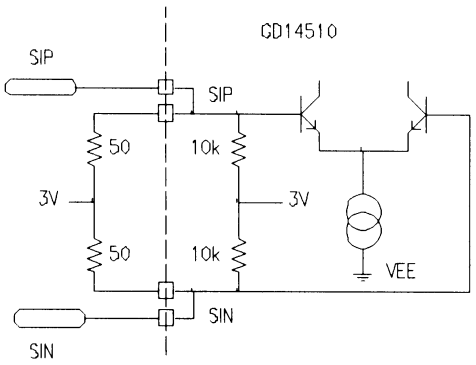
Note 1: For sense and external decoupling only. VREF is the midpoint of two 10 kΩ resistors to V_{CC} and V_{EE}
Note 2: The output voltage from 100m coax cable (Belden 8281) driven with 800 mV_{P-P}
Note 3: R_{load} = 50 Ω to V_{CC}. Current into CIP= 1 mA. Logic level "1" corresponds to no current in in the open collector output.
Note 4: Output terminated to 2.5 V during test.

AC characteristics

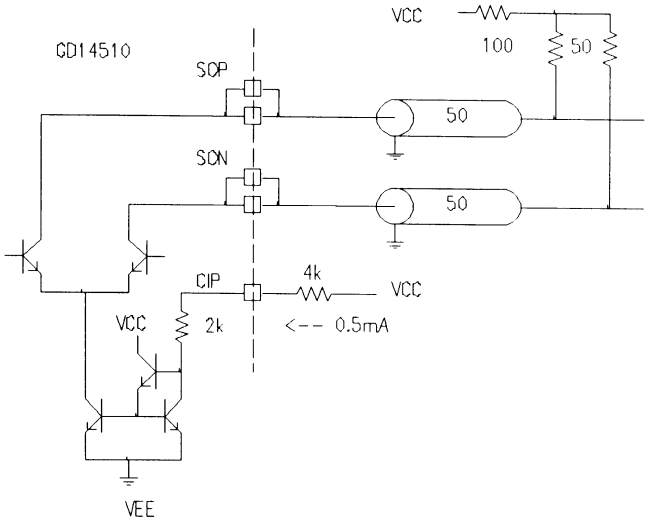
T_{CASE} = 0°C to 70°C, V_{CC} =5.0V

Symbol	Characteristic	Conditions	MIN	TYP	MAX	UNIT
f_{IN}	Input Data Rate				1500	Mb/s
G_{EQ}	Equaliser compensation	F_{IN} = 750 MHz	20			dB
J_{Tim}	Residual Timing Jitter	10 Hz< F <150 MHz (Note1)			1	UI_{p-p}
J_{Alg}	Residual Alignment Jitter	100 kHz<F<150 MHz (Note1)			0.2	UI_{p-p}
V_{IN}	SIN input voltage level	Single ended, 1 m cable	720	800	1000	mV_{p-p}
$T_{TLH\ SOP/SON}$	SOP/SON 20/80% rise time	1 m cable, 75 Ω load			270	ps
$T_{THL\ SOP/SON}$	SOP/SON 80/20% fall time	1 m cable, 75 Ω load			270	ps
$T_{THL\ MP/MN}$	MP/MN 20/80% rise time	1 m cable, 75 Ω load			270	ps
$T_{THL\ MP/MN}$	MP/MN 80/20% rise time	1 m cable, 75 Ω load			270	ps
$V_{o\ MP/MN}$	MP/MN output voltage	1 m cable, 75 Ω load		100		mV_{p-p}

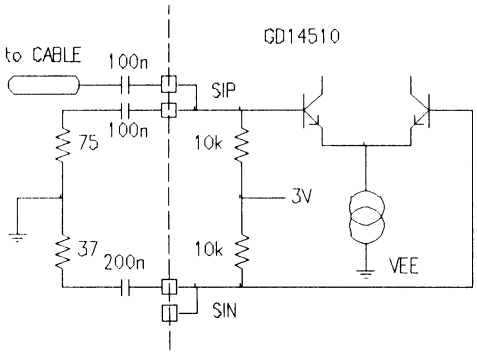
Note 1: 1 UI (serial) = 673 psec, Data Pattern 2^{23}-1 PRBS. 100 metres Belden 8281. Measured as per SMPTE RP184.



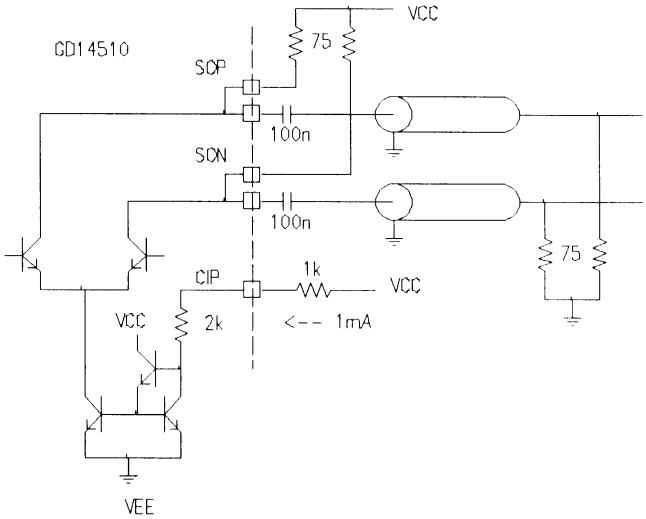
PECL Input configuration



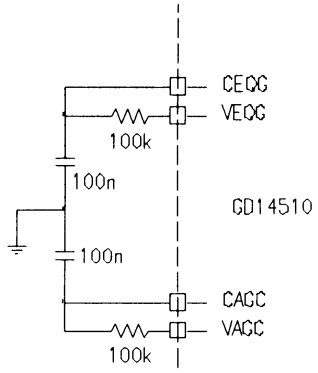
Differential PECL driver



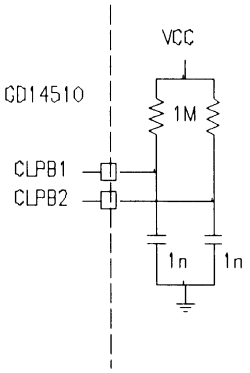
Standard Input configuration

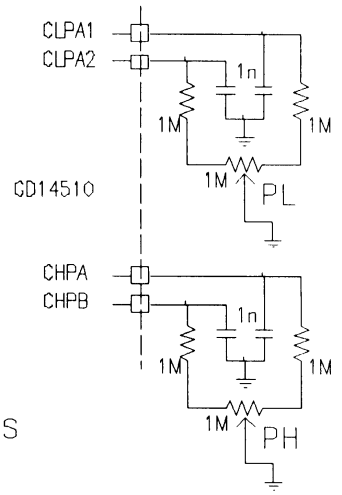


Dual 75R Cable driver



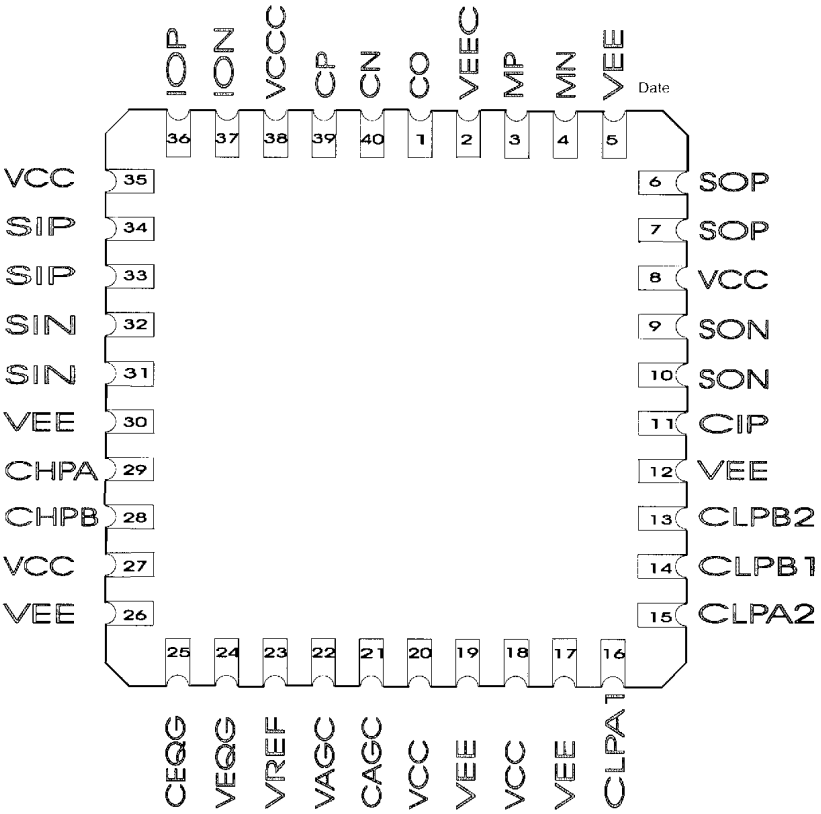
Loop filters





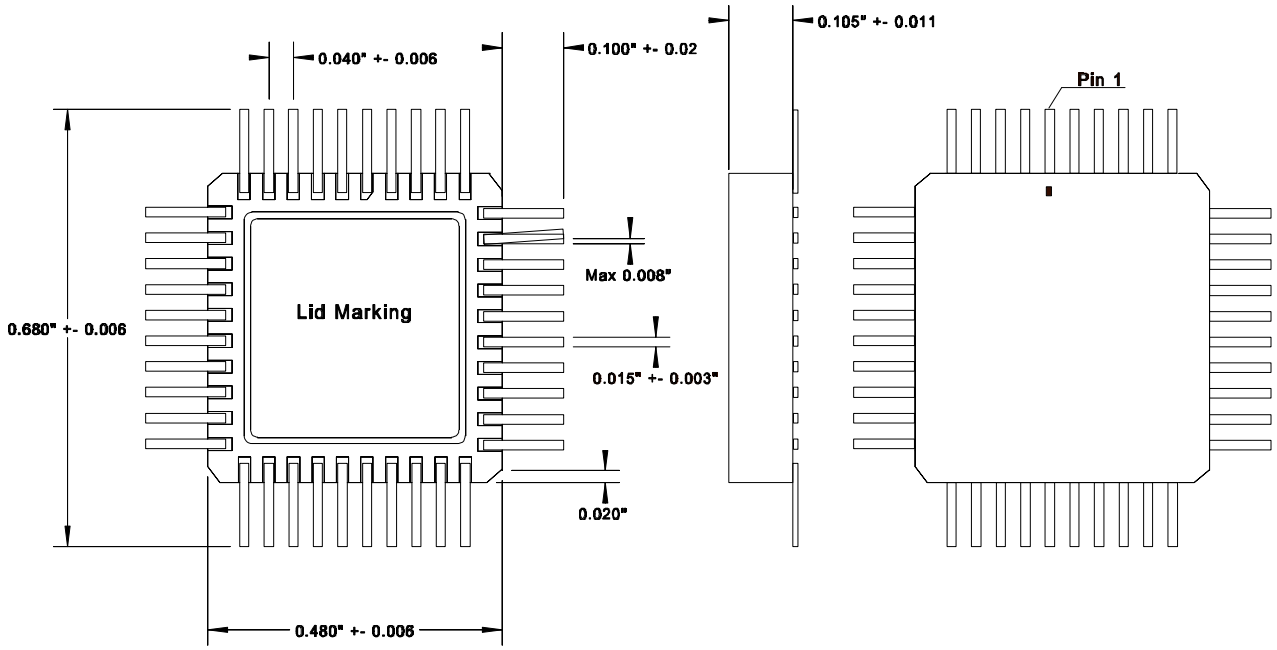
Peak detectors

Package Pinout



Pinout of GD14510, Bottom View

Package Outline



Note 1: Leads are hot dip soldered before cutting.
Note 2: Coplanarity of leads > 0.008”

Ordering Information

To order, please specify as shown below:

Package type	Temperature range	Speed Option	Product name
40 pin Ceramic (MLC)	0..70^{o}C		GD14510-40AB

Mileparken 22, DK-2740 Skovlunde
Denmark
Telephone +45 44 92 61 00
Telefax +45 44 92 59 00
E-mail: Sales@giga.dk

Document ID: GD14510.06
Version: 06
Date: 1998.06.26

Distributor: