10 Gbit/s Receiver, CDR and DeMUX GD16584/GD16588 (FEC)

Preliminary

General Description

GD16584 and GD16588 are Receiver chips for use in STM-64/192 and Optical Transport Networking (OTN) systems.

The component is available in two versions:

- GD16584 for 9.5328 Gbit/s.
- GD16588 for 10.66 Gbit/s for OTN or Forward Error Correction (FEC).

Except the different operating bit rates the two versions are functional identical.

The receiver is a Clock and Data Recovery IC with:

- a low noise VCO
- a Bang-Bang Phase Detector
- a 1:16 De-multiplexer
- a Lock Detect
- a Phase and Frequency Detector.

Clock and data are regenerated by using a *Phase Locked Loop* (PLL) with an external passive loop filter.

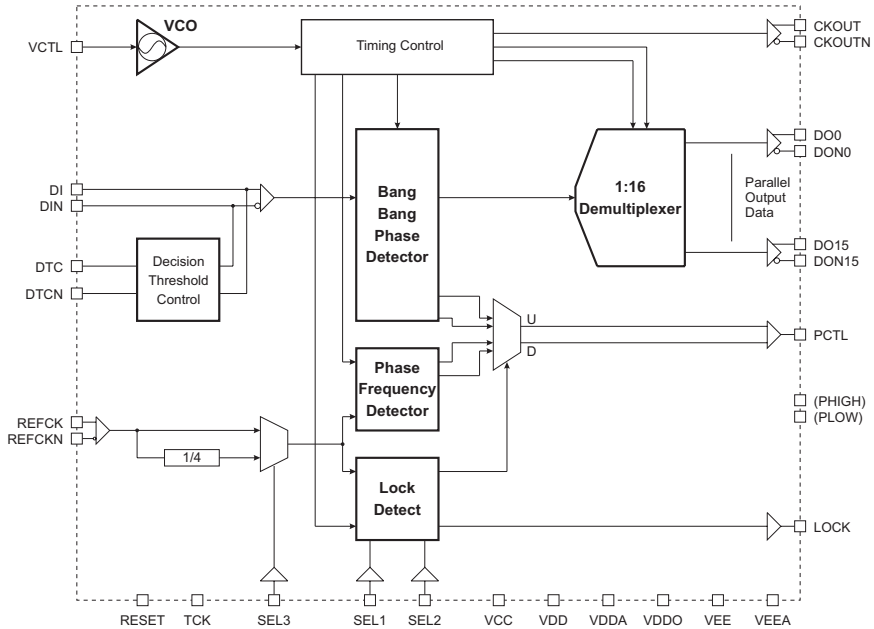
The VCO frequency is controlled by one of the two Phase Detectors in order to ensure capture and lock to the line data rate. The Lock Detector circuit monitors the VCO frequency and determines when the VCO is within the lock range. When the frequency deviates more than 500 ppm from the reference clock, it automatically switches the phase and frequency detector into the PLL loop. In the auto lock mode the locking range is selectable between 500 or 2000 ppm.

When the VCO frequency is within the lock range, the Bang-Bang Phase Detector takes over. It controls the phase of the VCO until the sampling point of data is in the middle of the bit period, where the eye opening is largest. A ±40 mV *Decision Threshold Control* (DTC) is provided at the 10 Gbit/s input.

The 10 Gbit/s input data is sampled and de-multiplexed by the 1:16 DeMUX. The parallel output interface is synchronised with the 622 MHz output clock. The clock and data outputs are LVDS compatible.

The device operates from a dual -5.2 V and +3.3 V power supply. The power dissipation is 3.3 W, typical.

The device is manufactured in a Silicon Bipolar process and packaged in an 132 balls 13 × 13 mm Ceramic Ball Grid Array (CBGA).



Features

- Complete Clock and Data Recovery IC with auto acquisition.
- 1:16 DeMUX with differential 622 Mbit/s data outputs
- 622 MHz Clock output.
- LVDS compatible clock and data outputs.
- OIF99.102.5 compliant timing.
- 155 or 622 MHz Reference Clock.
- Input Decision Threshold Control (DTC): ±40 mV.
- Low noise VCO with ±5 % tuning range.
- Dual supply operation: -5.2 V and +3.3 V.
- Power dissipation: 3.3 W (typ).
- Silicon Bipolar technology.
- 132 balls Ceramic BGA 13 × 13 mm package.
- Available in two versions:
  - GD16584 for 10 Gbit/s
  - GD16588 for 10.66 Gbit/s

Applications

- Telecommunication systems:
  - SDH STM-64
  - SONET OC-192.
  - Optical Transport Networking (OTN)
  - FEC applications
- Fibre optic test equipment.
- Submarine systems.

The application of GD16584 is as receiver in SDH STM-64 and SONET OC-192 optical communication systems.

It integrates:

- a Voltage Controlled Oscillator (VCO)
- a Bang Bang Phase Detector
- a Lock Detect Circuit
- a 1:16 DeMUX
- a Phase and Frequency Detector (PFD).

VCO

The VCO is an LC-type differential oscillator, voltage controlled by pin VCTL and with a tuning range of approximately ±5 %.

For GD16584, with the VCTL voltage at approximately -3.5 V, the VCO frequency is fixed at 9.953 GHz and by changing the voltage from 0 to -5.2 V the frequency is controlled from 8.9 GHz to 10.2 GHz. The modulation bandwidth of VCTL is 90 MHz.

PFD

The PFD ensures predictable locking conditions for the device. It is used during acquisition and pulls the VCO into the locking range where the Bang-Bang Phase Detector acquires lock to the incoming bit-stream. The PFD is made with digital set/reset cells giving it a true phase and frequency characteristic. The reference clock input (REFCK/REFCKN) to the PFD is differential and selectable between 155 MHz or 622 MHz by SEL3.

The reference clock is a CML input with 50 Ω internal termination resistors to 0 V. The reference clock is typically an X-tal oscillator type as shown in Figure 1. The reference clock input should be used differential for best performance. If the reference clock is DC coupled the input voltage swing is 0 V (high) and -0.4 V (low).

Bang-Bang Phase Detector

The Bang-Bang phase detector is designed as a true digital type producing a binary output. It samples the incoming data prior to, in the vicinity of and after any potential bit transition.

When a transition has occurred, these three samples tell whether the VCO clock leads or lags the data. The binary output is filtered through the (low pass) loop filter, performing an integration of all potential bit transitions. Hence the PLL is controlled by the bit transition point.

Loop Filter

A passive loop filter is used for the CMU consisting of a resistor and a capacitor driven from the PCTL pin. The PCTL pin outputs the phase information from the Bang-Bang Phase Detector. The phase information is very high frequency pulses (200 ps pulse width) either charging or discharging the external capacitor.

The values of the external components determines the characterisctics of the PLL, e.g. bandwidth and transfer functions. For recommended loop filter values, please refer to Figure 1.

The PCB lay-out of the external loop filter and the connecting lines between PCTL and VCTL are **critical** for jitter performance of the device. The external components and the artwork should be placed very close to the pins of the device.

If the PHIGH and PLOW outputs are not used they must be shorted VDD (0 V), please refer to Figure 1.

Lock Detect Circuit

The lock detect circuit continuously monitors the difference between the reference clock and the VCO clock. If they differ by more than 500 ppm (or 2000 ppm), it switches the PFD into the PLL, to pull it back into the locking range. The status of the lock circuit is given by output pin (LOCK). Manual or automatic lock is selected by SEL1. In auto lock mode, the lock range ±500 or ±2000 ppm is selected by SEL2. The LOCK output is an open collector output, and should be terminated with an external resistor. The maximum termination voltage is +3.5 V.

The Inputs

The input amplifier pin (DI/DIN) is designed as a gain buffer stage with high sensitivity and internal 50 Ω resistors terminated to 0 V. After retiming, the data is de-multiplexed down to 16 bit/s by demultiplexer.

It is recommended to use the 10 Gbit/s inputs differentially for best input sensitivity.

The input voltage decision threshold is adjustable by pin DTC and DTCN when connected to a potentiometer. Adjusting the resistor value of the meter controls the current into DTC and DTCN. This DC current is mirrored to the input pin (DI and DIN) whereby the DC bias voltage at the input is adjustable by ±40 mV. Optimizing the input decision threshold improves the system input sensitivity by 1-2 dB typical.

The input impedance into DTC and DTCN is 1.5 kΩ and when not used they should be de-coupled to 0 V by 100 nF.

The select inputs (SEL1-3, RESET and TCK) are low speed inputs that can be connected directly to the supply rails (0 / -5.2 V).

The 10 Gbit/s inputs **(DI and DIN) are not ESD protected** and extra precautions are needed when handling these inputs. (Internal 50 Ω resistors provide some ESD hardness making the input low impendance.)

Bit Order

The serial data stream is demultiplexed with the first received bit on DO0, the second on DO1 and with last received bit in a 16 bit frame on DO15. The naming is opposite to the OIF99.102.5 recommendation.

For OIF interfaces the data pins should be connected as shown in the following table.

Note: The clock output is inverted in order to refer the data crossing to the rising edge of CKOUTN

Output Pin:	**OIF:**
DO0/DON0	RXDATA15_P/N (MSB)
DO1/DON1	RXDATA14_P/N
DO2/DON2	RXDATA13_P/N
DO3/DON3	RXDATA12_P/N
DO4/DON4	RXDATA11_P/N
DO5/DON5	RXDATA10_P/N
DO6/DON6	RXDATA9_P/N
DO7/DON7	RXDATA8_P/N
DO8/DON8	RXDATA7_P/N
DO9/DON9	RXDATA6_P/N
DO10/DON10	RXDATA5_P/N
DO11/DON11	RXDATA4_P/N
DO12/DON12	RXDATA3_P/N
DO13/DON13	RXDATA2_P/N
DO14/DON14	RXDATA1_P/N

Output Pin:	OIF:
DO15/DON15	RXDATA0_P/N (LSB)
CKOUT	RXCLK_N
CKOUTN	RXCLK_P

The Outputs

The data and clock outputs are LVDS compatible outputs with internal bias resistors (500 Ω) to VCC (+3.3 V)

Refer to item “LVDS Compatible Interface” on page 6.

Timing to System ASIC

The timing between GD16584 and the system ASIC at 622 Mbit/s is controlled by the 622 MHz output clock synchronized with the output data. The clock is used as the input clock to the ASIC, clocking the input data into 16 parallel registers. The timing relation between the clock and data is given by the AC Characteristics.

For a OIF99.102.5 complaint timing the output clock should be inverted by using:

- **CKOUTN** as the *positive* output clock (RXCLK_P), and
- **CKOUT** as the *negative* output clock (RXCLK_N)

External Circuit

The external circuits needed to make the device work as a complete clock and data recovery with automatic acquisition are:

- A passive loop filter
- An X-tal oscillator or reference clock (155 MHz or 622 MHz)
- De-coupling capacitors

Package

The device is packaged in an 132 balls Ceramic BGA (13 × 13 mm). For the package outline, please refer to the figure on page 12.

The following pin pairs are individually shorted inside the package and mainly used as power pins:
C3/D3, C4/D4, C5/D5, C8/D8, C9/D9, C10/D10, J3/K3, J4/K4, J5/K5, J8/K8, J9/K9, and J10/K10.

Thermal Condition

The device dissipates 3.3 W from a dual voltage supply (–5.2 V and +3.3 V). The power consumption from the -5.2 V supply is approximately 2.9 W and 0.4 W from the +3.3 V supply.

The die is mounted in a cavity on a metal pad directly connected to the center balls (E4-9, F4-9, G4-9, and H4-9).

About 80% of the power is transferred through the balls of the package and 20% through the top lid.

The thermal resistance from the die (junction) to the back side of the package through the balls is 10-15 °C/W depending on the lay-out of the PCB. The thermal resistance from the die to the top side through the lid is 40 °C/W (the figures are measured values with the package mounted on the GD90584/585 Evaluation Board and with no air-flow).

The maximum allowed case temperature (on the top side) is 95 °C ensuring a die junction temperature below 125 °C, please refer to “Maximum Ratings” on page 9.

It is important to have a good thermal connection from the center balls of the package via the PCB to the ambient environment to ensure the case temperature in the range from 0 to 70 °C.

10.66 Gbit/s Application

A version of the transmitter with a bit rate of 10.66 Gbit/s for forward error correction application is available. The part number is GD16588.

The functionality and the pin-out are identically to GD16584.

The center frequency of the VCO (10.66 GHz) is the only difference to GD16584.

Applications

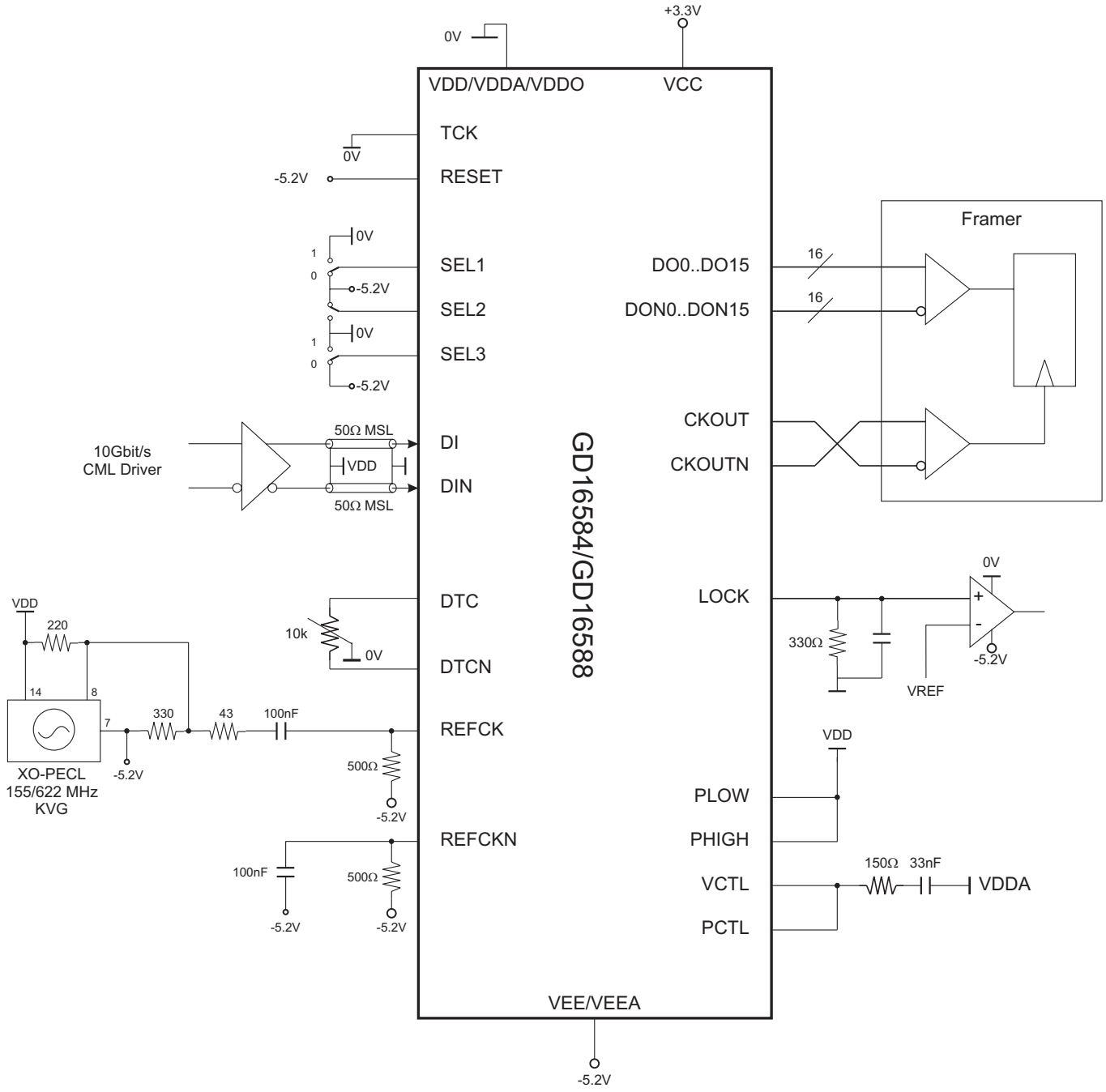


Figure 1. *Application Information.*

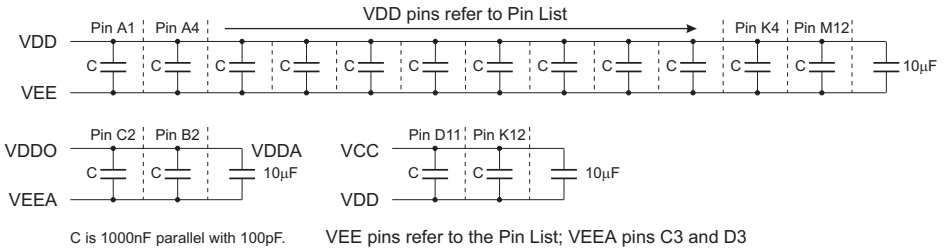


Figure 2. *De-coupling of the Power Supply.*

10 Gbit/s Input Interface

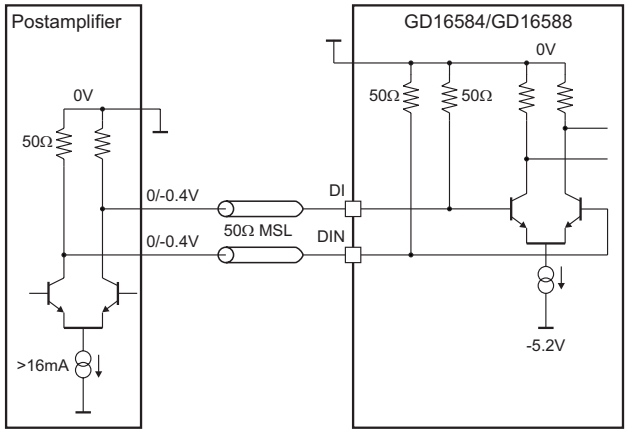


Figure 3. *10 Gbit/s Input (DI/DIN), DC Coupled*

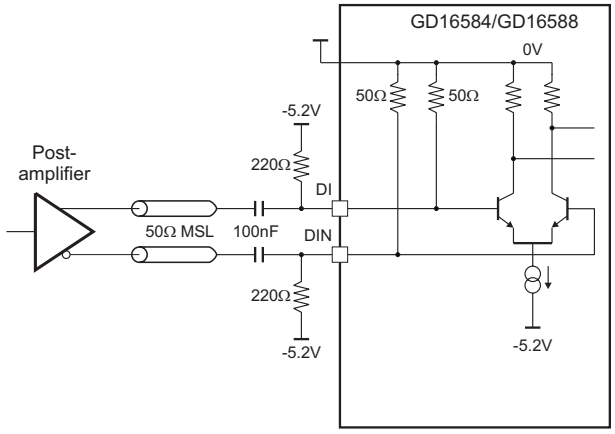


Figure 4. *10 Gbit/s Input (DI/DIN), AC Coupled*

LVDS Compatible Interface

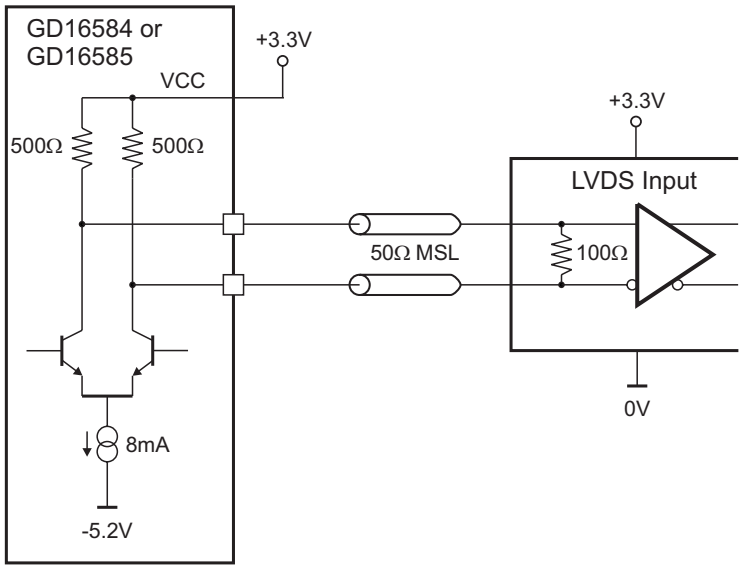


Figure 5. *LVDS Compatible Output.*

Reference Clock Input

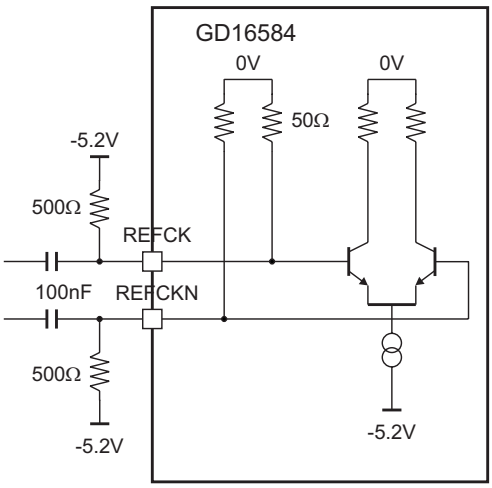


Figure 6. *Reference Clock Input (REFCK/REFCKN), Differential AC Coupled.*

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
DO0, DON0 DO1, DON1 DO2, DON2 DO3, DON3 DO4, DON4 DO5, DON5 DO6, DON6 DO7, DON7 DO8, DON8 DO9, DON9 DO10, DON10 DO11, DON11 DO12, DON12 DO13, DON13 DO14, DON14 DO15, DON15	A8, B8 A9, B9 A10, B10 A11, A12 C11, C12 D12, E12 G11, H12 J12, J11 M11, L10 M10, L9 M9, L8 L6, K6 M5, L5 L4, M3 M2, M1 K3, L2	LVDS Out	Data output, differential 622 Mbit/s. Demultiplexed to output with DO0, DO1...DO15 as first received bits. **Note:** The bit naming convention is opposite to OIF99.102.5: DO0 is MSB. Please refer to item “Bit Order” on page 2.
REFCK, REFCKN	A5, A6	CML In	Reference clock input, differential 155 MHz or 622 MHz.
SEL1, SEL2	C5, B5	ECL In	Clock and Data recovery setup. SEL1 SEL2 0 0 Auto Lock, 500 ppm. 0 1 Auto Lock, 2000 ppm. 1 0 Manual Phase Freq. Detector (PFD). 1 1 Manual Bang-Bang Phase Detector. When left open, the inputs are pulled to VDD.
SEL3	K11	ECL In	SEL3 0 155 MHz Reference Clock. 1 622 MHz Reference Clock. When left open, the input is pulled to VDD.
DI, DIN	H1, E1	CML In	Data input, differential 10 Gbit/s. **No ESD input protection.**
CKOUT, CKOUTN	L12, L11	LVDS Out	Clock output, differential 622 MHz. **Note**: The clock polarity is opposite to OIF99.102.5. Please refer to item “Bit Order” on page 2 and Figure 1.
LOCK	C6	Open Collector	Lock detect output. When low, the divided VCO frequency deviates more than 500/2000 ppm from REFCK/REFCKN, should always be terminated with a resistor to VDD.
PCTL	B3	Analogue Out	Charge pump output. Connected to an external passive loop filter.
VCTL	B1	Analogue In	VCO voltage control input.
DTC, DTCN	M6, K5	Analogue In	Decision threshold control.
(PHIGH, PLOW)	A3, B4	Open Collector	Not used. Always terminate to VDD.
TCK	C1	ECL In	Connect to VDD. Used for test purpose. When left open, the input is pulled to VDD.
RESET	L1	ECL In	Connect to VEE. Not needed on power up, used for test purpose.
VDD	A1, A4, B6, C10, D1-2, D6, D10, E4-9, F1-2, F4-9, F11, G1-2, G4-9, H4-9, J1-2, J4, J7, K4, M12	PWR	Digital Ground 0 V.
VDDA	B2	PWR	PLL Ground 0 V.
VDDO	C2	PWR	VCO Ground 0 V. For test purpose, connect to VEE.
VCC	D11, K12	PWR	+3.3 V Digital supply voltage.

Mnemonic:	Pin No.:	Pin Type:	Description:
VEE	C4, C8, D4, D7-8, J8-9, K1, K8-9	PWR	-5.2 V Digital supply voltage.
VEEA	C3, D3	PWR	-5.2 V PLL supply voltage.
NC	A2, A7, B7, B11-12, C7, C9, D9, F12, G12, J6, J10, K2, K7, K10, L3, L7, M4, M7-8,		Not Connected. Reserved for future use.
NC	D5, J3, J5		DO NOT CONNECT

Package Pinout

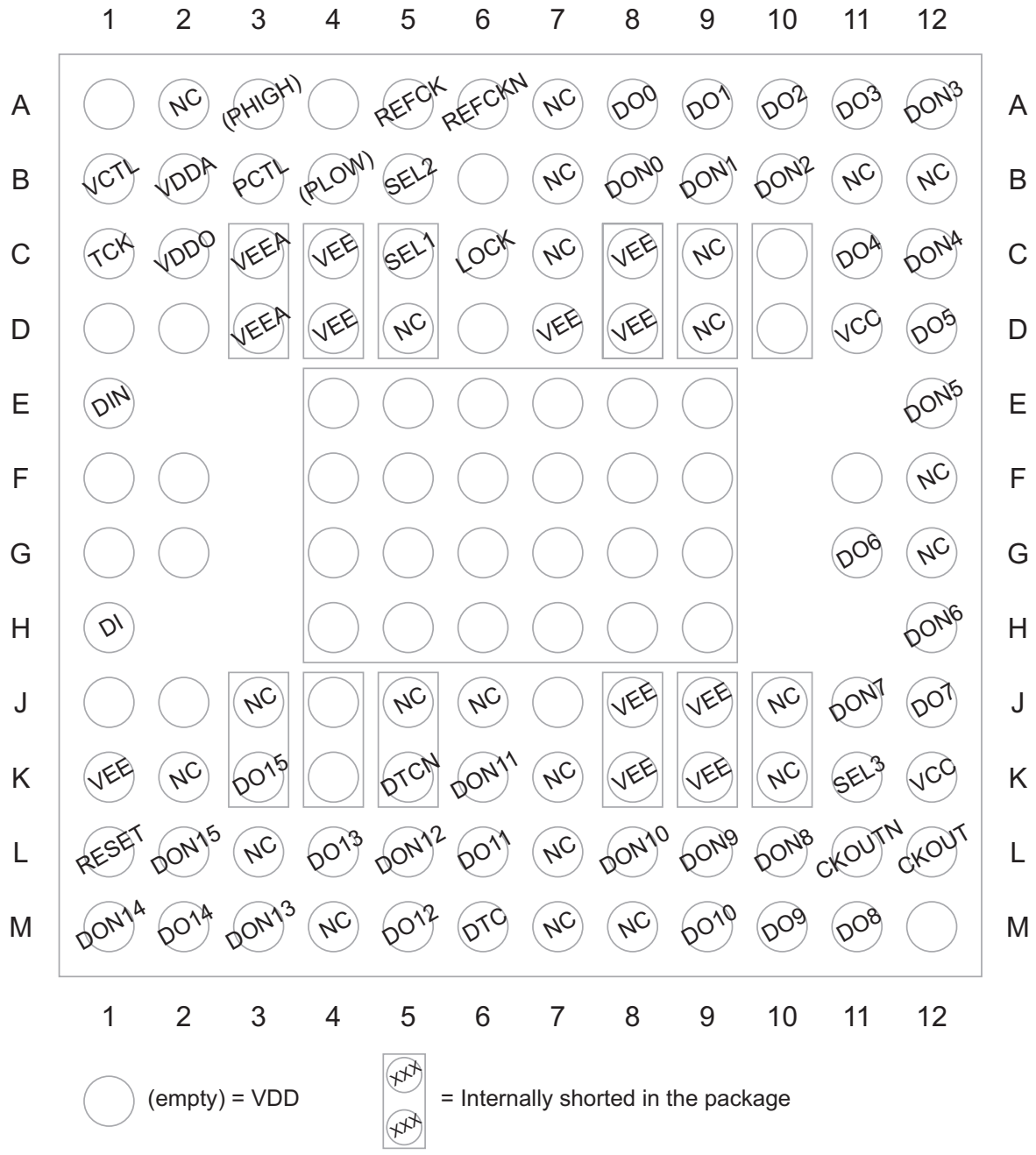


Figure 7. *Package Pinout. Top View - Seen Through the Package*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VDD.
All currents are defined positive out of the pin.
VDD is 0 V or GND.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Negative Supply		-6		0	V
V_{CC}	Positive Supply				+4	V
$V_{O\ LVDS}$	LVDS Output Voltage		0		V_{CC} +0.5	V
$I_{O\ LVDS}$	LVDS Output Current	Note 1	-24		24	mA
$V_{I\ CML,\ ECL}$	CML and ECL Input Voltage		V_{EE} +2		0.5	V
$I_{I\ CML}$	CML Input Current	Note 1	-24		24	mA
$V_{O\ OC}$	Open Collector Output Voltage		V_{EE} -0.5		0	V
$I_{O\ OC}$	Open Collector Output Current	Note 1	-12		0	mA
T_J	Junction Temperature	Note 2	-55		+125	°C
T_S	Storage Temperature		-65		+150	°C

Note 1: Nominal supply voltages.
Note 2: The maximum junction temperature equals a maximum case temperature of 95 °C (top side) with the device mounted on the GD90584/585 Evaluation Board.

DC Characteristics

T_{CASE} = 0 °C to 70 °C. VEE = -5.2 V, VCC = +3.3 V. VDD is 0 V or GND.
All voltages in table are referred to VDD.
All currents are defined positive out of pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Negative Supply Voltage		-5.46	-5.2	-4.94	V
I_{EE}	Negative Supply Current		455	550	660	mA
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Positive Supply Current		-180	-140		mA
$V_{OH\ LVDS}$	LVDS Output Voltage High	Note 7, V_{CC} = 3.3 V		1.4	1.5	V
$V_{OL\ LVDS}$	LVDS Output Voltage Low	Note 7, V_{CC} = 3.3 V	0.9	1.1		V
$V_{OD\ LVDS}$	LVDS Output Differential Voltage	Note 7, V_{CC} = 3.3 V	250	400	600	mV
$V_{IH\ CML}$	CML Input Voltage High		-0.1	0	+0.1	V
$V_{IL\ CML}$	CML Input Voltage Low		-1	-0.4	-0.25	V
$I_{IH\ CML}$	CML Input Current High	$V_{IH\ CML}$, 50 Ω input		0		mA
$I_{IL\ CML}$	CML Input Current Low	$V_{IL\ CML}$, 50 Ω input		8		mA
$R_{IN\ CML}$	CML Input Resistor Termination	DC	40	50	60	Ω
$I_{OH\ OC}$	Open Collector Output Current High	Note 1, 3	-0.1	0	+0.1	mA
$I_{OL\ OC}$	Open Collector Output Current Low	Note 1, 3	-10	-8	-7	mA
$V_{IH\ ECL}$	ECL Input Voltage High	Note 2, 5	-1.1		0	V
$V_{IL\ ECL}$	ECL Input Voltage Low	Note 2, 5	V_{EE}		-1.5	V
$I_{IH\ ECL}$	ECL Input Current High	V = -1.1 V			30	µA
$I_{IL\ ECL}$	ECL Input Current Low	V = -1.5 V			30	µA
VADS	Offset Adjustment by DTC/DTCN, Differential	Note 4, 6		±90		mV

Note 1: Output externally terminated by 50 Ω to 0 V.
Note 2: All ECL inputs can be connected directly to VDD/VEE.
Note 3: All open collector outputs should always be terminated with a resistor.
Note 4: With DTC and DTCN connected to a 10k potentiometer with the mid pin grounded (0 V).
Note 5: -5.0 V.
Note 6: With open data inputs.
Note 7: With 100 Ω termination resistor.

AC Characteristics

T_{CASE} = 0 °C to 70 °C. VEE = -5.2 V, VCC = +3.3 V.

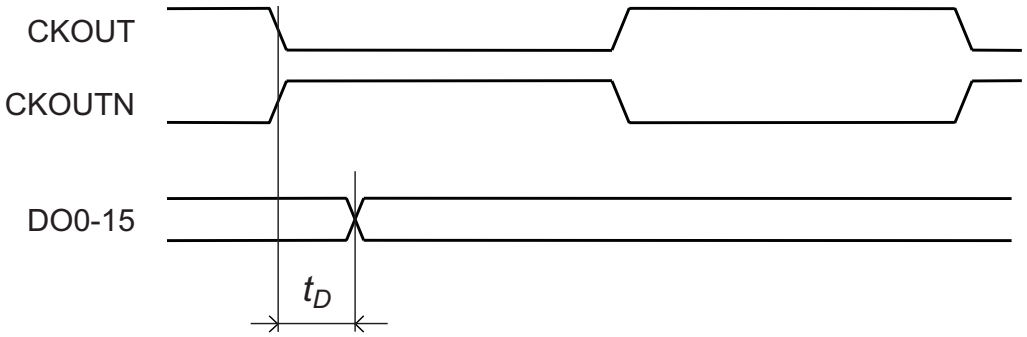


Figure 8. *OIF99.102.5 complaint timing relation between the negative output clock (CKOUTN) and output data (DO0-15).*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{Tol}	Jitter tolerance	f < 400 kHz 4 MHz < f Note 4	1.5 0.15			UI
t_D	Delay between DO0-15 and CKOUT/CKOUTN		0	120	200	ps
$V_{DI/DIN}$	Data input sensitivity, differential	Note 2		100		mV_{PP}
$\Gamma_{DI/DIN}$	DI/DIN input reflection coefficient	Note 3		-10		dB
$D_{CYCLE\ CKOUT/N}$	CKOUT/CKOUTN duty cycle		45		55	%
$F_{REFCK/N}$	REFCK/REFCKN frequency	Note 1		155/622		MHz
D_C	REFCK frequency deviation from nominal line frequency		-100		100	ppm
$D_{CYCLE\ REFCK/N}$	REFCK duty cycle		40		60	%

Note 1: Selectable by SEL3.
Note 2: BER = 10^{-9}
Note 3: From DC to 6 GHz. Depends on lead length, board, soldering etc. of the component.
Note 4: Measured with the recommended loop filter, see Figure 1.

Package Outline

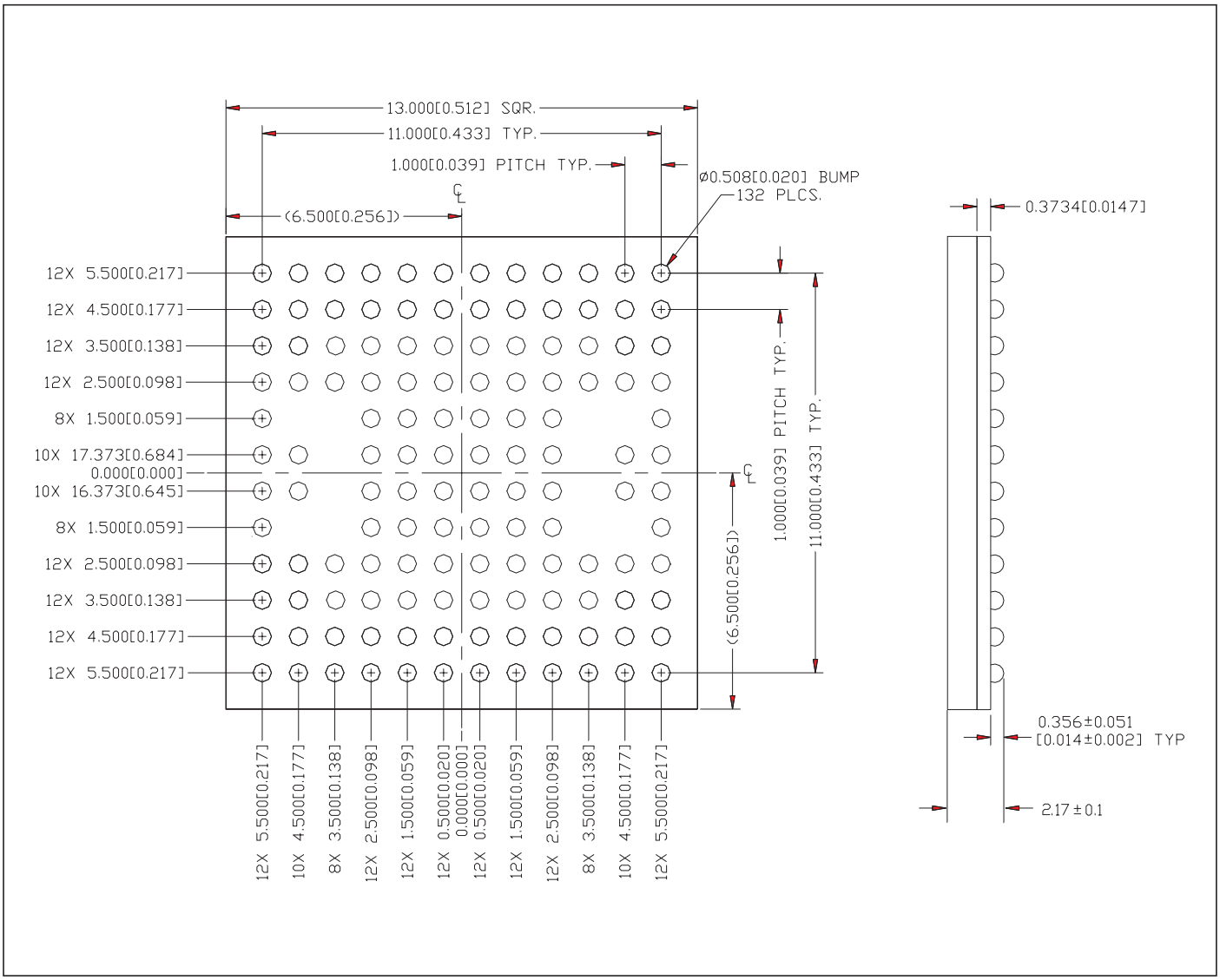


Figure 9. *Package 132 pin ceramic BGA. All dimensions are in mm.*

Device Marking

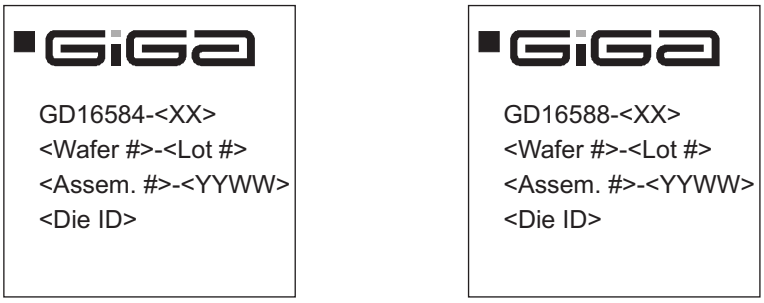


Figure 10. *Device marking. Top view. The black square marks location of ball A1.*

Ordering Information

To order, please specify as shown below:

Product Name:	Options:	Package Type:	Case Temperature Range:
GD16584-EB	10 Gbit/s	132 balls Ceramic BGA	0..70 °C
GD16588-EB	10.66 Gbit/s	132 balls Ceramic BGA	0..70 °C

Mileparken 22, DK-2740 Skovlunde
Denmark
Phone : +45 7010 1062
Fax : +45 7010 1063
E-mail : sales@giga.dk
Web site : http://www.giga.dk

Please check our Internet web site for latest version of this data sheet.

Distributor: