ASYNCHRONOUS SRAM

128K x 8 SRAM

WITH TWO CHIP ENABLE
TRADITIONAL PINOUT

FEATURES

- Fast access times: 10, 12, 15and 20ns
- Fast OE# access times: 5, 6, 7 and 8ns
- Single +5V ±10% power supply
- Fully static -- no clock or timing strobes necessary
- All inputs and outputs are TTL-compatible
- Three state outputs
- Easy memory expansion with CE1#, CE2 and OE# options
- High-performance, low-power consumption, CMOS double-poly, double-metal process

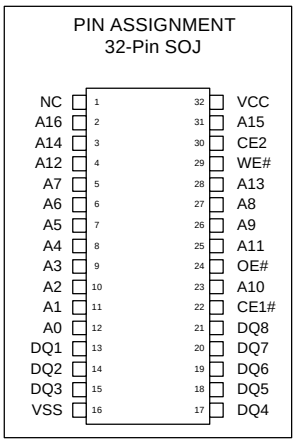
OPTIONS	MARKING	
• Timing		
10ns access	-10	
12ns access	-12	
15ns access	-15	
20ns access	-20	
• Packages		
32-pin SOJ (400 mil)	J	
32-pin SOJ (300 mil)	SJ	
32-pin TSOP (type I)	TS	
• Power consumption		
Standard	None	
Low	L	
• Temperature		
Commercial	None	(0°C to 70°C)
Industrial	I	(-40°C to 85°C)

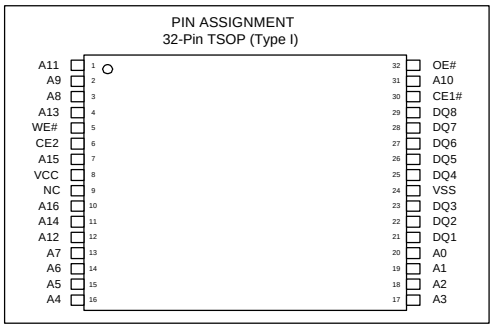
GENERAL DESCRIPTIO N

The GVT72024A8 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high performance, silicon gate, low-power CMOS process. Galvantech SRAMs are fabricated using double-layer polysilicon, double-layer metal technology.

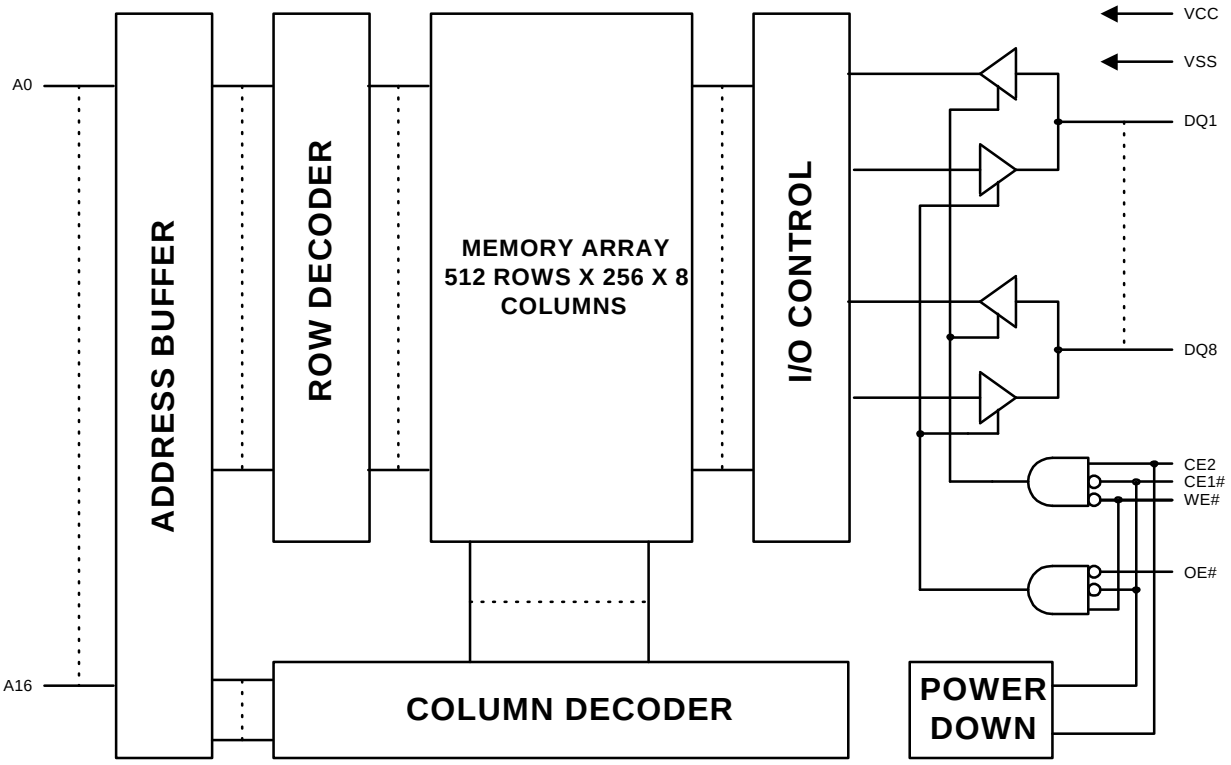
Static design eliminates the need for external clocks or timing strobes. For increased system flexibility and eliminating bus contention problems, this device offers two chip enables (CE1# and CE2) along with output enable (OE#) for this organization.

The chip is enabled when CE1# is LOW and CE2 is HIGH. With chip being enabled, writing to this device is accomplished when write enable (WE#) is LOW and reading is accomplished when (OE#) go LOW with (WE#) remaining HIGH. The device offers a low power standby mode when chip is not selected. This allows system designers to meet low standby power requirements.





FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	CE1#	CE2	WE#	OE#	DQ	POWER
READ	L	H	H	L	Q	ACTIVE
WRITE	L	H	L	X	D	ACTIVE
OUTPUT DISABLE	L	H	H	H	HIGH-Z	ACTIVE
STANDBY	H	X	X	X	HIGH-Z	STANDBY
STANDBY	X	L	X	X	HIGH-Z	STANDBY

PIN DESCRIPTIONS

SOJ & DIP Pin Numbers	TSOP Pin Numbers	SYMBOL	TYPE	DESCRIPTION
12, 11, 10, 9, 8, 7, 6, 5, 27, 28, 23, 25, 4, 28, 3, 31, 2	20, 19, 18, 17, 16, 15, 14, 13, 3, 2, 31, 1, 12, 4, 11, 7, 10	A0-A16	Input	Addresses Inputs: These inputs determine which cell is addressed .
29	5	WE#	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. WE# is LOW for a WRITE cycle and HIGH for a READ cycle .
22, 30	30, 6	CE1#, CE2	Input	Chip Enables: These inputs are used to enable the device. When CE1# is LOW and CE2 is HIGH, the chip is selected. When either CE1# is HIGH or CE2 is LOW, the chip is disabled and automatically goes into standby power mode .
24	32	OE#	Input	Output Enable: This active LOW input enables the output drivers .
13, 14, 15, 17, 18, 19, 20, 21	21, 22, 23, 25, 26, 27, 28, 29	DQ1-DQ8	Input/ Output	SRAM Data I/O: Data inputs and data outputs
32	8	VCC	Supply	Power Supply: 5V ±10%
16	24	VSS	Supply	Ground

ABSOLUTE MAXIMUM RATINGS *

Voltage on VCC Supply Relative to VSS.....-0.5V to +7.0V
V_{IN} .....-0.5V to VCC+0.5V
Storage Temperature (plastic) .....-55°C to +125°
Junction Temperature .....+125°
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITION S

(All Temperature Ranges; VCC = 5V ±10% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) voltage		V_{IH}	2.2	VCC+1	V	1, 2
Input Low (Logic 0) Voltage		V_{II}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-5	5	uA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ VCC	IL_O	-5	5	uA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		VCC	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	POWER	-10	-12	-15	-20	UNITS	NOTES
Power Supply Current: Operating	Device selected; CE1# ≤ V_{IL} & CE2 ≥ V_{IH}; VCC =MAX; f=f_{MAX}; outputs open	Icc	80	standard	210	180	150	110	mA	3, 14
				low	200	170	140	110		
TTL Standby	CE1# ≥V_{IH} or CE2 ≤V_{IL}; VCC = MAX; f=f_{MAX}	I_{SB1}	20	standard	60	55	50	40	mA	14
				low	45	40	35	30		
CMOS Standby	CE1# ≥VCC -0.2 or CE2≤ VSS +0.2; VCC = MAX; all other inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; f= 0	I_{SB2}	0.02	standard	10	10	10	10	mA	14
				low	1.0	1.0	1.0	1.0		

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz VCC = 5V	C_I	6	pF	4
Input/Output Capacitance (DQ)		$C_{I/O}$	8	pF	4

AC ELECTRICAL CHARACTERISTICS

(Note 5) (All Temperature Ranges; VCC = 5V ±10%)

DESCRIPTION		- 10		- 12		- 15		- 20			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAN	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	10		12		15		20		ns	
Address access time	^tAA		10		12		15		20	ns	
Chip Enable access time	^tACE		10		12		15		20	ns	
Output hold from address change	^tOH	3		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	3		4		4		4		ns	4, 7
Chip disable to output in High-Z	^tHZCE		5		6		7		8	ns	4, 6, 7
Output Enable access time	^tAOE		5		6		7		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output Enable to output in High-Z	^tHZOE		5		6		7		8	ns	4, 6
Chip Enable to power-up time	^tPU	0		0		0		0		ns	4
Chip disable to power-down time	^tPD		10		12		15		20	ns	4
WRITE Cycle											
WRITE cycle time	^tWC	10		12		15		20		ns	
Chip Enable to end of write	^tCW	8		8		9		10		ns	
Address valid to end of write, with OE# HIGH	^tAW	8		8		9		10		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP2$	10		10		11		12		ns	
WRITE pulse width, with OE# HIGH	$^tWP1$	8		8		9		10		ns	
Data setup time	^tDS	6		6		7		8		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		4		5		5		ns	4, 7
Write Enable to output in High-Z	^tHZWE		5		6		7		8	ns	4, 6, 7

AC TEST CONDITIONS

Input pulse levels	0V to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

OUTPUT LOADS

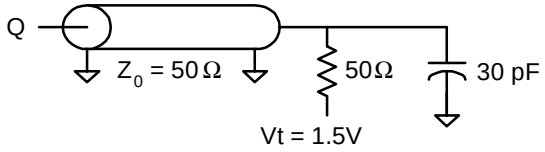


Fig. 1 OUTPUT LOAD EQUIVALENT

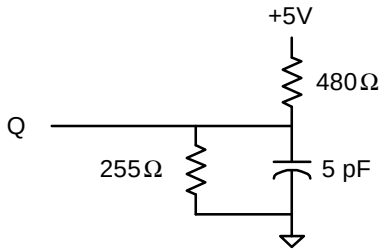


Fig. 2 OUTPUT LOAD EQUIVALENT

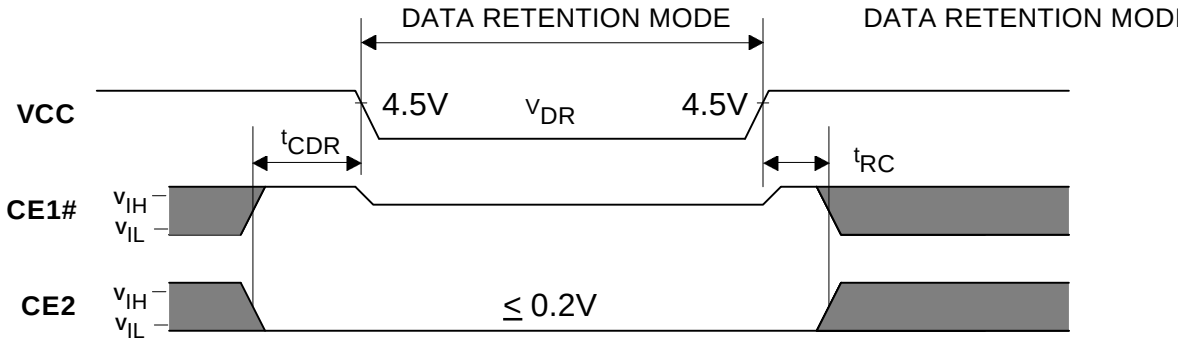
NOTES

1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH} \leq +7.0V$ for $t \leq {}^tRC/2$.
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tRC/2$
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L=5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. WE# is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip Enable and Write Enable can initiate and terminate a WRITE cycle.
13. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

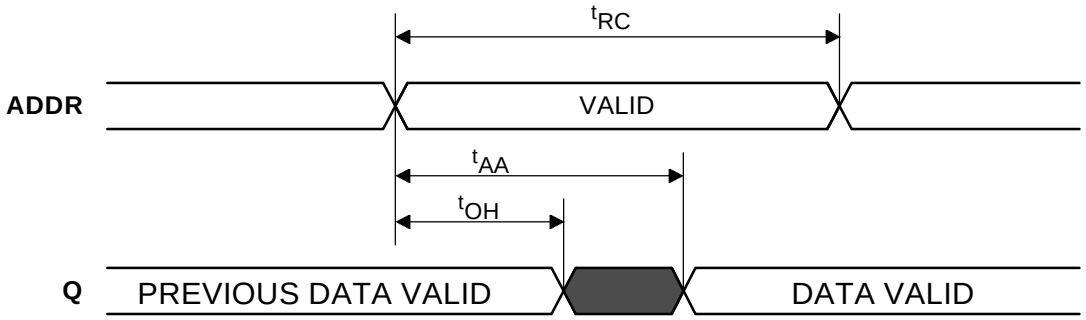
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	CE1# ≥VCC -0.2 or CE2≤ VSS +0.2; all other inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; f= 0	Vcc = 2V	I_{CCDR}		2	400	uA	13
		Vcc = 3V	I_{CCDR}		3	600	uA	13
Chip Deselect to Data Retention Time			t_{CDR}	0			ns	4
Operation Recovery Time			t_R	t_{RC}			ns	4, 11

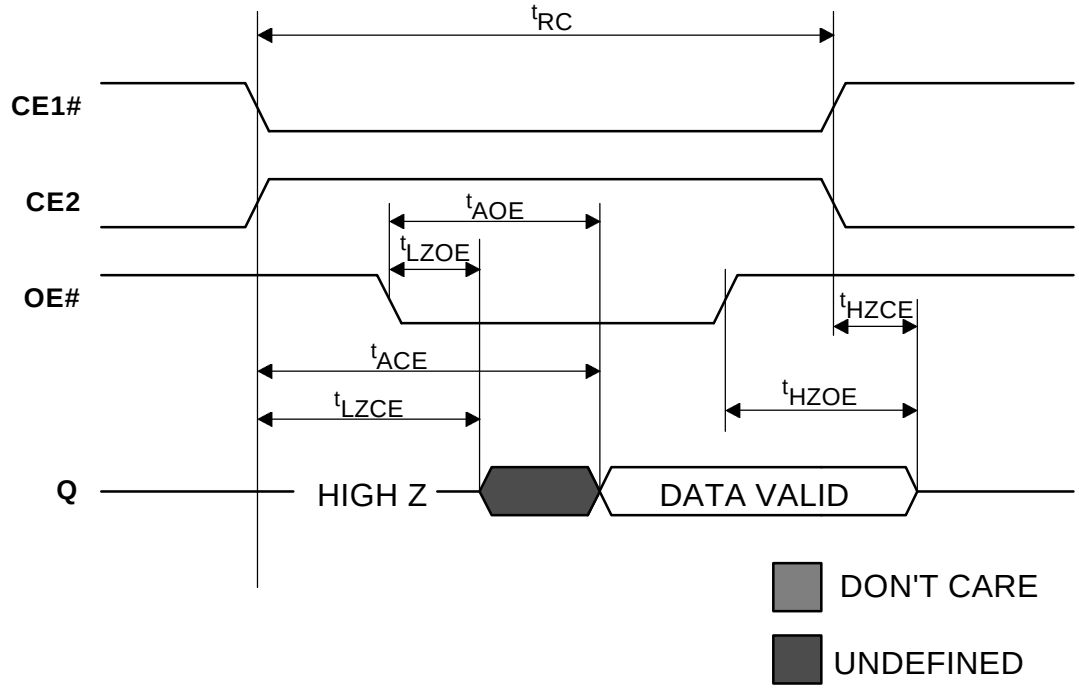
LOW VCC DATA RETENTION WAVEFORM



READ CYCLE NO. 1 (8, 9)

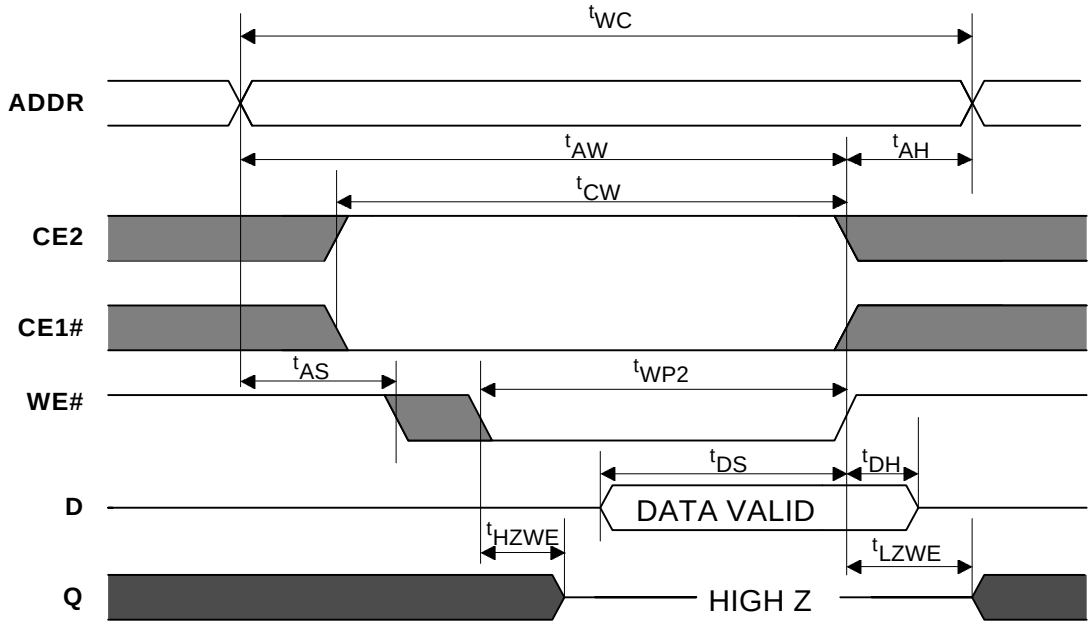


READ CYCLE NO. 2 (7, 8, 10, 12)



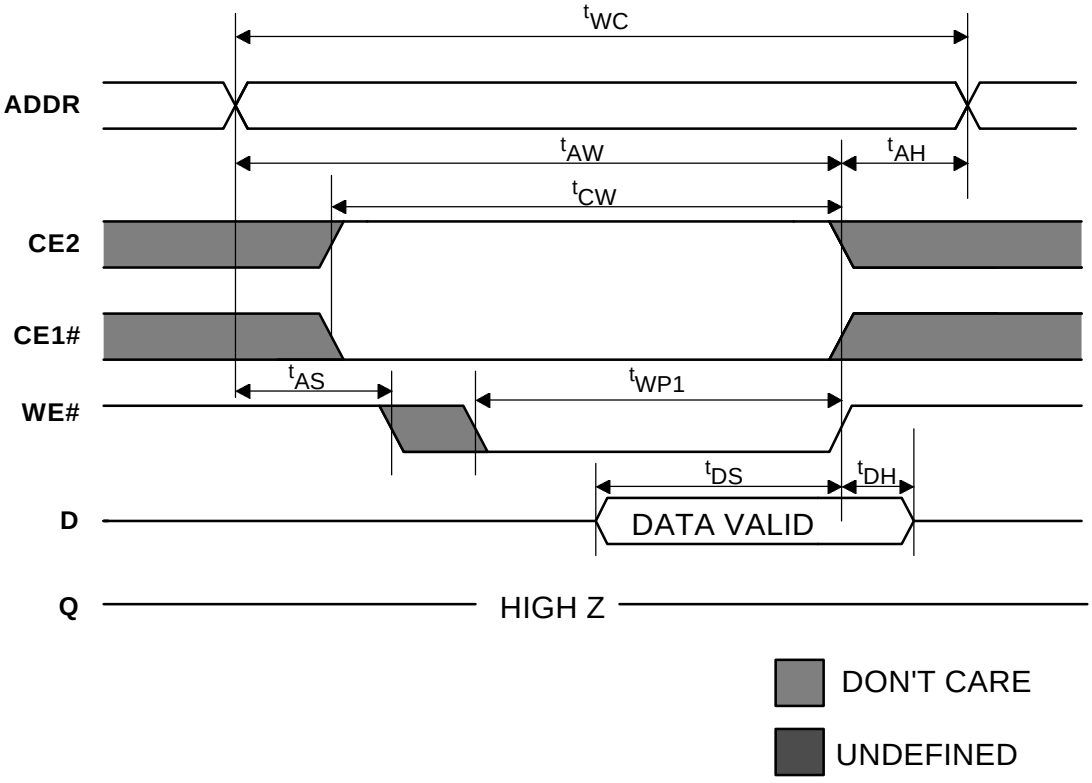
WRITE CYCLE NO. 1 (7, 12, 13)

(Write Enable Controlled with Output Enable OE# active LOW)

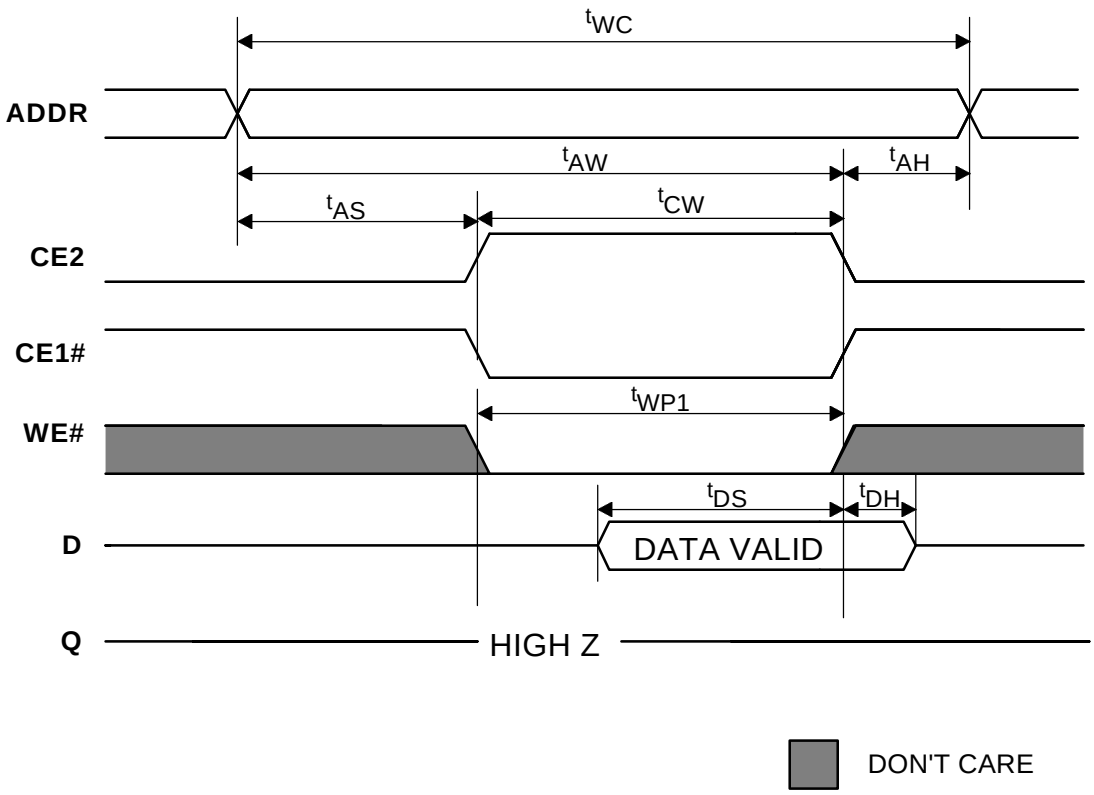


WRITE CYCLE NO. 2 (12, 13)

(Write Enable Controlled with Output Enable OE# inactive HIGH)

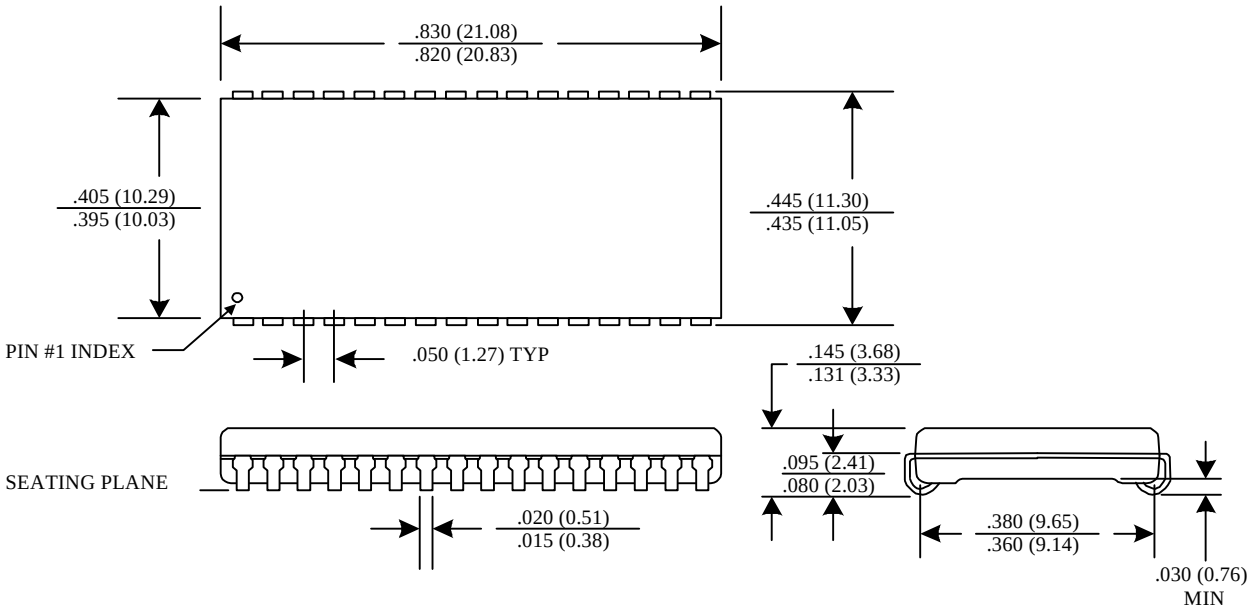


WRITE CYCLE NO. 3(12, 13)
(Chip Enable Controlled)



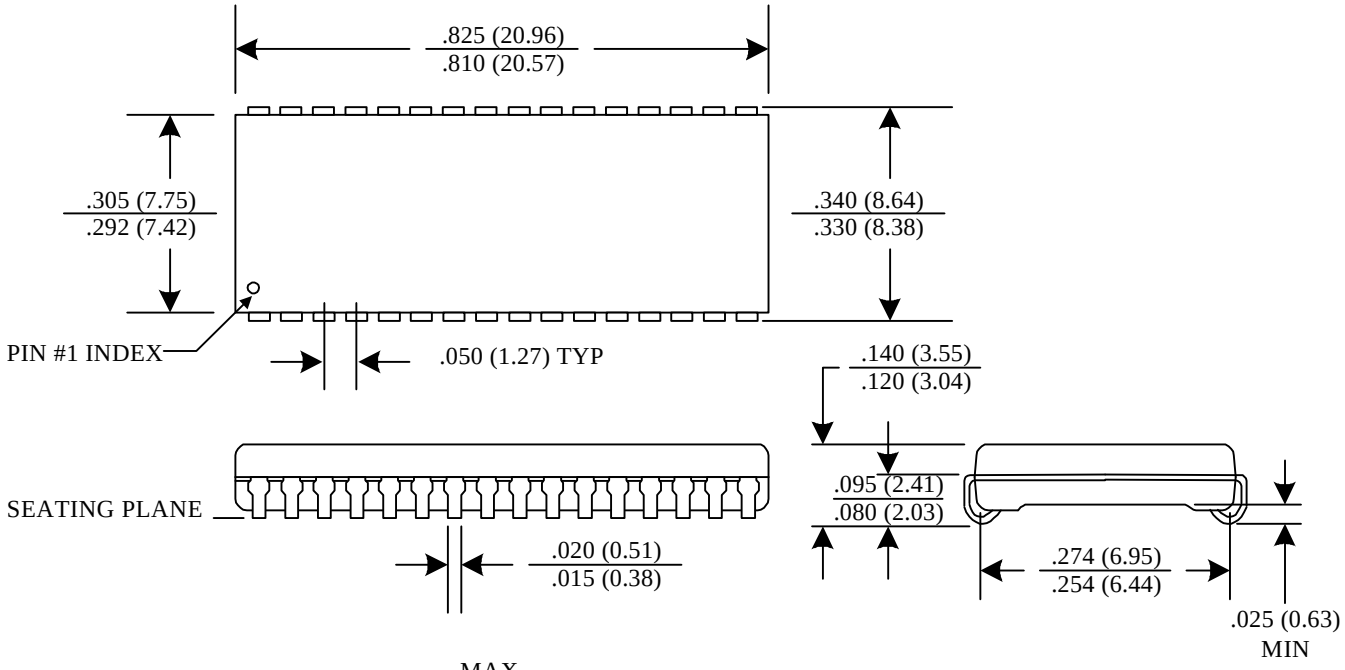
Package Dimensions

32-pin 400 Mil Plastic SOJ (J)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, min where noted.

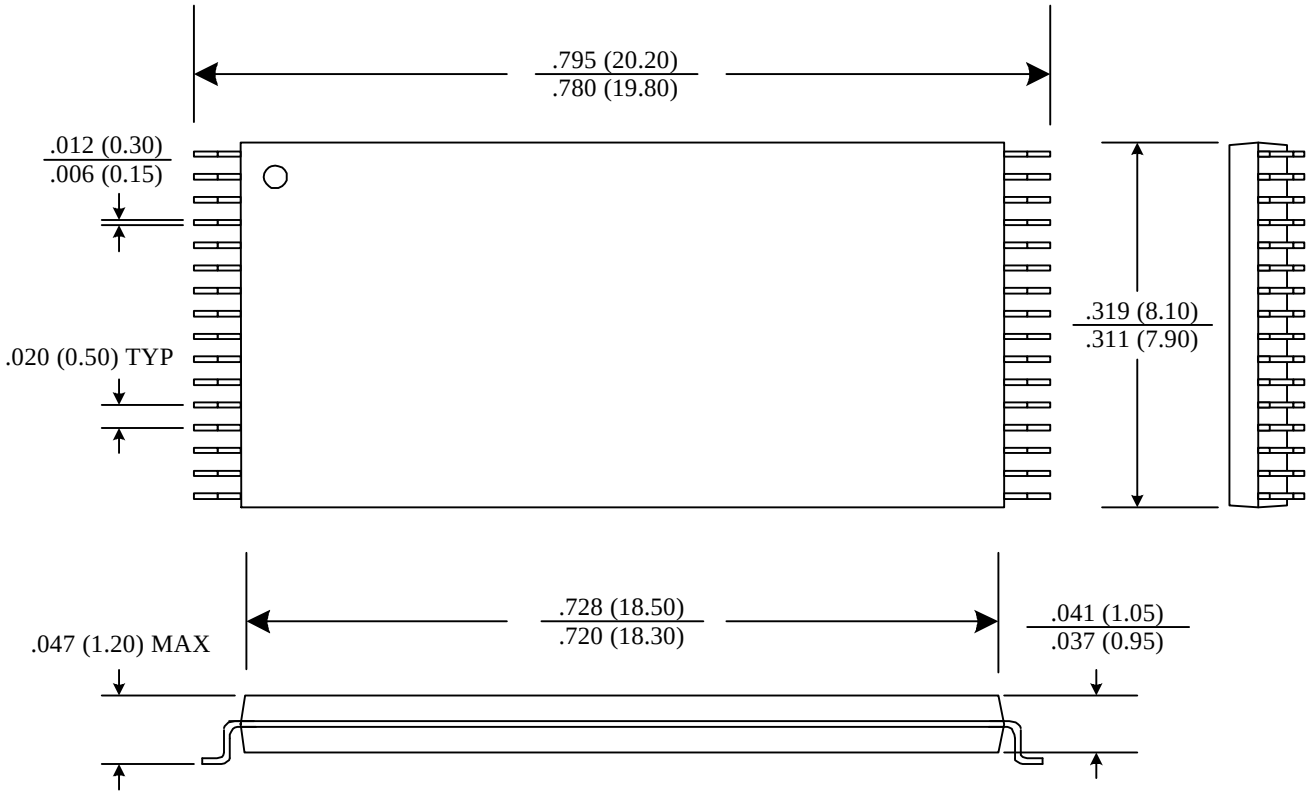
32-pin 300 Mil Plastic SOJ (SJ)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, min where noted.

Package Dimensions (continued)

32-pin Plastic TSOP (TS)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, max where noted.

Ordering Information

GVT 72024A8 XX - XX X X

- Galvantech Prefix
- Part Number
- Temperature (Blank = Commercial, I = Industrial)
- Power (Blank= Standard, L= Low Power)
- Speed (10 = 10ns, 12= 12ns, 15 = 15ns, 20 = 20ns)
- Package (J = 400 mil SOJ, SJ= 300 mil SOJ, TS= TSOP TYPE I)