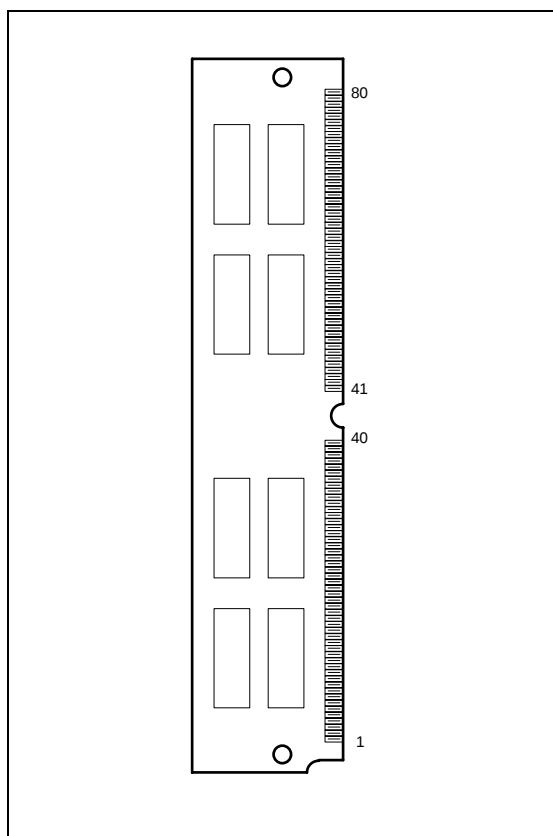


8 MByte SIMM FLASH MEMORY MODULE

PRELIMINARY DATA

- 80 PINS JEDEC 21-C package
- FAST ACCESS TIME: 70ns
- $5V \pm 10\%$ SUPPLY VOLTAGE for PROGRAM and ERASE OPERATIONS
- $5V \pm 10\%$ SUPPLY VOLTAGE in READ OPERATIONS
- BYTE PROGRAMMING TIME: 10 μ s typical
- ERASE TIME
 - Sector: 1.0 sec typical
 - Bulk: 2.5 sec typical
- PROGRAM/ERASE CONTROLLER (P/E.C.)
 - Program Byte-by-Byte
 - Data Polling and Toggle Protocol for P/E.C. Status
- MEMORY ERASE in SECTORS
 - 8 Sectors of 64K Bytes each
 - Sector Protection
 - Multisector Erase
- ERASE SUSPEND and RESUME MODES
- 100,000 PROGRAM/ERASE CYCLES per SECTOR


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ31	Data Input / Outputs
CE0-CE3	Chip Enable
OE	Output Enable
WE0-WE3	Write Enable
PD1-PD4	Presence & Module Type Detect
PD5-PD7	Module Speed Detect
VCC-VSS	Power Supply - Ground

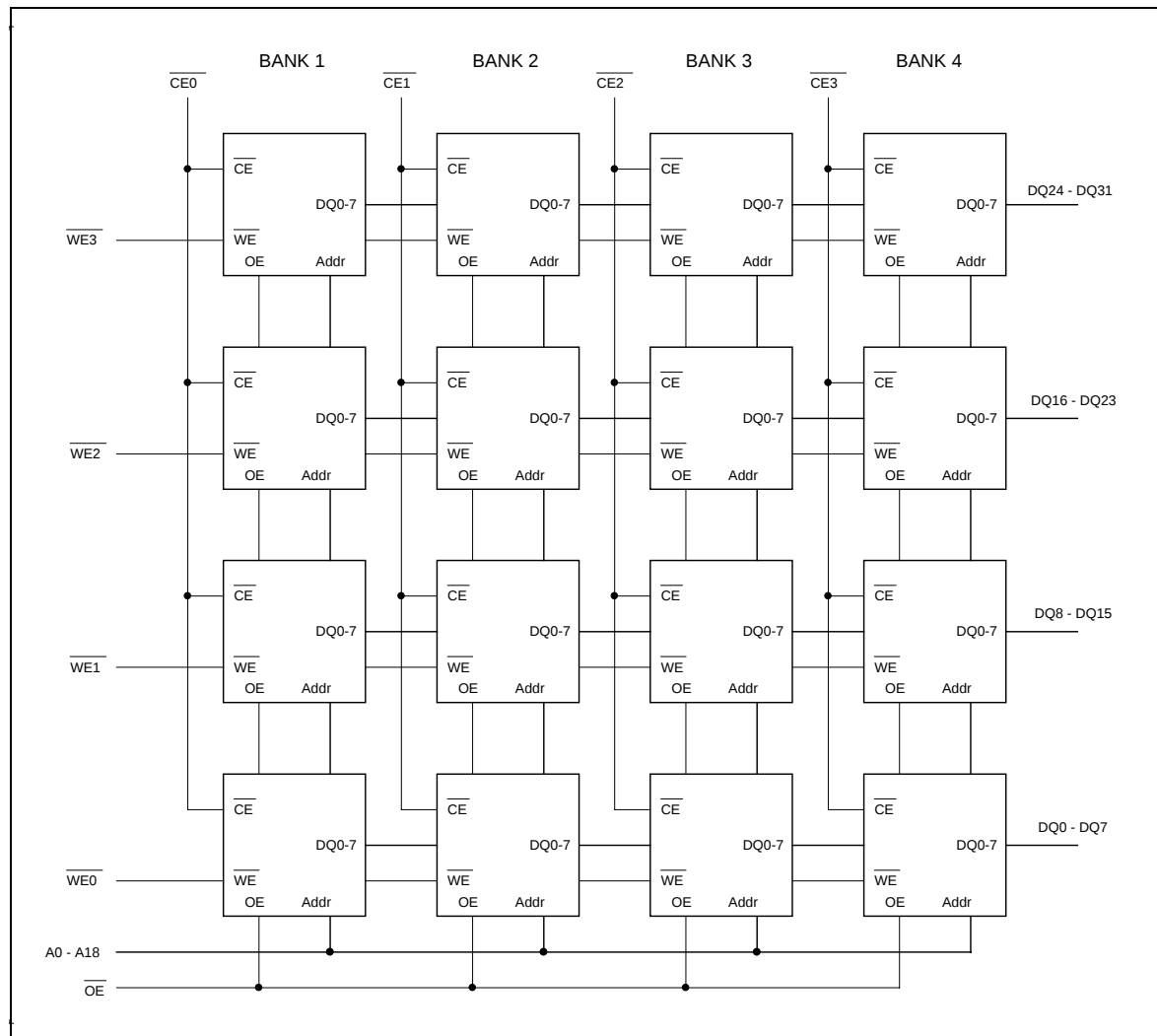
DESCRIPTION

The GS-F8MB-SIMM is an 8 Mbyte SIMM memory module built around 16 x M29F040 FLASH memory chips (please see relevant data sheet for all detailed informations about the chip performances). The devices are mounted on a Jedec 21-C standardized SIMM printed circuit.

Organisation

Figure 1 shows the block diagram. The FLASH module is organized as 16 x 512K x 8 bits with address lines A0-A18 and Data Inputs/Outputs DQ0 to 7, DQ8 to 15, DQ16 to 23 and DQ24 to 31.

Fig. 1. Block diagram



Memory control is provided by 4 Chip Enable (CE0, 1,2,3) inputs used to address the 4 memory banks and by 4 Write Enable inputs used to select through the DQ..... groups. An Output Enable input is used to read the stored data.

Erase and Program Functions are performed through the internal Program/Erase Controller (P/E.C.).

The Data Output chip bits DQ7 and DQ6 (and the corresponding DQ15 & 14, DQ23 & 22, DQ31 & 30) provide polling or toggle signals during Automatic

Program or Erase to indicate the Ready/Busy state of the internal Program/Erase Controller.

Configuration & speed pins

PD1-PD7 pins are used by the SIMM module to inform the motherboard about its relevant configuration and also about the speed of the chips used, as specified in the Jedec 21-C standard.

As the module allocates 8Mbyte memory, using 70 ns chips, configuration is the following:

PD1 : Vss PD2 : NC PD3 : NC PD4 : Vss
PD5 : NC PD6 : NC PD7 : Vss

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