10 Gbit/s Limiting Amplifier GD19908

Preliminary

General Information

GD19908 is a wide bandwidth Limiting Amplifier (LIA) intended to be used in OC-192/STM-64 receiver applications.

The typical linear gain is higher than 40 dB.

The LIA accepts input signals up to 2 V_{PP} with differential input data. Single-ended operation maximum 1 V_{PP}.

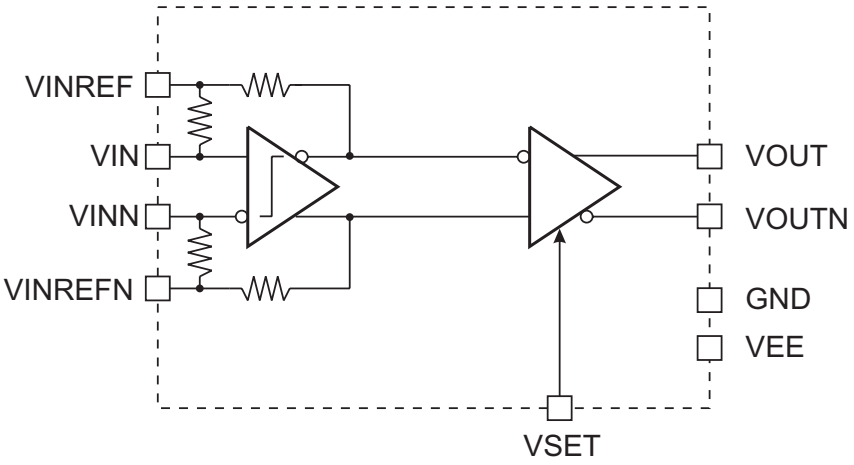
The output swing is controlled by the VSET voltage and can be varied from 0 and up to 1 V_{PP}.

Input and output is internally terminated with 50 Ω.

It uses a single power supply of –5.2 V and consumes only 260 mW (typ.).

The GD19908 features an active internal offset cancellation circuitry.

GD19908 is delivered in a 16 pin Ceramic QFP.



Features

- Differential or single-ended Input and Output.
- Gain: 40 dB @ 2.5 GHz (typ.).
- Large dynamic range: > 50 dB
- Large output swing: 0 – 1 V_{PP} adjustable
- Rise/Fall times, typ.: 38 ps (20 - 80%)
- Sensitivity: 2 × 5 mV_{PP} (10 mV_{PP} single ended) with good SNR into GD16584 or GD16588 DeMUX.
- Single power supply: –5.2 V
- Low power consumption: 260 mW (typ.); 800 mW (max.)
- Package: .16 pin Ceramic QFP (5.8 × 5.8 mm)

Applications

- Telecommunications systems:
  - SDH STM-64
  - SONET OC-192
- WDM systems
- 10 Gbit/s receivers
- 10 Gbit/s with 7% FEC

Application Information

Inputs

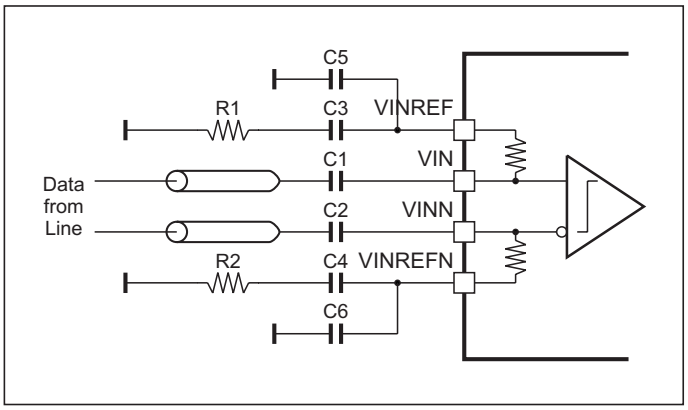
The inputs of GD19908 may be either AC or DC coupled. In either case input termination is made through the pins VINREF/ VINREFN which must be terminated through the external resistors (R1 and R2) and de-coupled to ground with capacitors (C3 and C6), as shown in the Figure1 .

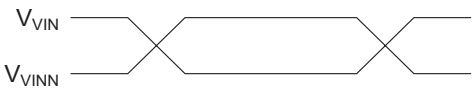
If the inputs are AC coupled GD19908 features an internal offset cancelling DC feedback. Because of the voltage division between the capacitors C3 and C1, (which must have the same value) on VIN / VINREF and C4 and C2 (which also must have the same value) on VINN / VINREFN, the lower cut-off frequency is in the kHz range. Notice that the offset cancellation will only work if VINREF and VINREFN are not shorted together, and if the inputs are AC coupled, as shown in the Figure 1.

R1 = R1 = 10 Ω
C3 = C4 = C5 = C6 = 100 nF

When single-ended input is required, the unsused input should be terminated with 50 Ω to ground. Figure 3 shows set-ups for DC and AC- coupled inputs.

For optimum sensitivity of the decision circuit following GD19908 external offset control can be applied as shown in Figure 4. This scheme can be applied on DC and AC- coupled inputs as well as single-ended and differential.





$$V_{diff} = |V_{VIN} - V_{VINN}|$$

$$V_{CM} = \frac{V_{VIN} + V_{VINN}}{2}$$

Figure 1. *AC coupled input*

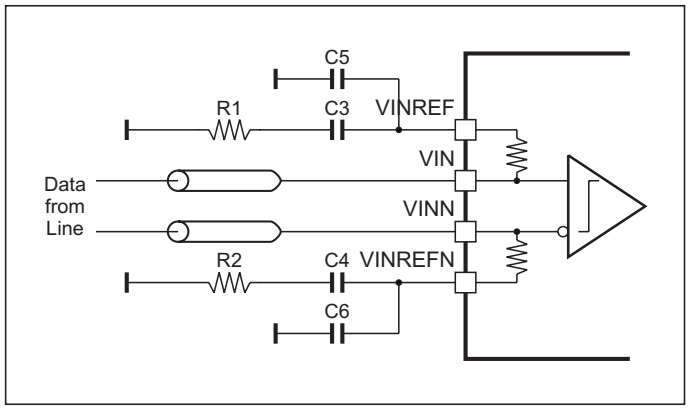


Figure 2. *DC coupling for large input amplitude*

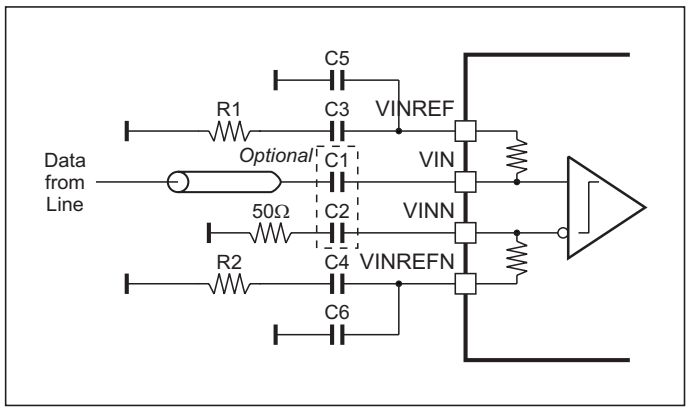


Figure 3. *Single-ended input.*
Use optional capacitors (C1 and C2) for AC-coupled inputs.

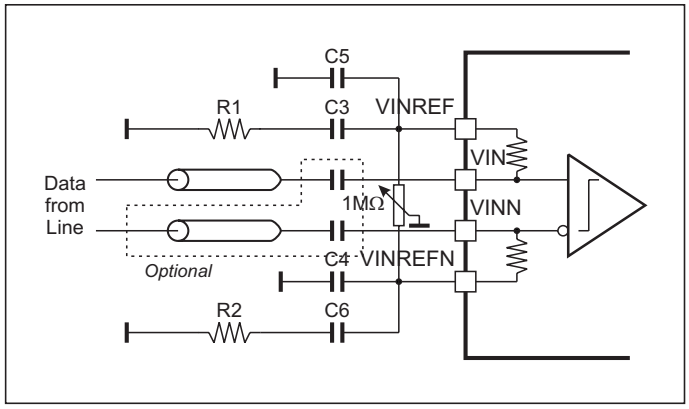


Figure 4. *External offset.*

Outputs

The outputs have 50 Ω termination internally and can be AC- or DC coupled.

When used with GD16584 or GD16588, best sensitivity is obtained with adjustable output set to approximately 400 mV amplitude (or 600 mV_{PP}). GD19908 can be coupled directly to GD16584 or GD16588 as shown in Figure 5.

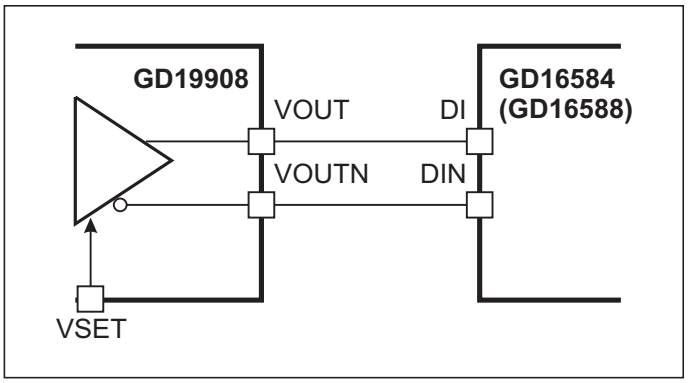


Figure 5. *Using GD19908 as pre-amplifier to GD16584 (GD16588), 10 (10.7) Gbit/s CDR/DeMUX*

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
VIN, VINN	14, 15	Analog Input	Differential Data Input
VOUT, VOUTN	7, 6	Analog Output	Differential Data Output
VSET	11	Analog Input	Output Swing Control
VINREF, VINREFN	12, 1	Analog Input	Input Voltage References
VEE	2, 3	PWR	Negative Supply Rail
GND	4, 5, 8, 9, 13, 16	PWR	Ground
NC	10		Reserved for future use. Do not connect.

Package Pinout

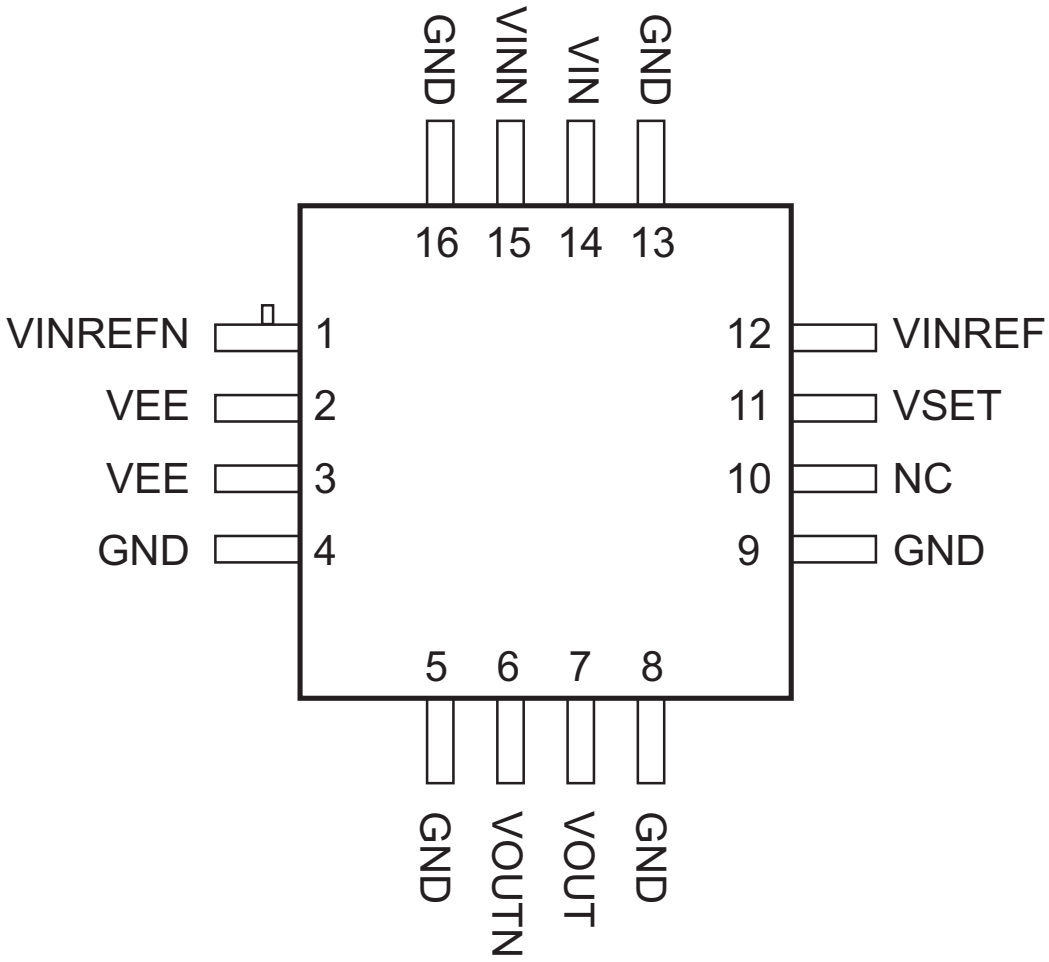


Figure 6. *Package pinout. Top View*

Maximum Ratings

Symbol:	Characteristics:	Conditions:	MIN.:	TYP.:	MAX.:	Units
V_{EE}	Negative supply		-6.5		0	V
$T_{J\ MAX}$	Maximum junction temperature		-		150	°C
T_S	Storage temperature		- 65		+125	°C
VSET	Input level		-6.5		+0.5	V
$V_{IN,\ INN\ MAX}$	Input level	Note 1	-3		+0.5	V

Note1: With VINREF and VINREFN open.

Environmental

ESD: >500 V, input protected to <100 V only.

DC Characteristics

The following data specifies the DC characteristics of the limiting amplifier IC over the operating temperature range from 0 to 70 °C case temperature, V_{EE} = -5.2 V.

Symbol:	Characteristics:	Conditions:	MIN.:	TYP.:	MAX.:	Units:
V_{EE}	Supply voltage		-4.9	-5.2	-5.5	V
I_{EE}	Negative supply current			50	155	mA
P_{DISS}	Power dissipation			260	800	mW
V_{DIN}, V_{DINN}	Quiescent input voltages	Note 4		-1.6		V
V_{OUT}, V_{OUTN}	Quiescent output voltages	Note 4		-0.5		V
$V_{INOFFSET}$	Input offset	Note 1		0		mV
$V_{OUTOFFSET}$	Output offset	Note 2		0		mV
V_{SET}	VSET control line	Note 3	-2.5		0.0	V

Note 1: DC difference between VIN & VINN for zero output offset, @ maximum gain. AC-coupled I/O's.
Note 2: DC difference between VOUT & VOUTN with zero input offset, @ maximum gain. AC-coupled I/O's.
Note 3: VSET = -2.5 V (V_{EE} +2.6 V) or VSET open gives minimum output. VSET = 0 V gives maximum output.
Note 4: I/O's open.

AC Characteristics

The following data specifies the DC characteristics of the limiting amplifier IC over the operating temperature range from 0 to 70 °C case temperature, V_{EE} = -5.2 V.

Symbol:	Characterisitcs	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
NF	Noise figure	2.5 GHz			15	dB
ΔG	Gain flatness	DC - 6 GHz		2		dB
GAIN MAX	AC gain (S21)	@ 2.5 GHz VSET = 0 V		40		dB
	S22	DC - 6 GHz		-10		dB
	S11	DC - 6 GHz		-10		dB
$V_{IN,\ P-P}$	Input peak-to-peak swing	Differential			2.0	V_{p-p}
$V_{OUT,\ P-P}$	Output peak-to-peak swing	Single-ended		1.0		V_{p-p}
t_R/t_F	Rise/Fall time	20 - 80% Limiting Operation		38		ps

Package Outline

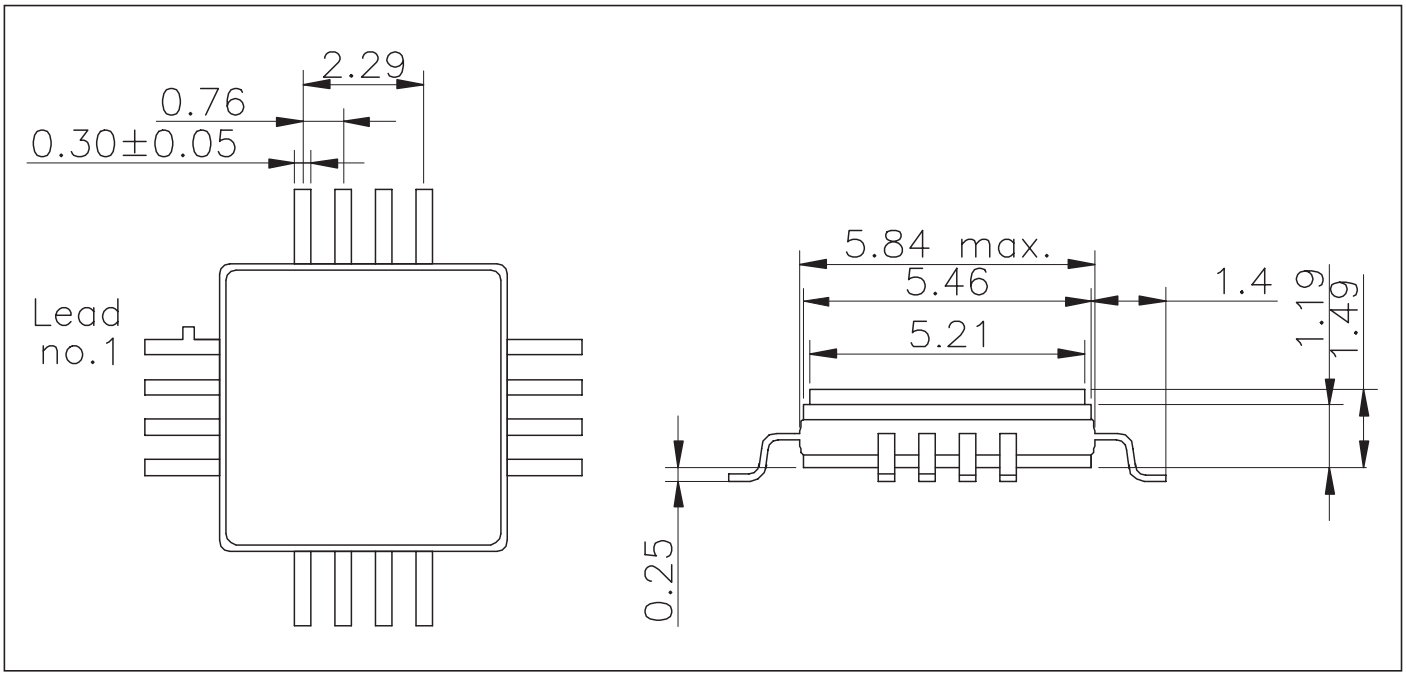


Figure 7. *Package Outline. All dimensions are in mm.*

Device Marking

TBD

Ordering Information

To order, please specify as shown below.

Order Number:	Package Type:	Case Temperature Range:	Options:
GD19908- PG	16 pin Ceramic QFP	0...70°C	

GD19908, Data Sheet Rev.: 05 - Date: 1 December 2000

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