gmFC1A

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IC Product Brief

Frame Buffer Controller / Frame Rate Converter

gmFC1A Chip Features

- Drop-in replacement for the gmFC1
- Maintains frame output image rate, regardless of input rate.
- Drops or replicates input data to maintain output frame rate.
- Enables non-'tearing' output.
- Pads or truncate input lines or fields to a programmed output image size.
- Programmable HSYNC and VSYNC delay
- Requires three external SDRAM devices for frame store.
- 3.3 Volt operation, 5 Volt tolerant I/O.
- 208 pin PQFP package.

Input Format

- Single pixel wide input interface (24 bit RGB or 16 bit YUV).
- Programmable to accept either sequential or interleaved pixels.
- Supports input formats up to 1024 x 768 at 85 Hz (95 MHz pixel clock).
 - (dependent on output format maximum total I/O bandwidth limit of ~ 500 MBytes/s)

Output Format

- Single pixel wide output interface.
- Supports output formats up to 1024 x 768 at 85 Hz.
 - (dependent on input format maximum total I/O bandwidth limit of ~ 500 MBytes/s)

Host Interface

 gmZ1/gmZ2/gmZ3 compatible three or four wire serial host interface access.

Frame Store Interface

 Supports a full 48-bit wide data path using 1M 16-bit or 4M 16-bit SDRAM devices.

Part Description

The gmFC1A offers all of the features of the gmFC1 frame rate converter, plus the ability to delay internal HSYNC and VSYNC signals, allowing the movement of output images across apparent sync boundaries. In addition, the gmFC1A supports the continuous and unrestricted reading of sync measurement values.

Applications

- Accommodate BIOS and various Windows frame rates during Windows boot up
- Manage high input data rates by reducing frame rates
- Manage various input frame rates to support fixed frame rate O/P such as LCD panels
- Games preferring low resolutions
- Special effects utilizing a frame buffer, ex: cropped zooms, freeze frame, 1:1 windowing
- Simplified FRC designs
- System cost reduction in applications ordinarily requiring expensive variable refresh LCD panels

gmFC1A IMPLEMENTATION BLOCK DIAGRAM

