GENESIS MICROCHIP

Product Brief gmZ3A

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High Resolution, High Quality, Low Cost Zoom Engine

The Genesis Microchip gmZ3A IC is a low-cost, highly integrated scaler producing top-quality digital video and computer graphics images. The gmZ3A uses Genesis' patented Advanced Image Magnification algorithm to create images of the highest quality at native resolution or larger magnifications. The gmZ3 is a three-channel device capable of processing RGB or YUV data streams. Additionally, features such as a built-in fully programmable display timing generator, graphics overlay support, multiple input and output data formats and on-chip memory make the gmZ3A a preferred solution for high-end fixed-resolution pixilated display devices such as LCD monitors with **resolutions up to SXGA**.

FEATURES

- **High-quality advanced zoom-only engine**
  - Fully programmable zoom ratios
  - Independent horizontal/vertical zoom
  - Advanced zoom algorithm provides improved performance for better image quality
- **Spatial de-interlacing of video inputs**
  - Corrected spatial positioning of odd and even input lines provides outstanding full-motion video quality
- **Built-in display timing generator**
  - Can be used to drive AMLCD panels
  - Support for DMD engines
  - Fully programmable timing parameters
  - One and two pixels-per-clock panel support
  - Up to 24 bits per pixel
  - Dithering logic to enhance pixel color depth for 18-bit panels
- **YUV input port**
  - 16-bit YUV input video
  - Clock rates up to 45MHz
  - NTSC/PAL square pixels/CCIR601
  - Glueless connection to video capture devices
  - Built-in YUV to RGB color space converter
- **RGB inputs**
  - Maximum 1280 pixels/line input
  - Supports XGA at 85Hz (95 MHz operation)
    - Single pixel (24-bit RGB)
  - Up to SXGA 75Hz (67.5 MHz operation)
    - Dual pixel (48-bit RGB) at half clock
  - Programmable input port timing
- **Auto Configuration** of image position and clock phase
- **Auto Detection** of input formats
- **Output Pixel Modes**
  - One and two pixels per clock panel support
  - Up to SXGA 75Hz (135 MHz operation)
    - Single pixel (24-bit RGB)
    - Dual pixel (48-bit RGB)
  - Compliant with proposed **VESA FPDI-2** std via direct connect to LVDS, PanelLink transceivers
- **Operating Modes**
  - Bypass mode with no filtering (up to SXGA 75Hz)
  - 1:1 scaling with programmable smoothing
  - Non-interlaced zoom
  - De-interlacing zoom
- **Display Synchronization Modes**
  - Frame Sync: input & output frame periods are forced to synchronize
  - Line Sync: display line rate synthesized from the input line rate
  - Free Run: input and output clock rates are not synchronized - ideal for frame-rate conversion
- **Simplicity of design speeds time to market**
  - Single-chip, zoom-only solution
  - No external memory required
  - Programmable horizontal and vertical front and back porches on input data
  - Input active window region decoded
  - Active window framing signal requests pixels two clocks before sampling time
  - Using line request and pixel request signals, pipelined video data I/F may be easily designed
  - Overlay menus supported via dedicated port, control and data lines
  - 4-wire or 3-wire serial host interface for easy connection to Intel or Motorola MCUs
  - Glueless interface to Genesis gmFC1A (FRC) and on-screen-display (OSD) chips

PACKAGE

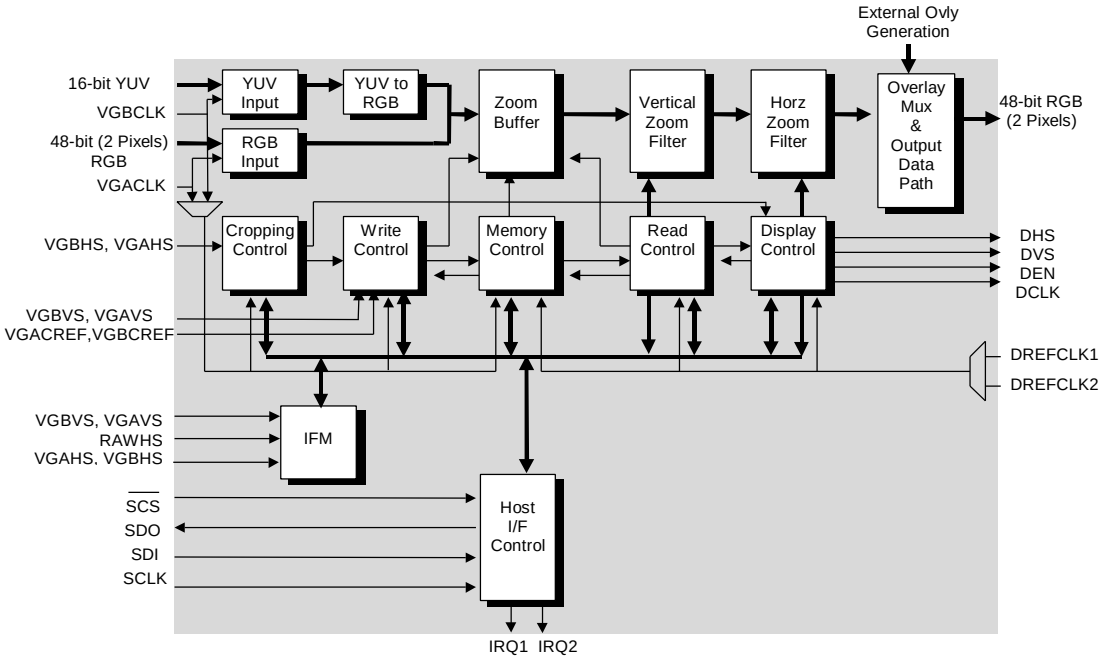
- 208-pin PQFP-EDHS package
- Pin-compatible with gmZ1 and gmZ2A

APPLICATIONS

- Multiple freq. LCD monitors for CRT replacement
- Projection systems (AMLCDs, DMDs)
- Fixed-resolution pixelated display devices
- Home theater and video walls
- Scan doublers/quadruplers/converters

Genesis Microchip
165 Commerce Valley Dr. West, Thornhill, ON Canada L3T 7V8 Tel: (905) 889-5400 Fax: (905) 889-0035
1871 Landings Drive • Mountain View • CA • USA. • 94043 • Tel: (650) 428-4277 • Fax: (650) 428-4288
www.genesis-microchip.com

Functional Block Diagram



System Design Example