Product Brief gmVLX1A-X

C2002-PBR-01H April, 2000

Description

The Genesis Microchip gmVLX1A-X is a low-cost, highly integrated IC for progressive television, DVD and Home Theater applications. This feature-packed chip offers Genesis state-of-the-art Vertical/Temporal (VT) video de-interlacing and Advanced Image Scaling with scale up for full screen video, scale down for video-in-a-window PC/TV applications, and format conversion from 4:3 to 16:9 or vice versa. The gmVLX1A-X also offers gamma correction via programmable VLUTs, vertical and horizontal sharpening / anti-aliasing filters, on-board color space conversion, as well as contrast, brightness, saturation and hue color controls. Vertical Blanking Interval (VBI) data is passed through for Internet TV applications.

The gmVLX1A-X supports two/three/four-wire serial host interface communication, and a seamless interface to low-cost memory (SGRAM or SDRAM) and video decoders. An on-chip display controller allows the gmVLX1A-X output to directly drive DACs or flat panel displays.

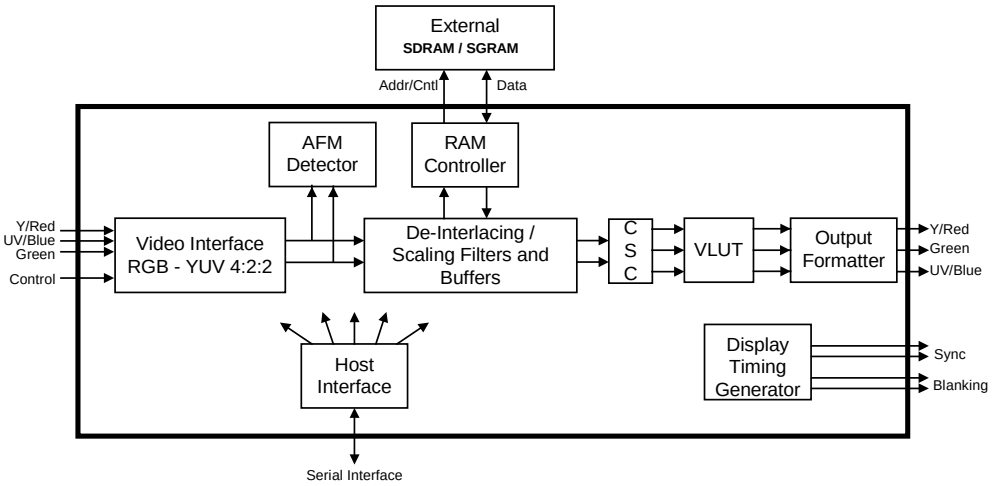
Features

- Genesis proprietary Vertical/Temporal (VT) de-interlacing filter
- Adaptive Film Mode (AFM)
- Advanced Image Scaling engine
- Scale up for full screen video
- Scale down for video-in-a-window PC/TV applications
- Conversion from 4:3 to 16:9 formats or vice versa
- Anamorphic zoom (panoramic mode)
- 4 Vert. and 4 Horz. sharpening filters, contrast, brightness, saturation and hue color controls
- Gamma correction via programmable 10-bit video lookup tables (VLUTs)
- Built-in display controller and color space converter
- Auto-detect NTSC / PAL inputs
- Seamless interface to most industry-standard video decoders: Techwell TW98, Philips, Samsung and ITT. 4:2:2 and 4:4:4 YUV video supported.
- SGRAM or SDRAM on-chip memory controller
- 8/16/24-bit YUV or 24-bit RGB interlaced input
- 12/16/20-bit 4:2:2 YUV, 18/24/30-bit 4:4:4 YUV or 18/24/30-bit RGB output
- VBI data pass-through (for Internet usage)

Applications

- Home Theater, Progressive TV, Progressive DVD
- PC/TV or PC/Theater
- Plasma panels / PDP TV
- Projection Systems
- Scan doublers/quadruplers/converters

gmVLX1A-X Block Diagram



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Functional Description

Input Video Interface

The Video Interface allows seamless connection to most common video decoders, accepting interlaced video in parallel 16-bit 4:2:2 YUV, 4:4:4 YUV, 24-bit RGB and 8-bit ITU-R BT656 formats. The maximum active pixels per line is 768.

Video Interface Timing Signals:

IPCLK: Input Clock - provides the master clock for the Video Interface. This clock is primarily intended to connect to a 2X pixel clock from the decoder.

CREF: Clock Reference - provides a clock-by-clock enable capability for transferring data and control information to the Video Interface.

HREF: Horizontal Reference - indicates the presence of active video during horizontal lines.

HS: Horizontal Sync - indicates the start of a new input line.

VS: Vertical Sync - indicates the start of a new input field.

ODD: Odd Field - indicates odd or even fields for interlaced inputs.

The table below lists some of the Video Decoder devices which interface seamlessly to the gmVLX1A-X:

DEVICE		DESCRIPTION
Techwell	TW98	Square Pixel and ITU-R BT601 NTSC/PAL
Philips	SAA7110	Square Pixel NTSC/PAL/SECAM
Philips	SAA7111	ITU-R BT601 NTSC/PAL
Philips	SAA7112	ITU-R BT601 NTSC/PAL/SECAM
Samsung	KS0122	Square Pixel and ITU-R BT601 NTSC/PAL
Samsung	KS0127	Square Pixel and ITU-R BT601 NTSC/PAL/SECAM
Micronas	VPX3220A	Square Pixel and ITU-R BT601 NTSC/PAL/SECAM
Micronas	VPX3225D	Square Pixel and ITU-R BT601 NTSC/PAL/SECAM

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Output Video Description

The gmVLX1A-X generates the following output timing signals:

DCLK: Display Clock - this output clock may be used to sample output data.
VSYNC: Vertical Sync - indicates the start of a new output frame or composite H/V Sync.
HSYNC: Horizontal Sync - indicates the start of a new output line.
VBLANK: Vertical Blanking - indicates vertical blanking (non-active lines).
HBLANK: Horizontal Blanking - indicates horizontal blanking (non-active pixels).
DV: Data Valid - a "composite active" signal indicating active video only.

Programmable Filters

(Controlled serially via the Host Interface.)

- Arbitrary and independent horizontal and vertical scaling controls
- Input/output cropping, pan, and scan registers
- Access to gamma correction/VLUT
- Selectable image sharpening – four levels horizontal and four levels vertical
- Anamorphic Zoom

Standard Modes (no microcontroller required)

OUTPUT TYPE	OUTPUT RESOLUTON
VESA	640 x 480 [VGA] 800 x 600 [SVGA] 1024 x 768 [XGA]
16:9 (wide screen)	852 x 480 [PDP]
Line Double	(640 or 720) x 480 [NTSC] (768 or 720) x 576 [PAL]
Line Quadruple	(640 or 720) x 960 [NTSC] (768 or 720) x 1152 [PAL]

Gamma Correction/VLUT

The Video Lookup Table (VLUT) provides a loadable lookup function on the input YUV data stream. The VLUT is implemented as static RAM which may be programmed via the Host Interface. The VLUT allows implementation of features such as gamma correction. The VLUT is 3x256x10 bits.

Vertical/Temporal (VT) Filter

The proprietary VT filter design is the heart of the gmVLX1A-X. This block processes data from the incoming field and stored field to produce the output frame. The VT filter performs temporal filtering between fields, and vertical filtering within a field. The VT filter also supports Adaptive Film Mode for optimum output using video converted from film.

Sharpening Filter

Programmable sharpening filters may be applied to the output image to enhance image sharpness.

Color Space Converter (CSC)

The CSC converts 4:2:2 YUV data to 4:4:4 RGB data, and is selectable via the external control pin RGB. When enabled, the CSC converts 4:2:2 YUV (conforming to ITU-R BT601 levels) to full-scale, 24-bit RGB data. The CSC output is clamped to prevent data under /overflow.

Display Controller

The Display Controller provides output control signals to reconstruct the output data. The output timing is determined by default values or by values programmed into the Host Interface.

Control Interface

The Control Interface allows global control over the gmVLX1A-X.

Control Interface signals:

/RESET: Global power-on reset.

RGB: Selects output format: 24-bit RGB or 16-bit 4:2:2 YUV.

OPSIZE: Selects one of eight fixed format output sizes for standard image zooms (e.g., NTSC to XGA).

ITU601: Selects ITU-R BT601 video or square pixel video.

ITU656: Selects ITU-R BT656 video or parallel 16-bit video.

Memory Controller

The gmVLX1A-X requires external memory to store one field of video/graphics data. To simplify design and reduce the solution cost, a built-in memory controller interfaces directly to external DRAM.

Suitable Memory Devices

ORGANIZATION	SUPPORTED MODES	ACCESS TIME	FEATURES
8-Mbit SGRAM 256K x 32-bit			
IBM IBM038329NQ6 Samsung KM4132G271 Hitachi HM5283206FP10	All Modes	10 ns / 12 ns / 16 ns	32-bit data width CAS latency of 3 256-word page size Write-per-bit 8 ms or greater minimum refresh
8-Mbit SGRAM 512K x 32-bit			
Etron EM636327Q-6 Samsung KM4132G512Q-10 Hitachi HM5216326FP10 Silicon Magic SM84L512K32ZL-7	All Modes		
16-Mbit SDRAM 1M x 16-bit			
TI TMS626162 Toshiba TC59S1616AFT NEC µPD45116161G5	Line Doubling, and Quadrupling	10 ns / 12 ns / 16 ns	16-bit data width CAS latency of 3 256-word page size 8 ms or greater minimum refresh
32-Mbit SDRAM 1M x 32-bit			
Samsung KM4132G112Q-7	All Modes		

Host Interface

All gmVLX1A-X functions and image parameters may be programmed through the Host Interface, including input image size, cropping, output image size, output timing, control functions such as input/output pin polarity, and RGB or YUV input/output. It is possible to operate the gmVLX1A-X in common modes using Standard Control Mode, without programming the Host Interface.

Host Interface signals:

/SCS: Serial Chip Select - enables / disables the Host Interface (three and four- wire only).
SCLK: Serial Clock - clocks serial data in /out of the Host Interface (all modes).
SDI: Serial Data Input - Host Interface data write.
SDO: Serial Data Output - Host Interface data read.
(SDO is connected to SDI for a two or three-wire interface configuration)

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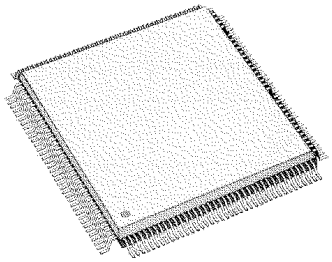
gmVLX1A-X Pinout

Symbol	I/O	Description
		VIDEO INTERFACE
IPCLK	I	Input clock (rising edge triggered)
CREF	I	Clock Reference: 1 = valid data, 0 = invalid data [default]
HREF	I	Horizontal Active Video: 1 = active video, 0 = blanking [default]
HS	I	Horizontal Sync: 1 = sync [default]
VS	I	Vertical Sync: 1 = sync [default]
ODD	I	Current input field type: 1 = odd, 0 = even [default]
Y_RIN(7:0)	I	Current field Y/RED input (unsigned)
UV_BIN(7:0)	I	Current field UV/BLUE input (unsigned)
GIN(7:0)	I/O	Current field Green input (unsigned) or General Purpose Outputs or LSBs of output data in 10-bit mode
AFM_RFF	I	Adaptive Film Mode Repeated First Field: 1 = First field repeated
		DRAM INTERFACE
/RAMRAS	O	External DRAM row address strobe
/RAMCAS	O	External DRAM column address strobe
/RAMWE	O	External DRAM write enable
/RAMOE	O	External DRAM output enable
/RAMCS	O	External DRAM chip select
RAMCLK	O	External DRAM clock
RAMCKE	O	External DRAM clock enable
RAMDSF	O	External DRAM special function enable
RAMADDR(11:0)	O	External DRAM address bus
RAMDQ(31:0)	I/O	External DRAM bi-directional data bus
VDD and GND	N/A	Power and ground connections

Symbol	I/O	Description
		OUTPUT INTERFACE
OPCLK	I	Output clock (rising edge triggered)
DCLK	O	Display clock (rising edge triggered)
HSYNC	O	Horizontal sync output: 0 = sync [default]
HBLANK	O	Horizontal blanking output for output data: 0 = blank [default]
VSYNC	O	Vertical or composite sync output for output frame: 0 = sync [default]
VBLANK	O	Vertical blanking output for output frame: 0 = blank [default]
DV	O	Output data valid: 0 = valid [default]
Y_RED(7:0)	O	8-bit Y/Red output data (unsigned)
UV_BLUE(7:0)	O	8-bit UV/Blue output data (unsigned)
GREEN(7:0)	O	8-bit Green output data (unsigned)
/OE	I	Output data enable: 1 = high Z, 0 = active
/OPFSYNC	I	Output Force Sync: 0 = re-synchronize
DTG_EN	I	Display Timing Generator Enable: 1 = enable, 0 = halt
		CONTROL INTERFACE
ITU656	I	Video interface: 1 = ITU-R BT656 (D-1), 0 = parallel YUV or RGB
ITU601	I	Video format: 1 = ITU-R BT601, 0 = square pixel
/RESET	I	Power-on reset: 0 = reset
RGB	I	Output data format: 1 = RGB, 0 = YUV
OPSIZE(2:0)	I	Zoom modes
/SCS	I	Host Interface chip select: 0 = select
SCLK	I	Host Interface serial clock input
SDI	I	Host Interface serial data input
SDO	O	Host Interface serial data output

gmVLX1A-X Package



160-Pin PQFP