PRELIMINARY DATA SHEET

gmCP1-BA

C0036-DAT-02A

June 2000

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C0036-DAT-02A	gmCP1-BA silicon – BA silicon part initial release	June 2000

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1. OVERVIEW

The gmCP1 IC is designed to insert sync signals into the digital video signal prior to external digital to analog conversion. The chip architecture offers a flexible, multi-mode controller capable of processing 30-bit RGB and YCbCr data. The I^2C compatible host interface allows user configuration of the sync signals. The chip provides a seamless interface to the Genesis Microchip gmVLX1A-X advanced video processor / scaler chip (refer to the gmVLX1A-X Data Sheet DAT-2002 or C2002-DAT-01).

FEATURES

- CGMS Copy Generation Management System (Programmable Video ID)
- Embedded Digital Sync insertion on Y channel
- Y : UV timing control (+/- 3 pixels)
- Programmable sync tip level and blanking level
- Support for 1x/2x horizontal over-sampled pixels
- Input clock 27MHz or 54MHz
- I^2C compatible host interface
- 30-bit YCbCr and RGB formats
- Seamless interface to gmVLX1A-X
- Seamless interface to common YCbCr / RGB DACs
- Single +3.3Volt operation, +5Volt tolerant inputs

INPUT FORMAT

- YCbCr / RGB 525 progressive scan with 1x / 2x horizontal over-sampled pixels (30-bit)

OUTPUT FORMAT

- YCbCr / RGB progressive scan with 1x / 2x horizontal over-sampled pixels (30-bit).

HOST INTERFACE

- I^2C compatible interface

PACKAGE

- 144-pin TQFP package

APPLICATIONS

- Companion chip for gmVLX1A-X for DVD, STB etc.

Supported Input / Output Formats

Input \ Output	YCbCr (4:4:4) - p	RGB (30-bit) – p
YCbCr (4:4:4) - p	**Yes**	**Yes ***
RGB (30-bit) - p	**Yes ***	**Yes**

★ This conversion available only in the gmVLX1A-X device

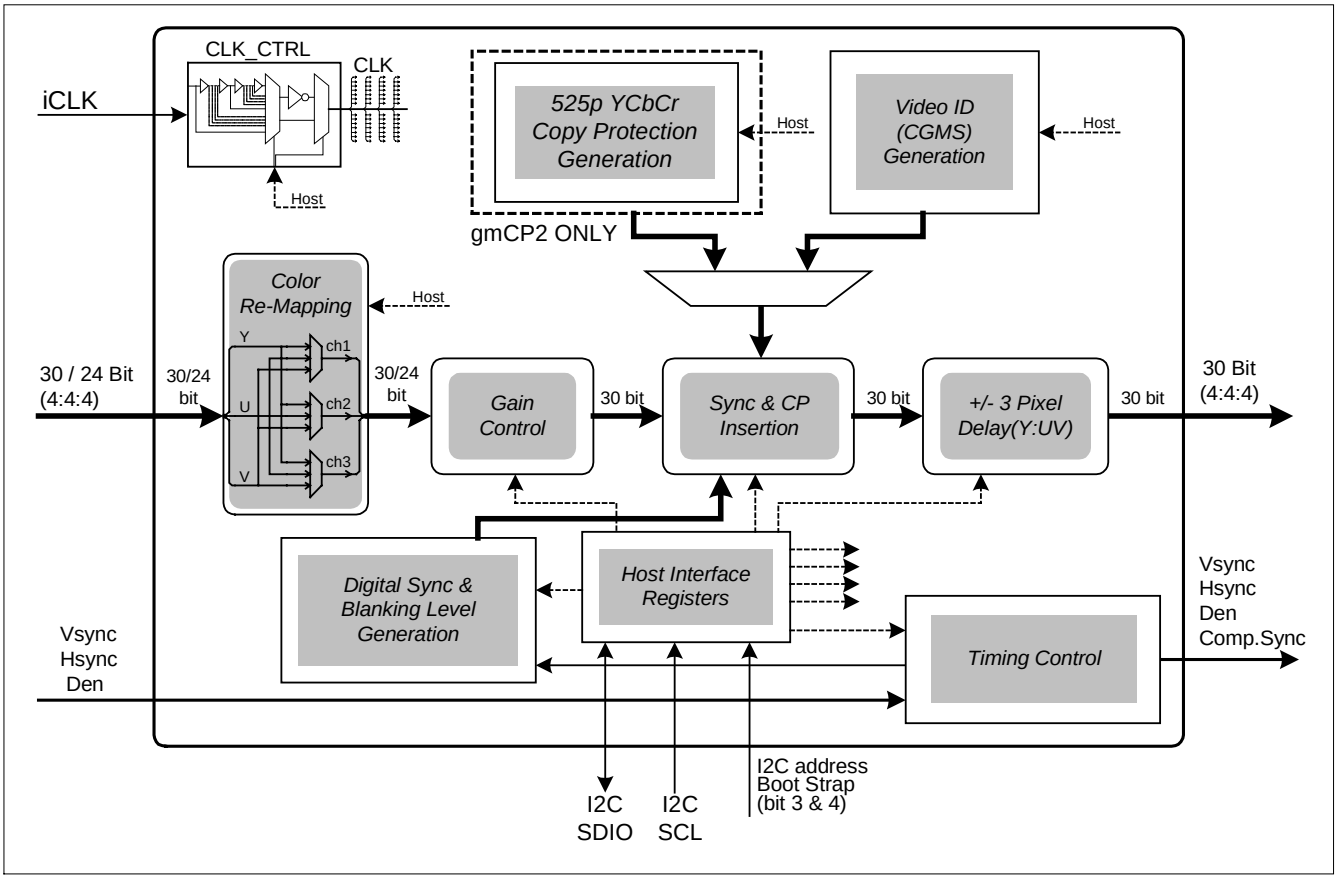


Figure 1: Chip Functional Block Diagram

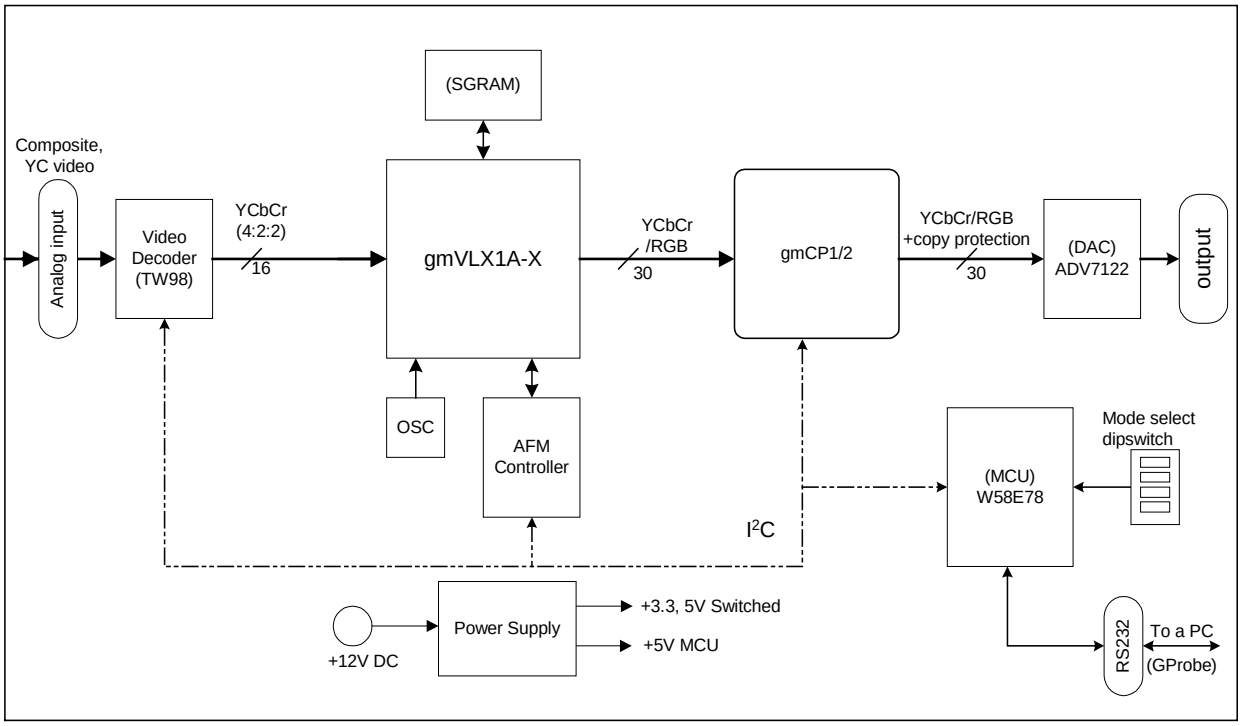


Figure 2: System Design Example

2. PINOUT

Table 1: gmCP1 Pinout

PIN #	PIN NAME	Description	Load (pF)	I/O
1	No connect	No Connection		
2	No connect	No Connection		
3	RESERVED	Must be left open or connected to ground	-	I
4	No connect	No Connection		
5	VCC	3.3V		
6	VCC	3.3V		
7	Y_RED9	Input Y (9)	10	I
8	Y_RED8	Input Y (8)	10	I
9	Y_RED7	Input Y (7)	10	I
10	Y_RED6	Input Y (6)	10	I
11	Y_RED5	Input Y (5)	10	I
12	Y_RED4	Input Y (4)	10	I
13	Y_RED3	Input Y (3)	10	I
14	Y_RED2	Input Y (2)	10	I
15	GND	Gnd		
16	GND	Gnd		
17	Y_RED1	Input Y (1)	10	I
18	Y_RED0	Input Y (0)	10	I
19	U_BLU9	Input Cb (9)	10	I
20	U_BLU8	Input Cb (8)	10	I
21	U_BLU7	Input Cb (7)	10	I
22	U_BLU6	Input Cb (6)	10	I
23	U_BLU5	Input Cb (5)	10	I
24	VCC	3.3V		
25	VCC	3.3V		
26	U_BLU4	Input Cb (4)	10	I
27	U_BLU3	Input Cb (3)	10	I
28	U_BLU2	Input Cb (2)	10	I
29	U_BLU1	Input Cb (1)	10	I
30	U_BLU0	Input Cb (0)	10	I
31	V_GRN9	Input Cr (9)	10	I
32	V_GRN8	Input Cr (8)	10	I
33	V_GRN7	Input Cr (7)	10	I
34	RESERVED	Must be left open or connected to ground	-	I
35	No connect	No Connection		
36	V_GRN6	Input Cr (6)	10	I
37	V_GRN5	Input Cr (5)	10	I
38	V_GRN4	Input Cr (4)	10	I
39	V_GRN3	Input Cr (3)	10	I
40	GND	Gnd		
41	V_GRN2	Input Cr (2)	10	I

PIN #	PIN NAME	Description	Load (pF)	I/O
42	V_GRN1	Input Cr (1)	10	I
43	V_GRN0	Input Cr (0)	10	I
44	SYNC	Output Composite Sync	30	O
45	VCC	3.3V		
46	BLANKn	Output Blank	30	O
47	DUGRN0	Output Port 1 (Y0)	25	O
48	DUGRN1	Output Port 1 (Y1)	25	O
49	DUGRN2	Output Port 1 (Y2)	25	O
50	GND	Gnd		
51	DUGRN3	Output Port 1 (Y3)	25	O
52	VCC	3.3V		
53	VCC	3.3V		
54	HSYNC	Input H Sync	10	I
55	CLK	Input Clock	12	I
56	VSYNC	Input V Sync	10	I
57	GND	Gnd		
58	GND	Gnd		
59	DUGRN4	Output Port 1 (Y4)	25	O
60	DUGRN5	Output Port 1 (Y5)	25	O
61	VCC	3.3V		
62	DUGRN6	Output Port 1 (Y6)	25	O
63	DUGRN7	Output Port 1 (Y7)	25	O
64	DUGRN8	Output Port 1 (Y8)	25	O
65	DUGRN9	Output Port 1 (Y9)	25	O
66	GND	Gnd		
67	DVBLU0	Output Port 2 (Cb0)	25	O
68	DVBLU1	Output Port 2 (Cb1)	25	O
69	DVBLU2	Output Port 2 (Cb2)	25	O
70	DVBLU3	Output Port 2 (Cb3)	25	O
71	VCC	3.3V		
72	DVBLU4	Output Port 2 (Cb4)	25	O
73	DVBLU5	Output Port 2 (Cb5)	25	O
74	No connect	No Connection		
75	VCC	3.3V		
76	No connect	No Connection		
77	No connect	No Connection		
78	DVBLU6	Output Port 2 (Cb6)	25	O
79	DVBLU7	Output Port 2 (Cb7)	25	O
80	DVBLU8	Output Port 2 (Cb8)	25	O
81	DVBLU9	Output Port 2 (Cb9)	25	O
82	DYRED0	Output Port 3 (Cr0)	25	O
83	DYRED1	Output Port 3 (Cr1)	25	O
84	GND	Gnd		
85	GND	Gnd		
86	DYRED2	Output Port 3 (Cr2)	25	O

PIN #	PIN NAME	Description	Load (pF)	I/O
87	DYRED3	Output Port 3 (Cr3)	25	O
88	DYRED4	Output Port 3 (Cr4)	25	O
89	DYRED5	Output Port 3 (Cr5)	25	O
90	DYRED6	Output Port 3 (Cr6)	25	O
91	DYRED7	Output Port 3 (Cr7)	25	O
92	DYRED8	Output Port 3 (Cr8)	25	O
93	VCC	3.3V		
94	VCC	3.3V		
95	DYRED9	Output Port 3 (Cr9)	25	O
96	SCL	Input I2C serial clock	12	I
97	SDIO	Input / Output serial Data for I2C Interface	12/100	IO
98	HSYNC	Output Separate H Sync	30	O
99	VSYNC	Output Separate V Sync	30	O
100	No connect	No Connection		
101	No connect	No Connection		
102	I2CADDA4	I2C Address Selection (Bit 4)	10	I
103	GND	Gnd		
104	GND	Gnd		
105	No connect	No Connection		
106	No connect	No Connection		
107	No connect	No Connection		
108	No connect	No Connection		
109	No connect	No Connection		
110	No connect	No Connection		
111	No connect	No Connection		
112	No connect	No Connection		
113	TEST_2	No Connection	25	O
114	TEST_1	No Connection	25	O
115	VCC	3.3V		
116	I2CADDA3	I2C Address Selection (Bit 3)	10	I
117	No connect	No Connection		
118	No connect	No Connection		
119	No connect	No Connection		
120	No connect	No Connection		
121	No connect	No Connection		
122	HARD_RESETn	Input Hard Reset	10	I
123	VCC	3.3V		
124	No connect	No Connection		
125	No connect	No Connection		
126	DEN	Input Data Enable	10	I
127	GND	Gnd		
128	No connect	No Connection		
129	GND	Gnd		
130	No connect	No Connection		
131	No connect	No Connection		

PIN #	PIN NAME	Description	Load (pF)	I/O
132	No connect	No Connection		
133	No connect	No Connection		
134	VCC	3.3V		
135	No connect	No Connection		
136	No connect	No Connection		
137	No connect	No Connection		
138	No connect	No Connection		
139	GND	Gnd		
140	No connect	No Connection		
141	No connect	No Connection		
142	No connect	No Connection		
143	No connect	No Connection		
144	No connect	No Connection		

3. SETUP INFORMATION

The purpose of this section is to provide information required to successfully power up the ***gmVLX1A-X / gmCP1*** chip set.

3.1 Power Up Sequence

For correct and reliable chip operation, it is important that the following power up sequence be followed exactly by the main system microprocessor:

A- Power on all devices

B- Set the **Reset** signal low (0)

C- Wait for 10us

D- Set the **Reset** signal high (1)

E- Program the gmCP1 host interface register to the required mode

F- Program the gmAFMC to disable the auto-detection function (see Table 2 – first line)

G- Program the gmVLX1A_X host interface register to the required mode (see Table 2)

H- Download the gmVLX1A_X Gamma Table *(optional)*

I- Program the gmAFMC to enable the auto-detection function (see Table 2 – last line)

Table 2: gmVLX1A_X (ITU656 input)

Device Name	Device Address	Register Name	Register Address	Value
gmAFMC	10	VT MODE_SEL	F1	FE
gmVLX1A_X	10	Output Polarity	06	0000
gmVLX1A_X	10	Input Format	08	0007
gmVLX1A_X	10	Scaling Control	0B	0071
gmVLX1A_X	10	Output Control	0C	00E1
gmVLX1A_X	10	In. Horiz. Act. Start MSB	0F	0000
gmVLX1A_X	10	Input Horiz Act. St. LSB	10	0000
gmVLX1A_X	10	In. Horiz. Act. Wid. MSB	11	0002
gmVLX1A_X	10	In. Horiz. Act. Wid. LSB	12	00D0
gmVLX1A_X	10	In. Vert. Act. St. MSB Odd	13	0000
gmVLX1A_X	10	Input Vert. Act. St. Odd	14	000D
gmVLX1A_X	10	In. Vert. Act. St. MSB Ev.	15	0000
gmVLX1A_X	10	Input Vert. Act. St. Even	16	000D
gmVLX1A_X	10	Input Vert. Act. Len. MSB	17	0000
gmVLX1A_X	10	Input Vertical Act. Len.	18	00F0
gmVLX1A_X	10	Input Horiz. Loc. Ev. MSB	19	0003
gmVLX1A_X	10	Input Horiz. Loc. Ev. LSB	1A	005B
gmVLX1A_X	10	Input Vert. Loc. Ev. MSB	1B	0000
gmVLX1A_X	10	Input Vert. Loc. Ev. LSB	1C	0012
gmVLX1A_X	10	Input Horiz. Loc. Ev. MSB	1D	0000
gmVLX1A_X	10	Input Horiz. Loc. Ev. LSB	1E	0001
gmVLX1A_X	10	Input Vert. Loc. Ev. MSB	1F	0000
gmVLX1A_X	10	Input Vertical Loc. Ev.	20	0012
gmVLX1A_X	10	Out. Vert. Fram Len. MSB	38	0002
gmVLX1A_X	10	Out. Vert. Fram Len. LSB	39	000D
gmVLX1A_X	10	Output Vert. Sync Width	3A	0006
gmVLX1A_X	10	Output Vert. Act. St. LSB	3C	001C
gmVLX1A_X	10	Output Vert. Act. Len. MSB	3D	0001
gmVLX1A_X	10	Output Vert. Act. Len. LSB	3E	00E3
gmVLX1A_X	10	Control Reg 1	04	0008
gmAFMC	10	VT MODE_SEL	F1	DF

4. REGISTER PROGRAMMING GUIDE

4.1 Clock Control

The Clock Control function allows selection of the input clock edge (rising or falling) to be used for sampling data and general chip timing. It also allows an advance or delay of the input clock with respect to the input data and timing signals. This allows for fine-tuning of the input setup and hold requirement and output propagation delay.

Table 3 lists all the host registers that control the Clock Control function and their default values (hard reset values).

Table 3: CLOCK CONTROL Host Registers

Register	Function	Default value	Remarks
Register 0x02 bit 3	IO_POLARITY (CLK edge selection)	0	0 = Rising Edge
Register 0x08 bit 4 to 7	DELAY_CTRL (CLK delay control)	0x8	0x0 = -3 ns, …,0x3 = 0 ns, …, 0xF = +13ns

4.2 Polarity Control

The Polarity Control function is used to select the proper / required polarity for all the input and output control/timing signals.

The Output Blanking Signal (Data Valid) can be enabled or disabled (Register 0x01 bit 6). When Output Blanking is enabled, the polarity of the Blanking signal is controlled by register IO_POLARITY (0x02 bit 6). When Output Blanking is disabled, the chip will set the Output Blanking pin to a steady state level (High or Low) based on register IO_POLARITY (0x02 bit 6) If bit 6 = 0, Blanking = Low. If bit 6 = 1, Blanking = High. See Table 4 for more details regarding the polarity control function.

The input signals that may be polarity controlled are:

1- Horizontal Sync.
2- Vertical Sync.
3- Data Valid (Data Enable).

The output signals that may be polarity controlled are:

1- Horizontal Sync.
2- Vertical Sync.
3- Composite Sync.
4- Data Valid (Data Enable / Blanking Signal).

Table 4: POLARITY CONTROL Host Registers

Register	Function	Default value	Remarks
Register 0x02 bit 0	Input H Sync polarity	0	Active Low
Register 0x02 bit 1	Input V Sync polarity	0	Active Low
Register 0x02 bit 2	Invert input Data Valid polarity	1	Active High
Register 0x02 bit 4	Output H Sync polarity	0	Active Low
Register 0x02 bit 5	Output V Sync polarity	0	Active Low
Register 0x02 bit 6	Output Data Valid Polarity / State	0	Active Low (Low for steady state mode)
Register 0x02 bit 7	Output Composite Sync (oSYNC)	0	Normal (not inverted)

4.3 Color Re-mapping

The Color Re-mapping function allows the input colors (Y, Cb, Cr, R, G and B) to be mapped to the output in all the possible combinations. Three bits control the re-mapping are in register 0x07 bits 0, 1 and 2.

Note: the Color Re-mapping function only affects input active data; Digital embedded Sync will always appear at the same output port (output port 1).

Table 5: Valid Color Re-mapping Functions

#	Register Add. 0x07 Bits 0,1 & 2	Output 1 (Y)	Output 2 (Cb)	Output 3 (Cr)
1	000	Y	Cb (U)	Cr (V)
2	001	Y	Cr (V)	Cb (U)
3	010	Cr (V)	Cb (U)	Y
4	011	Cr (V)	Y	Cb (U)
5	100	Cb (U)	Cr (V)	Y
6	101	Cb (U)	Y	Cr (V)
7	110	Y *(inverted)*	Cb (U)	Cr (V)
8	111	Y *(inverted)*	Cb (U) *(inverted)*	Cr (V) *(inverted)*

4.4 Gain Control

The Main function of the Gain Control is to re-map / shift the input active data to allow the gmCP1 to insert sync into the data. The Gain Control function has two main parts, the first is a 6-bit multiplier, and second is a 9-bit adder. Figure 3 show a simple example on how the Gain Control function works. Please note that the illustrated example is not a typical (practical) example; just a simplified case used to explain the Gain Control function.

For practical purposes, use the formula in Figure 4 and the actual min/max values for input and output to obtain the correct values for the adder and multiplier. Load these values into the Gain Control Host Registers (address 0x09 & 0x0A).

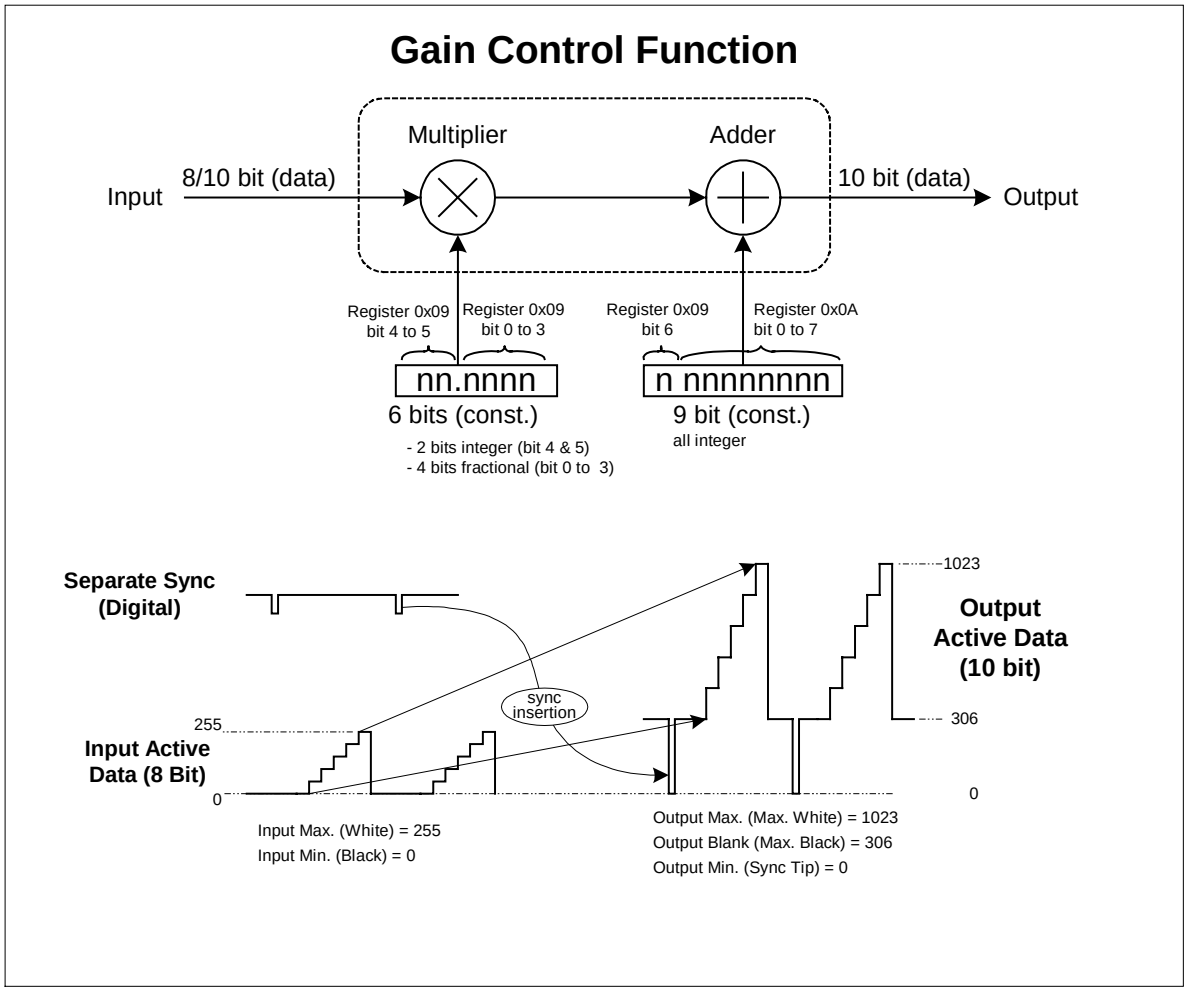


Figure 3: Gain Control Function

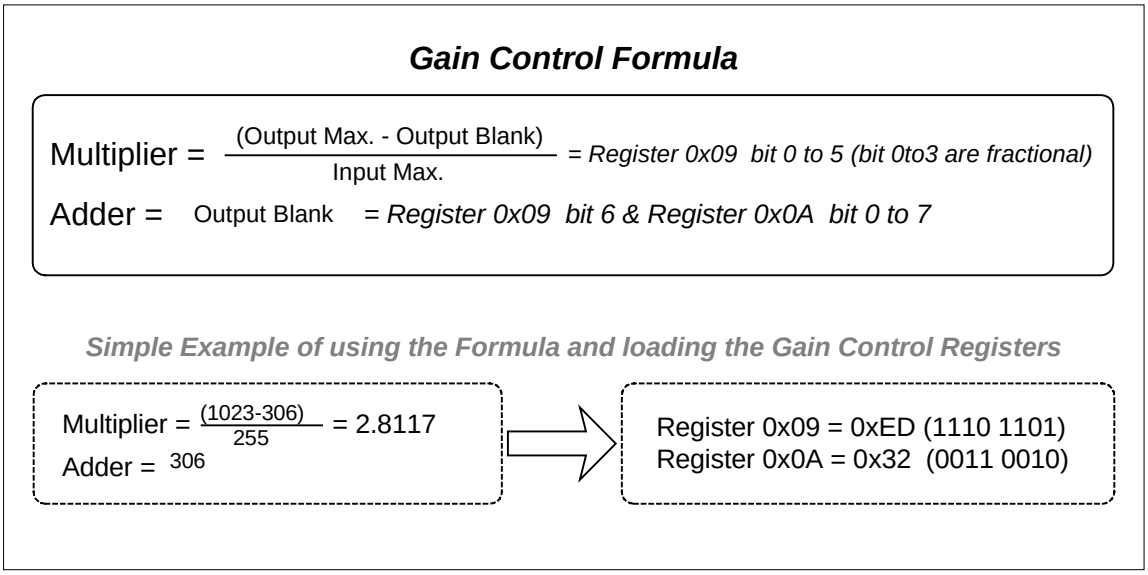


Figure 4: Gain Control Formula

Table 6: Gain Control Registers

Register	Function	Default value	Remarks
Register 0x01 bit 4	Gain Control Enable	1	Gain control enabled
Register 0x07 bit 3	8/10 bit selection	0	8 bit input selected
Register 0x09 bit 0 to 3	Multiplier fractional part	1100	
Register 0x09 bit 4 to 5	Multiplier integer part	10	
Register 0x09 bit 6	Bit 8 of adder integer part	0	
Register 0x09 bit 7	Adder fractional part	1	Adder rounding control (1=ON)
Register 0x0A bit 0 to 7	Bit 0 to 7 of adder integer part	0xE6	

4.5 Digital Sync Insertion

Bit 5 in Register 0x01 is used to select the type of output sync signal as follows:

1. When set to 1: the gmCP1 will operate in Separate Sync Mode in which it will output separate digital H and V Syncs and a digital Composite Sync. In this mode the active video data can swing from 0 to 1023. When the chip operates in this mode, the system will require a DAC (digital to analog converter) that has a separate digital input sync (usually composite sync) to insert the sync into the Y/G channel.

** Please note that when operating in this mode, the sync slew rate control will not be functional, and the rise and fall time of the sync will depend completely on the DAC.

2. When set to 0: the gmCP1 will operate in Embedded Sync Mode in which it will insert Sync into the Y/G channel. In this mode the active video data will swing between the Y Blanking level to 1023 while the range from 0 to Blanking will be used for Sync insertion only (shifting the data from 0 to Blanking level is done by the Gain Control Block).

   ** Please note that operating in this mode will require the correct programming of the Gain Control, Blanking Level and CTRL_REG.

4.6 Setting the Sync Tip and Blanking Level

The gmCP1 allows the user to control the sync tip level and the blanking level for Y and Cb/Cr *(this is only valid for embedded digital sync on Y mode).*

Register 0x03 sets the sync tip level to a value between 0 and 255, with a default value of 0.

Registers 0x04 and 0x06 set the blanking level for the Y signal to a value between 0 and 1023, with a default value of 214.

Registers 0x05 and 0x06 set the blanking level for Cb/Cr signals to a value between 0 and 1023 with the default value of 575.

Notes:

- *The default values are loaded internally after a Hard Reset.*
- *All gmCP1 registers are 8-bit, so register 0x04 and 0x05 contains only bit 0 to bit 7 (LSB) and register 0x06 bits 0, 1, 2 and 3 contains bit 8 and bit 9 (MSB) of the 10 bits value.*

See Figure 5 below for more details.

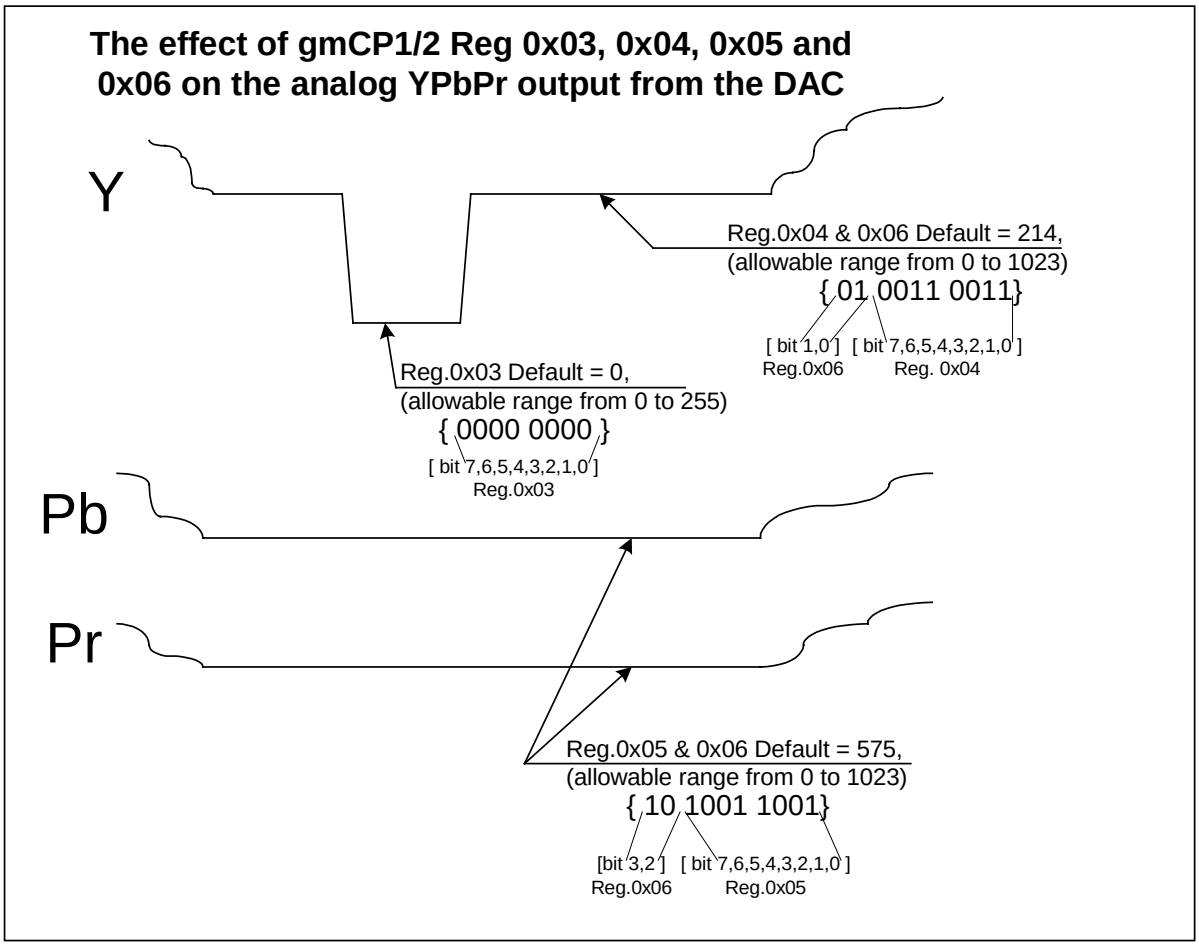


Figure 5: Sync Tip and Blanking Control

4.7 Slew Rate Control

The gmCP1 allows the control over the rise / fall time of the embedded sync and CGMS pulses. See Table 7 for listing of all valid Slew Rate Control values and see Figure 6 for detailed function explanation.

Table 7: Slew Rate Control Programming Values

Register	Function	Default value	Remarks
Register 0x07 bits 4 to 6	Sync Slew Rate Control 000 (binary) = slew rate control is off (Fast) 001 (binary) = 1 step slow slew rate 010 (binary) = 2 step slow slew rate 011 (binary) = 3 step slow slew rate 100 (binary) = 4 step slow slew rate 101 (binary) = 5 step slow slew rate 110 (binary) = 6 step slow slew rate **111** (binary) = *** * * * Invalid Setting * * * ***	0x2	Each step in the slew rate control is 1 clock cycle
Register 0x14 bits 4 to 6	CGMS Slew Rate Control 000 (binary) = slew rate control is off (Fast) 001 (binary) = 1 step slow slew rate 010 (binary) = 2 step slow slew rate 011 (binary) = 3 step slow slew rate 100 (binary) = 4 step slow slew rate 101 (binary) = 5 step slow slew rate 110 (binary) = 6 step slow slew rate **111** (binary) = *** * * * Invalid Setting * * * ***	0x2	Each step in the slew rate control is 1 clock cycle

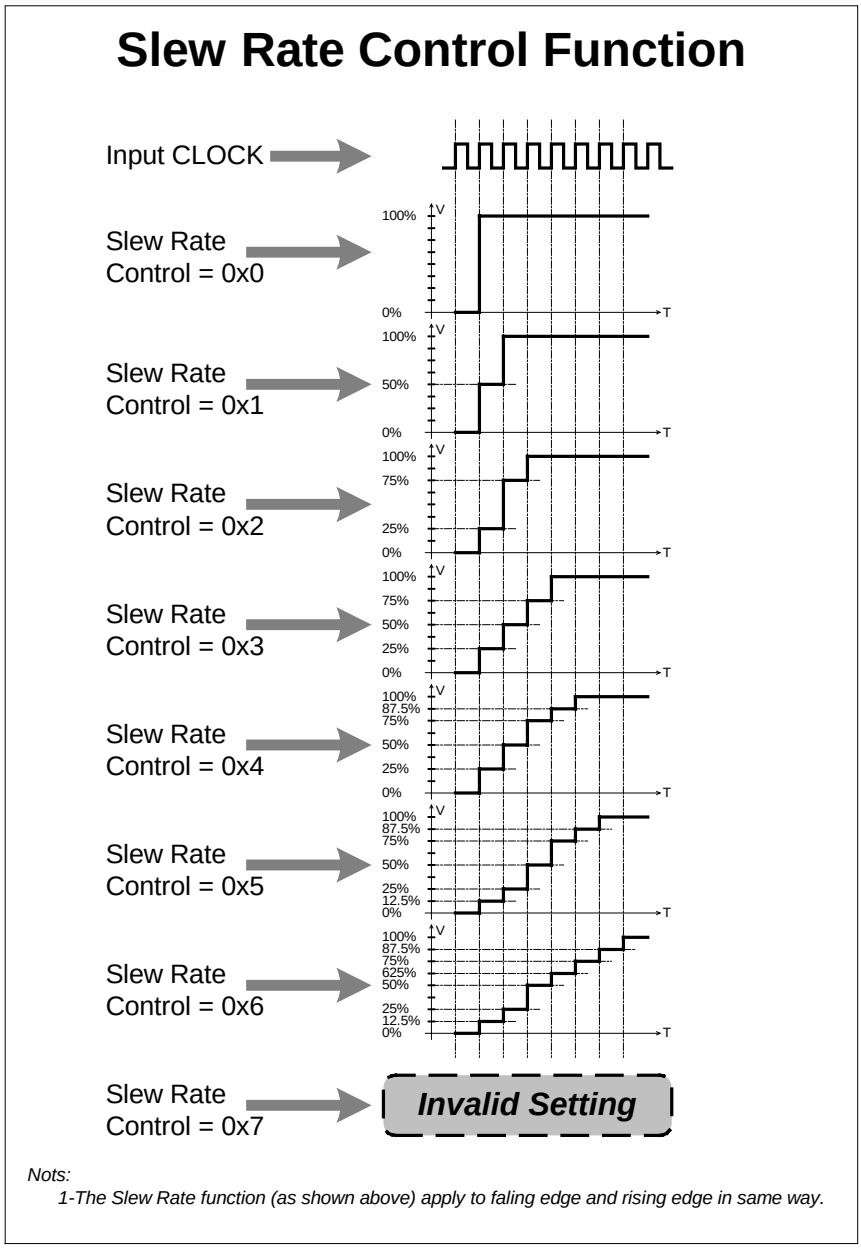


Figure 6: Slew Rate Control Function

Note:

1- *Sync Slew Rate only functions for the Embedded Digital Sync on Y, i.e. separate sync are not supported.*

2- *Although Slew Rate control for CGMS and Sync are controlled by 3 bits, valid values range from 0 to 6, i.e. the **Value 7 is invalid** for CGMS and SYNC.*

3- *The Slew Rate Control affects only the Y channel, i.e. it has no affect on the Cb and Cr channels.*

4.8 CGMS (Video ID)

The gmCP1 supports placing the CGMS (Copy Generation Management System) into the output data stream (for the Y channel only). Utilizing a very flexible CGMS generator, the chip can support different standards.

Please refer to ***EIA-805*** for the American Standard, and ***EIAJ CPR-1204*** for the Japanese Standard.

When setting the chip to generate the ***Japanese Standard*** refer Figure 7 to and Table 8.

When setting the chip to generate the ***American Standard*** refer to Figure 8 and Table 9.

Figure 7: CGMS Wave form (Japanese Std.)

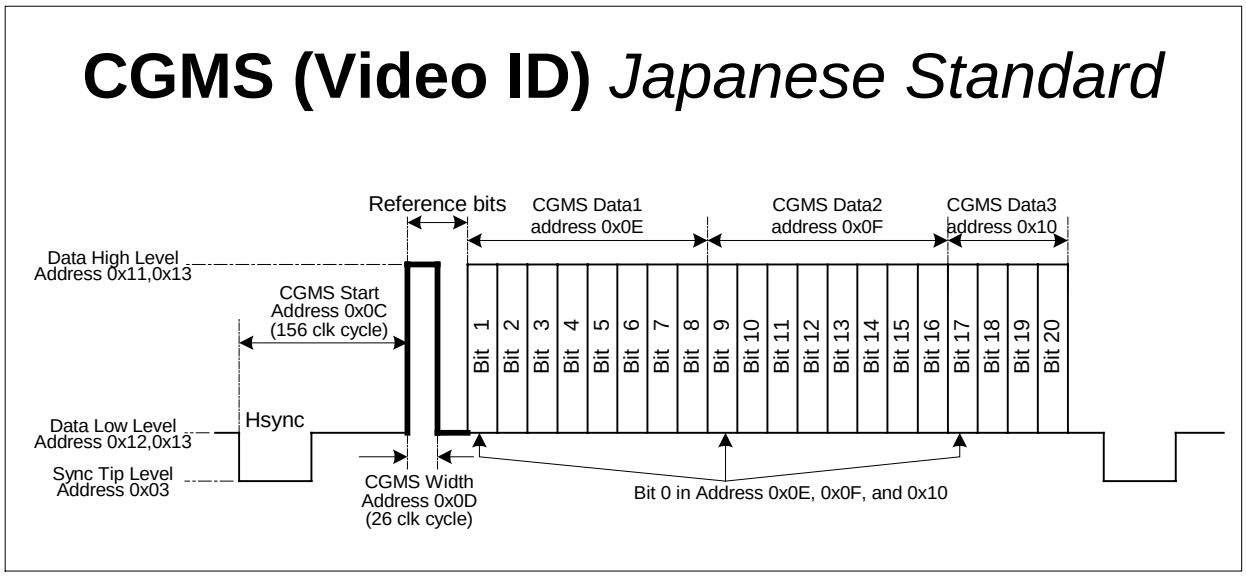


Table 8: CGMS Registers setting (for Japanese Std.)

Register	Bits	Function	Program. value Binary (Hex)	Remarks
Register 0x0B	bit 0 to 7	CGMS Control	(0x69)	
	bit 0 to 5	CGMS line selection	10 1001	Select line 41
	bit 6	CGMS Enable	1	Enable CGMS
	bit 7	Reference bits selection	0	Select 2 reference bits
Register 0x0C	bit 0 to 7	CGMS Start	(0x9C)	From the leading edge of Sync to the leading edge of first reference bit (156 clk cycle).
Register 0x0D	bit 0 to 7	CGMS Width	(0x1A)	Width of the CGMS pulse (26 clk cycle).
Register 0x0E	bit 0 to 7	CGMS Data 1	(0xnn)	Bit 1 to bit 8
	bit 0	Bit 1 of CGMS data Package		
	bit 1	Bit 2 of CGMS data Package		
	bit 2	Bit 3 of CGMS data Package		
	bit 3	Bit 4 of CGMS data Package		
	bit 4	Bit 5 of CGMS data Package		
	bit 5	Bit 6 of CGMS data Package		
	bit 6	Bit 7 of CGMS data Package		
	bit 7	Bit 8 of CGMS data Package		
Register 0x0F	bit 0 to 7	CGMS Data 2	(0xnn)	Bit 9 to 16
	bit 0	Bit 9 of CGMS data Package		
	bit 1	Bit 10 of CGMS data Package		
	bit 2	Bit 11 of CGMS data Package		
	bit 3	Bit 12 of CGMS data Package		
	bit 4	Bit 13 of CGMS data Package		
	bit 5	Bit 14 of CGMS data Package		
	bit 6	Bit 15 of CGMS data Package		
	bit 7	Bit 16 of CGMS data Package		
Register 0x10	bit 0 to 3	CGMS Data 3	(0x0n)	Bit 17 to 20
	bit 0	Bit 17 of CGMS data Package		
	bit 1	Bit 18 of CGMS data Package		
	bit 2	Bit 19 of CGMS data Package		
	bit 3	Bit 20 of CGMS data Package		
	bit 4	Not used		Must be set to 0
	bit 5	Not used		Must be set to 0
	bit 6	Not used		Must be set to 0
	bit 7	Not used		Must be set to 0
Register 0x11	bit 0 to 7	CGMS Hi Level – LSB	(0xnn)	Bit 0 to 7 of 10 bit data Hi level (the data Hi should be set to 70% of the peak white)
Register 0x12	bit 0 to 7	CGMS Low Level – LSB	(0xnn)	Bit 0 to 7 of 10 bit data Low level (the data Low should be set to the Y Blanking Level)
Register 0x13	bit 0 to 7	CGMS Miscellaneous	(0x2n)	
	bit 0 to 1	CGMS Hi Level – MSB	nn	
	bit 2 to 3	CGMS Low Level – MSB	nn	
	bit 4	CGMS Reference bit 1	0	
	bit 5	CGMS Reference bit 0	1	
	bit 6	Not used	0	Must be set to 0
	bit 7	Not used	0	Must be set to 0

Figure 8: CGMS Wave Form (American Std.)

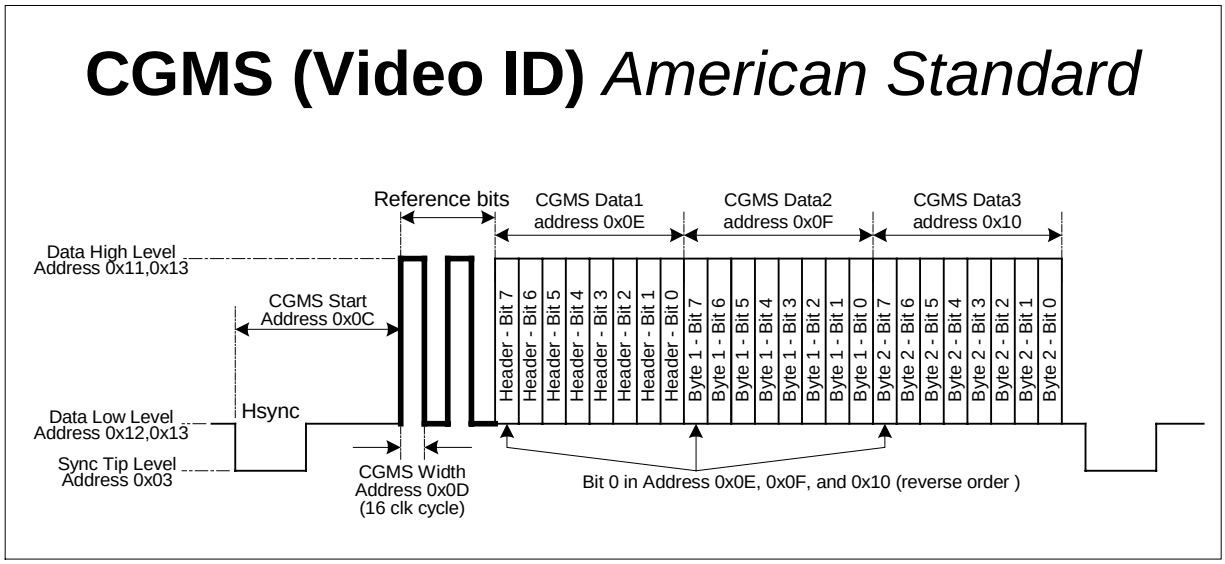


Table 9: CGMS Registers setting (for American Std.)

Register	Bits	Function	Program. value Binary (Hex)	Remarks
Register 0x0B	bit 0 to 7	CGMS Control	(0xE9)	
	bit 0 to 5	CGMS line selection	10 1001	Select line 41
	bit 6	CGMS Enable	1	Enable CGMS
	bit 7	Reference bits selection	1	Select 4 reference bits
Register 0x0C	bit 0 to 7	CGMS Start	(0xnn)	From the leading edge of Sync to the leading edge of first reference bit (refer to EIA805 for the start value).
Register 0x0D	bit 0 to 7	CGMS Width	(0x10)	Width of the CGMS pulse (16 clk cycle).
Register 0x0E	bit 0 to 7	CGMS Data 1	(0xnn)	CGMS Header Byte (*in reverse order*)
	bit 0	Bit 7 of CGMS data Header		
	bit 1	Bit 6 of CGMS data Header		
	bit 2	Bit 5 of CGMS data Header		
	bit 3	Bit 4 of CGMS data Header		
	bit 4	Bit 3 of CGMS data Header		
	bit 5	Bit 2 of CGMS data Header		
	bit 6	Bit 1 of CGMS data Header		
	bit 7	Bit 0 of CGMS data Header		
Register 0x0F	bit 0 to 7	CGMS Data 2	(0xnn)	CGMS Data Byte 1 (*in reverse order*)
	bit 0	Bit 7 of CGMS data Byte 1		
	bit 1	Bit 6 of CGMS data Byte 1		
	bit 2	Bit 5 of CGMS data Byte 1		
	bit 3	Bit 4 of CGMS data Byte 1		
	bit 4	Bit 3 of CGMS data Byte 1		
	bit 5	Bit 2 of CGMS data Byte 1		
	bit 6	Bit 1 of CGMS data Byte 1		
	bit 7	Bit 0 of CGMS data Byte 1		
Register 0x10	bit 0 to 3	CGMS Data 3	(0xnn)	CGMS Data Byte 2 (*in reverse order*)
	bit 0	Bit 7 of CGMS data Byte 2		
	bit 1	Bit 6 of CGMS data Byte 2		
	bit 2	Bit 5 of CGMS data Byte 2		
	bit 3	Bit 4 of CGMS data Byte 2		
	bit 4	Bit 3 of CGMS data Byte 2		
	bit 5	Bit 2 of CGMS data Byte 2		
	bit 6	Bit 1 of CGMS data Byte 2		
	bit 7	Bit 0 of CGMS data Byte 2		
Register 0x11	bit 0 to 7	CGMS Hi Level – LSB	(0xnn)	Bit 0 to 7 of 10 bit data Hi level (the data Hi should be set to 85 -100% of the peak white)
Register 0x12	bit 0 to 7	CGMS Low Level – LSB	(0xnn)	Bit 0 to 7 of 10 bit data Low level (the data Low should be set to the Y Blanking Level)
Register 0x13	bit 0 to 7	CGMS Miscellaneous	(0xAn)	
	bit 0 to 1	CGMS Hi Level – MSB	nn	
	bit 2 to 3	CGMS Low Level – MSB	nn	
	bit 4	CGMS Reference bit 3	0	
	bit 5	CGMS Reference bit 2	1	
	bit 6	CGMS Reference bit 1	0	
	bit 7	CGMS Reference bit 0	1	

4.9 +/- 3 Pixel Delay

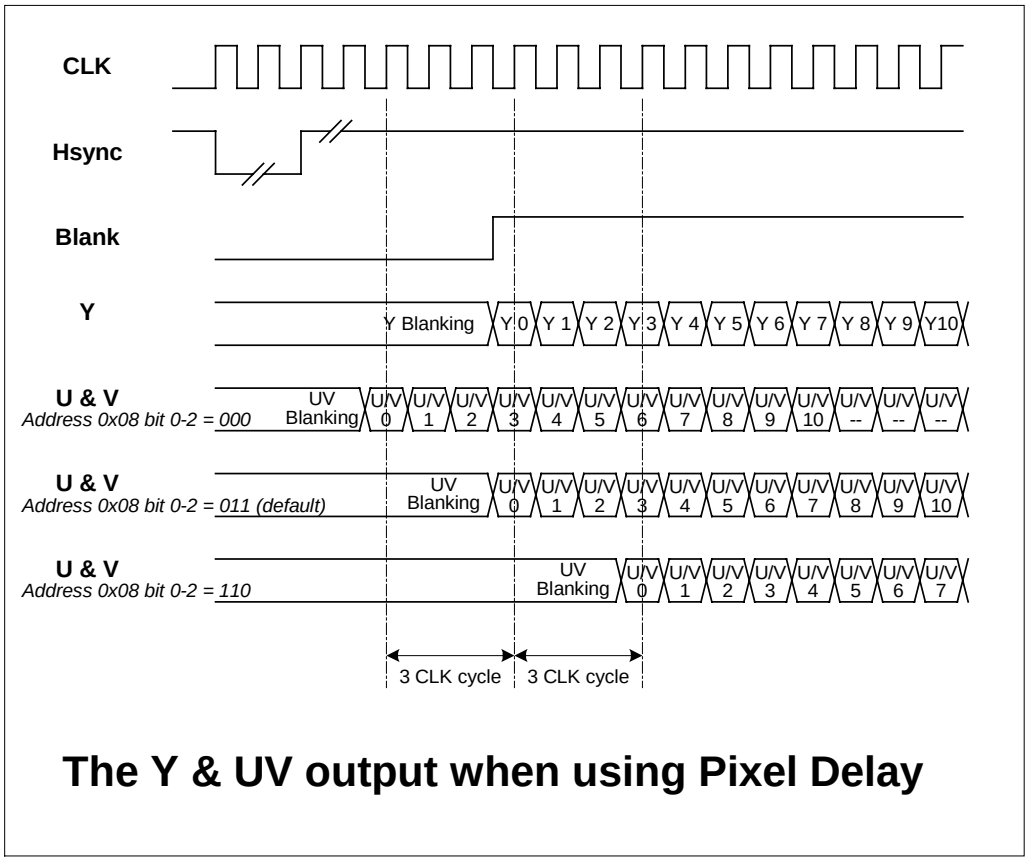
The Pixel Delay function allows for the control of Y:UV timing. By programming the Pixel Delay register, the U & V channels can be delayed or advanced with respect to the Y channel (+/- 3 clock cycles). When the relation between Y : UV changes, the relation between the Y channel and the separate control signals (H, V, Osync and Blank) remains unchanged. i.e., the Pixel Delay function only affects the U & V channel, without having any affect on the Y or separate control signals.

The Pixel Delay Register uses three bits, allowing seven settings: three delay steps, three advance steps, one neutral step. The last setting (binary 111) is invalid. For more details, see Figure 9.

Note:

The Pixel Delay function is based on clock cycles, not image pixels; when operating at 27 MHz, the function can swing from –3 to +3 image pixels, but when operating at 54 MHz, the function can swing from –1.5 to +1.5 image pixels. At 54 MHz, each image pixel requires 2 clock cycles.

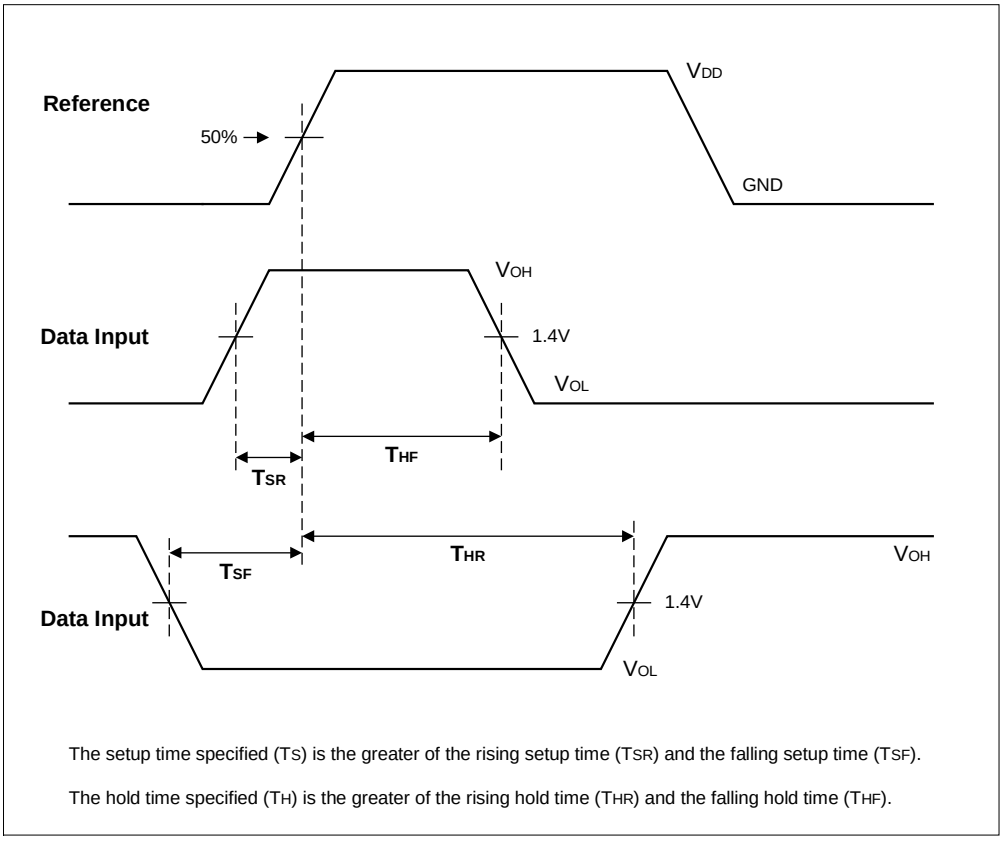
Figure 9: Pixel Delay Function



5. PRELIMINARY TIMING

All specifications were derived from simulations only, under the following conditions:

	Voltage	Ambient Temp.	Process
Min.	3.6 VDC	-40 C	Min.
Typ.	3.3 VDC	25 C	Nominal
Max.	3.0 VDC	85 C	Max.



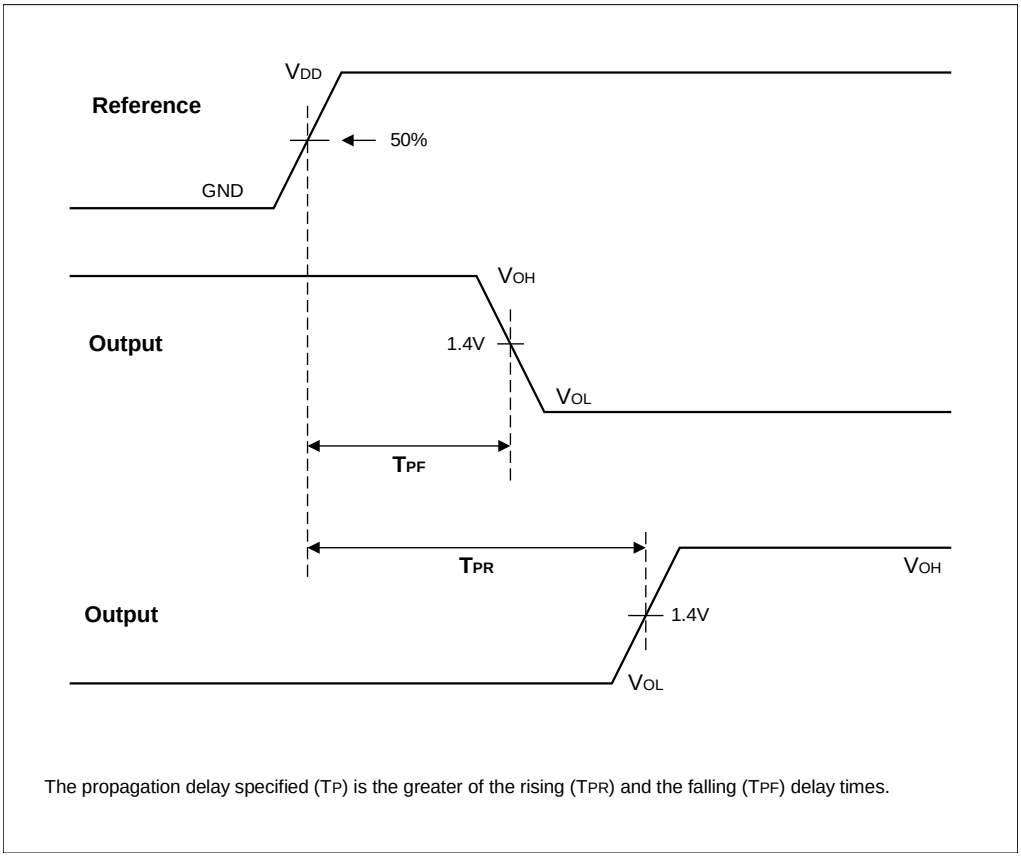
The setup time specified (T_S) is the greater of the rising setup time (T_{SR}) and the falling setup time (T_{SF}).

The hold time specified (T_H) is the greater of the rising hold time (T_{HR}) and the falling hold time (T_{HF}).

Figure 10: Setup and Hold Parameters

Table 10: Setup and Hold Times (ns)

		Setup T_S			Hold T_H					Setup T_S	Hold T_H
Signal	**Clock Reference**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**		**Clock Reference**	**Min.**	**Min.**
DEN	ICLK								SCLK		
HSYNC	ICLK								SCLK		
VSNC	ICLK								SCLK		
U_BLU	ICLK								SCLK		
V_GRN	ICLK								SCLK		
Y_RED	ICLK								SCLK		
SDIO	ICLK								SCLK		
HARD_RESETn	ICLK								SCLK		
SCL	ICLK								SCLK		



The propagation delay specified (TP) is the greater of the rising (TPR) and the falling (TPF) delay times.

Figure 11: Propagation Delay Parameters

Table 11: Output Propagation Delays (ns)

Signal	Clock Reference	T_P Min.	T_P Typ.	T_P Max.		Clock Reference	T_P Min.	T_P Typ.	T_P Max.
SYNC	ICLK					SCLK			
HSYNC_OP	ICLK					SCLK			
VSYNC_OP	ICLK					SCLK			
BLANKn	ICLK					SCLK			
DVBLU	ICLK					SCLK			
DUGRN	ICLK					SCLK			
DYRED	ICLK					SCLK			
SDIO	ICLK					SCLK	1SCLK	1SCLK	1SCLK

6. HOST INTERFACE

6.1 Two Wire Protocol

The gmCP1 provides an I^2C compatible host interface register to support device configuration. The register file is written to and read from using an I^2C compatible protocol. All read and write register bits take effect immediately after being written. All registers contain 8-bits.

The bus master, typically a controller, is responsible for generating the SCL clock input. The rising edge of SCL samples an input bit on the SDA data line, and the falling edge of SCL initiates the launch of an output bit from the SDA data line. All transmissions are most significant bit (MSB) first. The gmCP1 device address is 6Dh.

All communications with the gmCP1 Host Interface must be initiated by a START condition. This condition consists of a high to low transition on the SDA data line while SCL is high. The master then transmits the seven bit device address followed by a R/W bit; a low indicating a write, or a high indicating a read. The value transmitted during the R/W cycle directly declares the direction of transfer for the next successive bytes.

Upon receipt of the 7-bit device address and 1-bit read/write, an acknowledge is transmitted by the gmCP1 Host Interface. The bus master may then transmit the eight bit operation code. The gmCP1 Host Interface again acknowledges this byte. For every byte transmitted by the bus master, the Host Interface sends an acknowledge, provided communication was successful. When the bus master is receiving, it is the bus master that must provide the acknowledge bit. This acknowledge indicates to the gmCP1 Host Interface that receipt of a byte was successful. The bus master receiver must note the end of a data burst transmission by NOT acknowledging the last byte read. During the acknowledge bit cycle, a STOP condition must instead be transmitted by the bus master. This STOP condition consists of a low to high transition on the SDA data line while SCL is high.

The first byte (after the device address) of each Two-Wire protocol transfer is an instruction byte indicating the type of operation to be performed. Table 12 provides a listing of the available operation codes. The selection of a SPARE operation code results in a no operation. The reserved operation codes should not be used, as they represent diagnostic operations.

Hex Value	Operation Mode
0x00 / 0x50 / 0x60 / 0x70 / 0xD0 / 0xE0 / 0xF0	Spare
0x20 / 0x30 / 0x40 / 0x80 / 0x90 / 0xB0 / 0xC0	Reserved
0x10	Single Byte Write
0xA0	Single Byte Read

Table 12: gmCP1 Two Wire Protocol Operation Modes

Operation	Code	Description
Single Write	0x10	Allows the user to write a single byte to a specified address location.

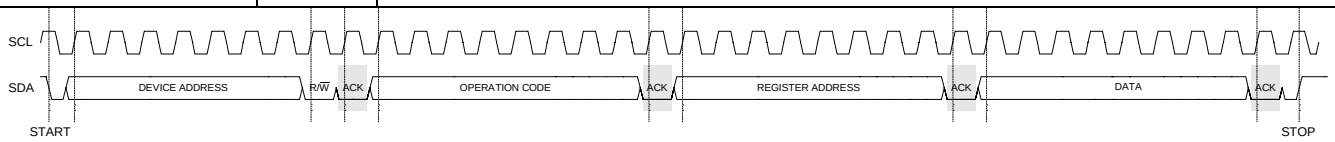


Figure 12: Two Wire Single Byte Write Operation

Operation	Code	Description
Single Read	0xA0	Allows the user to read a single byte from a specified address location. Note: The last byte must not be followed by an acknowledge. A low to high transition must occur on the SDA data line during the acknowledge cycle.

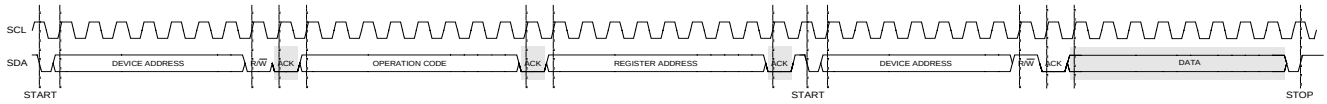


Figure 13: Two Wire Single Byte Read Operation

6.2 Host Interface Register Map

The gmCP1 provides an I^2C compatible host interface register to support device configuration. The register file is written to and read from using an I^2C compatible protocol. All read and write register bits take effect immediately after being written. All registers contain 8-bits.

Table 13: gmCP1 Host Interface Register

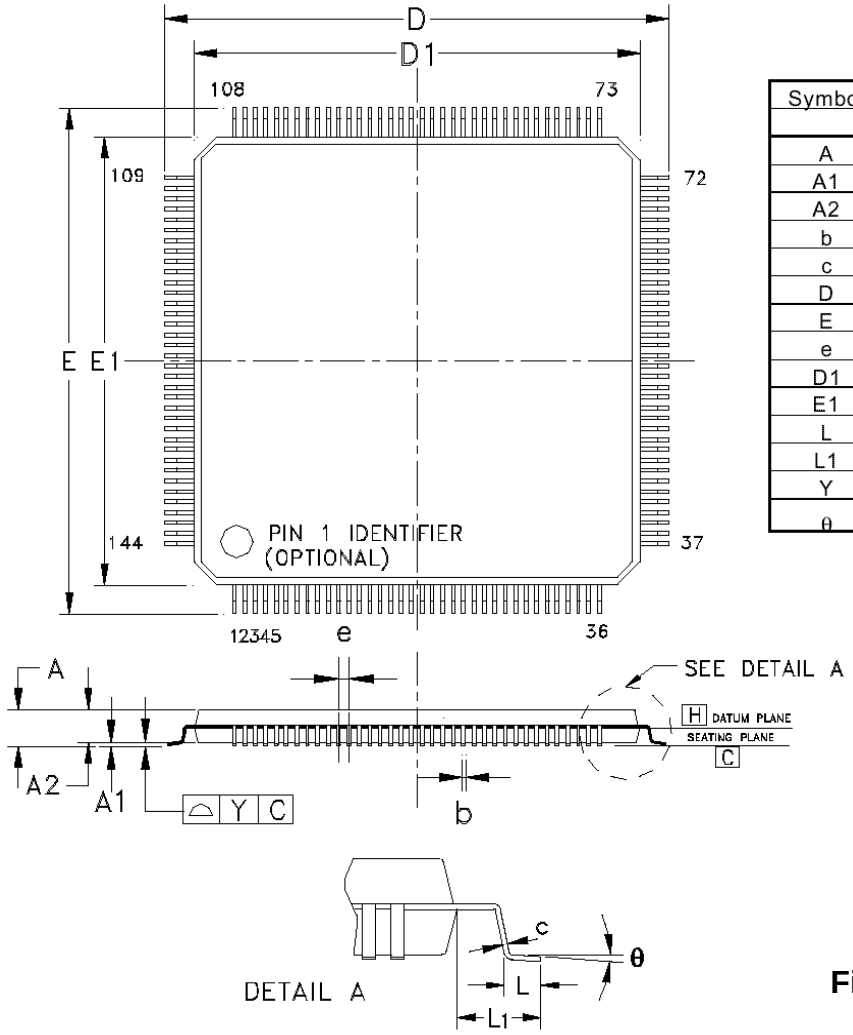
Address		Description	Default Value	Function if = 0	Function if = 1	Remarks
0	0x00	**CHIP_ID (Read Only)**	0xnB			
	Bit 0 to 3	BA silicon version	B			
	Bit 4 to 7	1=gmCP1, 2=gmCP2	1 / 2			
1	0x01	**CTRL_REG**	0x10			
	Bit 0 to 3	RESERVED	0			
	Bit 4	Gain Control Enable	1	Disabled	Enabled	
	Bit 5	Sync on Y/G	0	Embedded Sync	Separate Sync	Embedded digital Sync
	Bit 6	Output Blanking (DV)	0	Disabled	Enabled	When disabled the output = DV STAT
	Bit 7	54MHz input	0	27MHz	54MHz	
2	0x02	**IO_POLARITY**	0x40			
	Bit 0	Input H polarity	0	Active low	Active Hi	
	Bit 1	Input V polarity	0	Active low	Active Hi	
	Bit 2	Invert input DV polarity	1	Active low	Active Hi	
	Bit 3	iCLK (sampling edge selection)	0	Rising edge	Falling edge	
	Bit 4	Output H polarity	0	Active low	Active Hi	
	Bit 5	Output V polarity	0	Active low	Active Hi	
	Bit 6	Output DV State	0	Active Low (1)	Active Hi (1)	
	Bit 7	Output Composite Sync (oSYNC)	0	Normal	Inverted	
3	0x03	**SYNC_TIP**	0x00			For embedded digital Sync
	Bit 0 to 7	8 bit Sync tip level				(0 to 255)
4	0x04	**Y_CLAMP**	0xD6			
	Bit 0 to 7	10 bit Y Blanking level				(0 to 1023)
5	0x05	**UV_CLAMP**	0x3F			
	Bit 0 to 7	10 bit U & V Blanking level				(0 to 1023)
6	0x06	**CLAMP_MSB**	0x08			
	Bit 0 to 1	Y Clamping Level Bit 8 & 9				
	Bit 2 to 3	Cb Cr Clamping Level Bit 8 & 9				
	Bit 4 to 7	RESERVED				
7	0x07	**MISCELLANEOUS**	0x20			
	Bit 0 to 2	Output Color Re-mapping				
	Bit 3	10/8 bit input selection	0	8 bit (bit 2 to 9)	10 bit	Must set to 8 bit when using the Gain_Ctrl function
	Bit 4 to 6	Sync Slew Rate Control				000= no slew, 001=1 clk, …,110=6 clk
	Bit 7	RESERVED				
8	0x08	**DELAY_CTRL**	0x23			
	Bit 0 to 2	+/- 3 clk (valid from 0 to 6)				000=-3CLK, ...,011=0 CLK, …,110=+3CLK
	Bit 3	RESERVED				
	Bit 4 to 7	CLK delay				0000 = -8 ns, …,1000 = 0 ns, …, 1111 = +7ns
9	0x09	**Gain_CTRL1**	0xAC			
	Bit 0 to 3	Multiplier fractional part				Multiplier = 2.8125
	Bit 4 to 5	Multiplier main part				
	Bit 6	Bit 8 of adder integer part	0			
	Bit 7	Adder fractional part	1	Rounding Off	Rounding On	Should be always set to rounding on (on = 1)
10	0x0A	**Gain_CTRL2**	0xE6			
	Bit 0 to 7	Bit 0 to 7 of adder integer part				Adder = 305.5
11	0x0B	**CGMS_CTRL**	0x23			
	Bit 0 to 5	CGMS line selection	29h			
	Bit 6	CGMS enable	1	Disabled	Enabled	
	Bit 7	Reference bits selection	0	2 bit Ref.	4 bit Ref.	
12	0x0C	**CGMS_STRT**	0x9C			
	Bit 0 to 7	CGMS code start location	9Ch			
13	0x0D	**CGMS_WID**	0x1A			

	Bit 0 to 7	CGMS pulse width	0x1A			
14	0x0E	**CGMS_D1**	0x00			
	Bit 0 to 7	CGMS code bit 0 to 7	0xnn			
15	0x0F	**CGMS_D2**	0x00			
	Bit 0 to 7	CGMS code bit 8 to 15	0xnn			
16	0x10	**CGMS_D3**	0x00			
	Bit 0 to 7	CGMS code bit 16 to 23	0xnn			
17	0x11	**CGMS_HI**	0x84			
	Bit 0 to 7	CGMS level high	0x84			
18	0x12	**CGMS_LO**	0xD6			
	Bit 0 to 7	CGMS level low	0xD6			
19	0x13	**CGMS_MISC**	0x22			
	Bit 0 to 1	CGMS level high bit 8 & 9	0			
	Bit 2 to 3	CGMS level low bit 8 & 9	0			
	Bit 4	Reference bit 1 (bit 3 for 4-bit ref.)				
	Bit 5	Reference bit 0 (bit 2 for 4-bit ref.)				
	Bit 6	Reference bit 1 (for 4-bit ref.)				
	Bit 7	Reference bit 0 (for 4-bit ref.)				
20	0x14	**CP25P_CTRL**	0x23			
	Bit 0 to 3	RESERVED	00			
	Bit 4 to 6	CGMS slew rate				000= no slew, 001=1 clk, …,110=6 clk
	Bit 7	RESERVED	0			
21 to 55	0x15 to 0x37	***RESERVED***	Don't Care			
56	0x38	**SERAT_PULS**	0x15			
	Bit 0 to 7	Bit 0 to 7 of 10 bit Serration value				
57	0x39	**SERAT_PULS MSB**	0x03			
	Bit 0 to 1	Bit 8 & 9 of Serration value				
	Bit 2 to 7	RESERVED				

Notes:

(1) Depends also on the sync mode (embedded digital sync or composite separate sync)

7. MECHANICAL SPECIFICATIONS



Symbol	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		22.00	BSC		0.866	
E		22.00	BSC		0.866	
e		0.50	BSC		0.020	
D1		20.00	BSC		0.787	
E1		20.00	BSC		0.787	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00	REF		0.039	
Y		0.08			0.003	
θ	0°	3.5°	7°	0°	3.5°	7°

All dimensions in millimeters (mm). Inches given for reference only.

Figure 14: 144-Pin Plastic Thin Quad Flat Pack

8. ORDERING INFORMATION

Order Code	Package	Speed		Temperature Range
		1x Horizontal Over-sampled Pixels	2x Horizontal Over-sampled Pixels	
gmCP1-BA	144-pin TQFP	27MHz	54MHz	0-70°C