# 10/100 LAN Interface Module for PC Card applications

## EPF8029G

• Recommended for use with SSI78Q2120 •

• Guaranteed to operate with 8 mA DC bias at 70°C •
Low profile, fully integrated with two channels

• Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards •

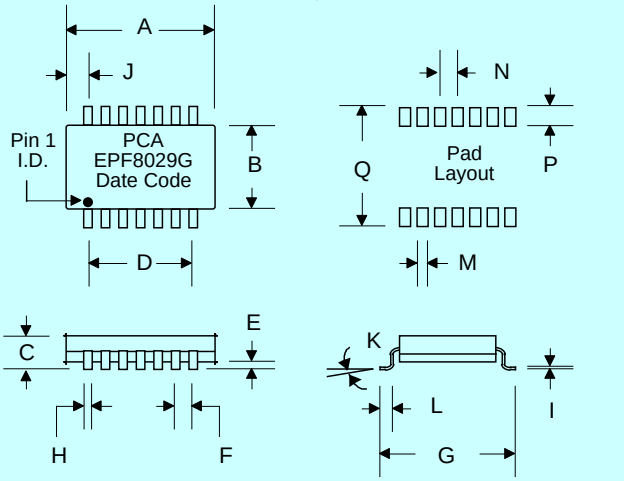
### Electrical Parameters @ 25° C

| **OCL** @ 70°C | **Insertion Loss** (dB Max.) | | | | | | **Return Loss** (dB Min.) | | | | | | **Common Mode Rejection** (dB Min.) | | | | | | **Crosstalk** (dB Min.) [Between Channels] | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 KHz, 0.1 Vrms 8 mA DC Bias | 1-80 MHz | | 80-100 MHz | | 100-150 MHz | | 1-30 MHz | | 30-60 MHz | | 60-100 MHz | | 1-30 MHz | | 30-100 MHz | | 100-500 MHz | | 5-10 MHz | 10-100 MHz |
| **Cable Side** | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | | |
| 350µH | -1 | -1 | -1 | -1 | -3.5 | -3 | -20 | -20 | -17 | -17 | -10 | -10 | -38 | -38 | -30 | -30 | -10 | -10 | -40 | -40 |

• **Isolation** : 1500 Vrms • **Impedance** : 100 Ω • **Rise Time** : 3.0 nS Max. •

### Schematic


### Package




### Dimensions

| Dim. | (Inches) Min. | Max. | Nom. | (Millimeters) Min. | Max. | Nom. |
|---|---|---|---|---|---|---|
| A | .790 | .810 | | 20.06 | 20.57 | |
| B | .510 | .530 | | 12.95 | 13.46 | |
| C | .088 | .098 | | 2.24 | 2.49 | |
| D | .600 | Typ. | | 15.24 | Typ. | |
| E | .003 | .020 | | 0.076 | .508 | |
| F | .100 | Typ. | | 2.54 | Typ. | |
| G | .660 | .680 | | 16.76 | 17.27 | |
| H | .016 | .022 | | .406 | .559 | |
| I | .008 | .012 | | .203 | .305 | |
| J | .090 | Typ. | | 2.28 | Typ. | |
| K | 0° | 8° | | 0° | 8° | |
| L | .025 | .045 | | .635 | 1.14 | |
| M | | | .030 | | | .762 |
| N | | | .100 | | | 2.54 |
| P | | | .085 | | | 2.16 |
| Q | | | .700 | | | 17.78 |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The circuit below is a guideline for interconnecting PCA's EPF8029G with the SSI78Q2120 10/100 Mb/s transceiver.

Typical insertion loss of the isolation transformer is 0.7dB. This parameter covers the entire spectrum of the encoded signals in 10/100 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you may have to adjust the load resistors on the chip to get at least 2.15V pk-pk across pins 12-14 or adjust R0 pulled to VCC; evidently, maximum voltage is obtained is R0=0Ω as shown below. The receiver channel connection is straight forward in that it only requires a split 50Ω termination across pins 1 and 2. The center of the load can be conveniently used for enhancing local common mode rejection further.

If center taps of the transceiver side are being used, note that the shunt capacitor to system ground need only to be a low-voltage capacitor. The range of values could only be determined from EMI test results. If shunt capacitors are present on the secondary center tap, it is common practice to use high voltage capacitors on the cable side.

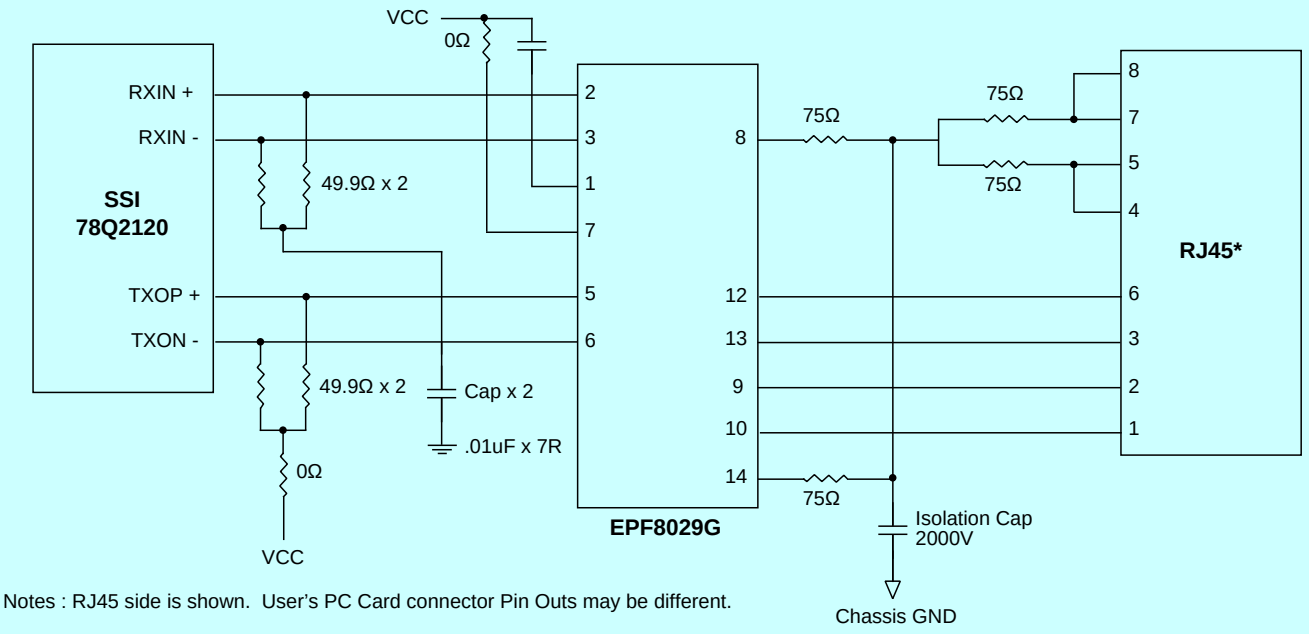
The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75Ω shown from the center taps of the secondary may be taken to chassis ground via a cap of suitable value. This depends upon user's design, EMI margin etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8029G. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50Ω, balanced and well coupled to achieve minimum radiation from these traces.

**Typical Application Circuit for UTP CAT5 (Excerpts from SSI 78Q2120 application notes)**




Notes : RJ45 side is shown. User's PC Card connector Pin Outs may be different.

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