4-Port 10 Base-T Interface Module with enhanced Common Mode Attenuation

EPE6243S

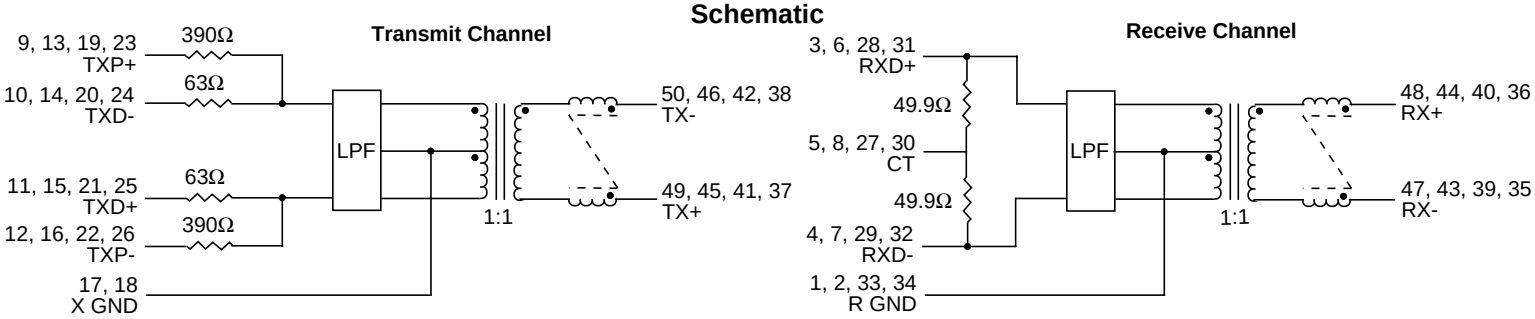
- Optimized for LSI Chip L64381 •
- Robust construction allows for solder reflow processes •
- Complies with or exceeds IEEE 802.3, 10 Base-T Requirements •

Electrical Parameters @ 25° C

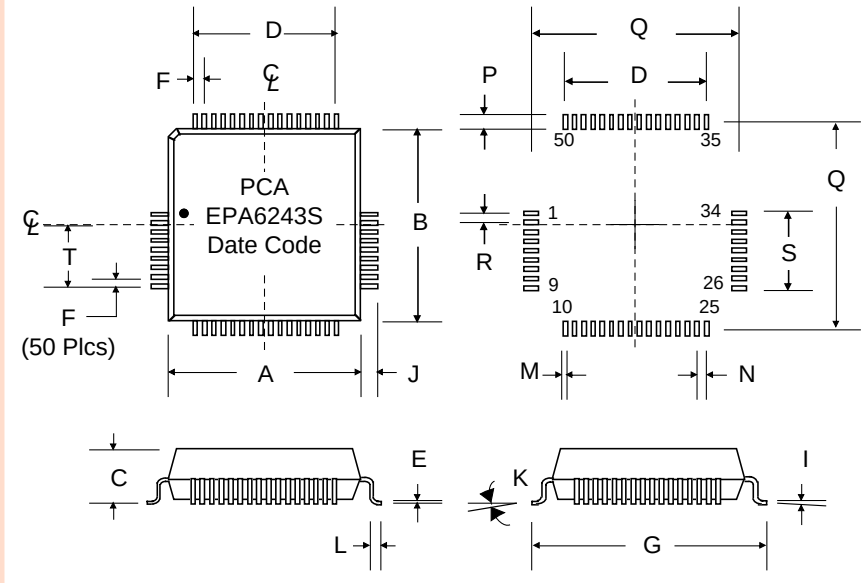
Cut-off Frequency (MHz)(1)		Insertion Loss (dB Max.)(†)		Return Loss (dB Min.)		Attenuation (dB Min.)(†)						Common Mode Rejection (dB Min.)										Crosstalk (dB Min.)	
± 1.0 MHz	± 1.5 MHz	1-10 MHz		5-10 MHz		@ 20 MHz		@ 25 MHz		@ 30 MHz		@ 5 MHz		@ 10 MHz		@ 50 MHz		@ 100 MHz		@ 200 MHz		@ 1-10 MHz	
Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv
17	19.5	-6	-6.5	-15	-15	-8	-6	-16	-11	-27	-16	-50	-32	-45	-30	-40	-30	-30	-38	-25	-27	-30	-30

• **Optimized design to give 3nS group delay difference over 5MHz-10MHz** • **†Resistor Network Included** •

Schematic



Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(Millimeters) Min.	Max.	Nom.
A	1.00	SQ		25.40	SQ	
B	1.00	SQ		25.40	SQ	
C	.265	.285		.265	7.24	
D	.750	Typ.		19.05	Typ.	
E	.003	.020		.076	.508	
F	.050	Typ.		1.27	Typ.	
G	1.150	SQ		29.21	SQ	
H	.016	.022		.406	.559	
I	.008	.012		.203	.305	
J	.090	Typ.		2.29	Typ.	
K	0°	8°		0°	8°	
L	.035	.055		.889	1.40	
M			.025			.635
N			.050			1.27
P			.080			2.03
Q			1.100			27.94
R			.075			1.91
S			.400			10.16
T	.325	Typ.		8.26	Typ.	

PCA ELECTRONICS, INC.
16799 SCHOENBORN ST.
NORTH HILLS, CA 91343

TEL: (818) 892-0761
FAX: (818) 894-5791
http://www.pca.com

4-Port 10 Base-T Interface Module with Enhanced Common Mode Attenuation

EPE6243S

The circuit below is a guideline for interconnecting PCA's EPE6243S with a typical 10 Base-T PHY chip over UTP cable. Further details of system design, such as chip pin-out, etc. can be obtained from the specific chip manufacturer.

Typical insertion loss of the isolation transformer/filter alone is 0.7dB. This parameter covers the entire spectrum of the encoded signals in 10 Base-T protocols. However, the predistortion resistor network introduces some loss which has to be taken into account in determining how well your design meets the Standard Template requirements. Additionally, the following need to be considered while selecting resistor values : (a) The filter needs 100Ω termination, thus the Thevenin's equivalent resistance seen by the filter looking into the transmit outputs from the chip must be equal to a value close to 100Ω. The typical driver output impedance is 5Ω. The internal predistortion values are selected appropriately for each input. Following these guidelines will guarantee that the return loss specifications are satisfied at all extremes of cable impedance (i.e. 85Ω to 115Ω) while the module is installed in your system. (b) That the template requirements are satisfied under the worst case Vcc (i.e. 4.5V), will impose a further constraint on resistor selection, in that they ought to be the minumum derived from the calculations. The values chosen by LSI application are optimum enough to satisfy this.

Note that some systems have auto polarity detection and some do not. If not, be certain to follow the proper polarity.

It is recommended that the chip side center taps are returned to ground via low voltage capacitors. The EMI situation generally improves only if the system ground return used to shunt common mode energy is itself a "quiet" ground. System designers need to bear this in mind while testing for EMI or laying the PCB out.

The pulldown resistors used around the RJ45 connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized. Legacy 10 Base T system designs generally did not incorporate this feature of containing EMI but use of this technique is wide spread in recent 10/100 solutions.

It is recommended that there is a neat separation of ground planes in the layout. It is a generally accepted practice to limit the plane off at least 0.08 inches away from the chip side pins of EPE6243S. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP shown for one port only