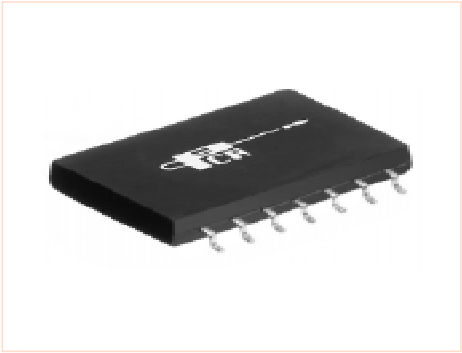
PCA ELECTRONICS INC.

10 Base-T Module with Enhanced Common Mode Attenuation

EPE6138



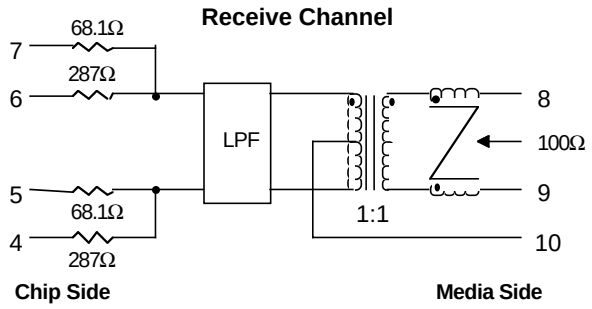
- For Card Bus ASIC solutions requiring predistortion • (similar to AT&T T7240)
- Robust design allows for toughest soldering processes •
- Complies with or exceeds IEEE 802.3, 10 Base-T Requirements •

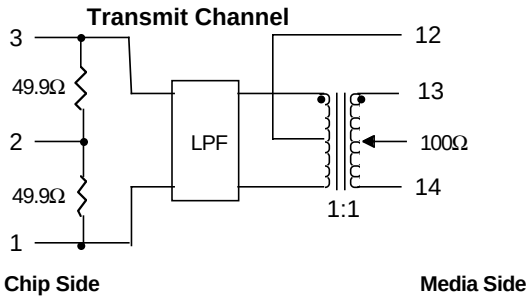
Electrical Parameters @ 25° C

Cut-off Frequency (MHz)		Insertion Loss (dB Max.)		Return Loss (dB Min.)		Attenuation (dB Min.)								Common Mode Rejection (dB Min.)						Crosstalk (dB Min.)	
±1.0 MHz		1-10 MHz		5-10 MHz		@ 20 MHz		@ 25 MHz		@ 30 MHz		@ 40 MHz		@ 50 MHz		@ 100 MHz		@ 200 MHz		@ 1-10 MHz	
Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv
17	17	-1	-1	-18	-18	-7	-5	-18	-11	-35	-18	-35	-18	-45	-40	-35	-30	-30	-25	-50	-50

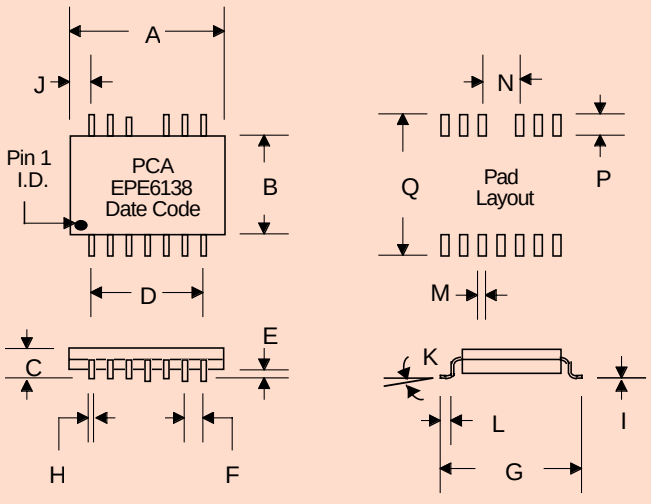
• **Isolation** : meets or exceeds 802.3 IEEE Requirements • **Characteristic Filter Impedance** : 100 Ω •

Schematic





Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(Millimeters) Min.	Max.	Nom.
A	.790	.810		22.86	23.62	
B	.510	.530		9.40	.991	
C	.088	.094		2.24	2.39	
D	.600	Typ.		15.24	Typ.	
E	.003	.010		.076	.254	
F	.100	Typ.		2.54	Typ.	
G	.670	Typ.		17.02	Typ.	
H	.016	.020		.406	.508	
I	.010	Typ.		.254	Typ.	
J	.100	Typ.		2.54	Typ.	
K	0°	8°		0°	8°	
L	.030	.050		.762	1.27	
M			.030			.762
N			.200			5.08
P			.085			2.16
Q			.700			17.78

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The circuit below is a guideline for interconnecting PCA's EPE6138 with ASICS for 10 Base-T PHY chip over UTP cable Further details of system design, such as chip pin-out, etc. can be obtained from the Card Bus specific chip manufacturer.

Typical insertion loss of the isolation transformer/filter is 0.7dB. This parameter covers the entire spectrum of the encode signals in 10 Base-T protocols. However, the predistortion resistor network introduces some loss which has to be taker into account in determining how well your design meets the Standard Template requirements.
Thevenin's equivalent termination impedance provided by the transmitt outputs is 2*(287//68.1)Ω or approx. 110Ω. Thus bench testing for return loss will assume an output impedance less than 1Ω on each of the driver outpust.
Note that some systems have auto polarity detection and some do not. If not, be certain to follow the proper polarity.

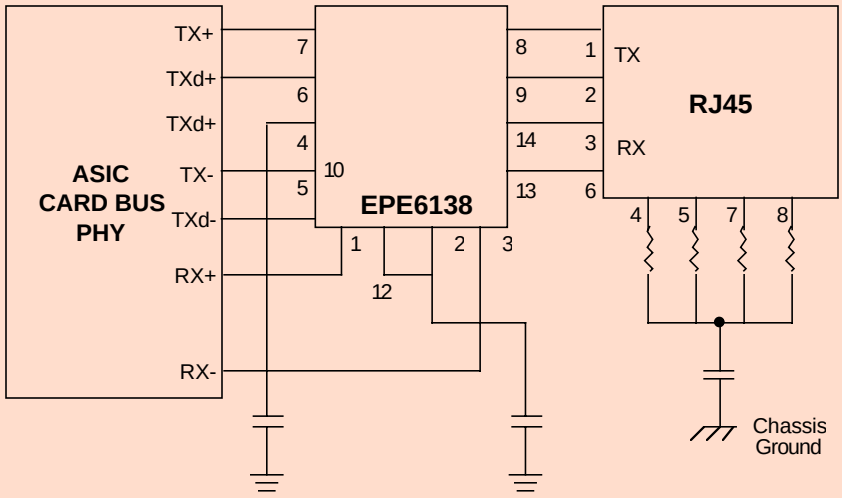
It is recommended that system designers ground the chip side center taps via a low voltage capacitor. Taking the cabl side center taps to chassis via capacitors, is not recommended, as this will add cost without containing EMI. This ma worsen EMI, specifically if the primary "common mode termination" is pulled to ground as shown.

The pulldown resistors used around the RJ45 connector have been known to suppress unwanted radiation that unuse wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design i finalized.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limi the plane off at least 0.08 inches away from the chip side pins of EPE6138. There need not be any ground plane beyon this point.

For best results, PCB designer should design the outgoing traces preferably to be 50Ω, balanced and well coupled t achieve minimum radiation from these traces.

Typical Application Circuit for UTP PC Card



Notes : * Pin-outs shown are for NIC configurations.

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