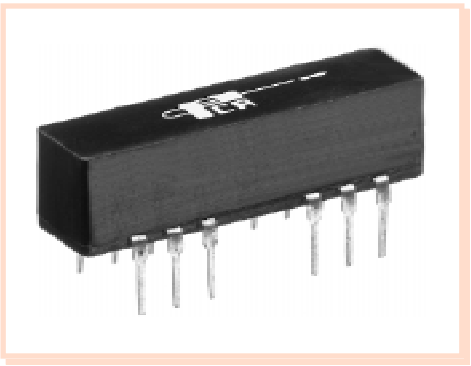
# 10 Base-T Interface Module

## EPA2013D



- General Purpose 10 Base-T Filter Module •
- Available in SMD and DIP Packages •
- Complies with or exceeds IEEE 802.3, 10 Base-T Requirements •

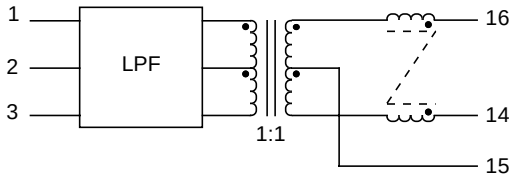
### Electrical Parameters @ 25° C

| Cut-off Frequency (MHz) | | Insertion Loss (dB Max.) | | Return Loss (dB Min.) | | Attenuation (dB Min.) | | | | | | | | Common Mode Rejection (dB Min.) | | | | | | Crosstalk (dB Min.) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ± 1.0 MHz | | 1-10 MHz | | 5-10 MHz | | @ 20 MHz | | @ 25 MHz | | @ 30 MHz | | @ 40 MHz | | @ 50 MHz | | @ 100 MHz | | @ 200 MHz | | @ 1-10 MHz | |
| Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv |
| 17 | 17 | -1 | -1 | -15 | -15 | -7 | -6 | -19 | -14 | -30 | -20 | -35 | -31 | -30 | --- | -25 | --- | --- | --- | -30 | -30 |

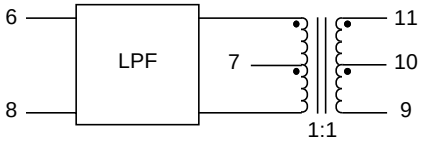
• **Isolation** : meets or exceeds 802.3 IEEE Requirements • **Characteristic Filter Impedance** : 100 Ω •
• Referenced to the Output Level Fundamental Frequency @ 5 MHz •

### Schematic

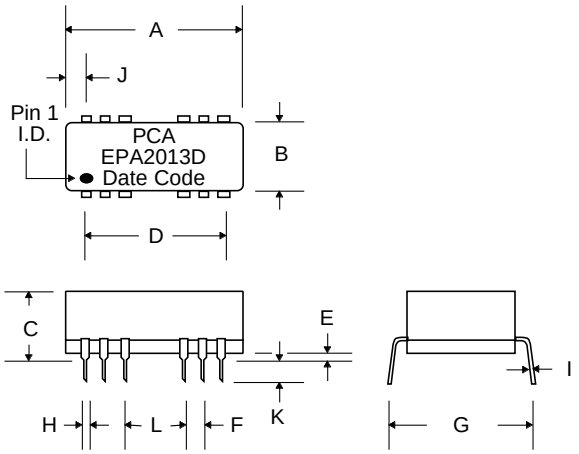
**Transmit Channel**




**Receive Channel**




### Package




### Dimensions

| Dim. | (Inches) Min. | Max. | Nom. | (Millimeters) Min. | Max. | Nom. |
|---|---|---|---|---|---|---|
| A | .980 | 1.00 | | 25.15 | 25.4 | |
| B | .260 | .280 | | 6.60 | 7.11 | |
| C | .290 | .310 | | 7.37 | 7.87 | |
| D | .700 | Typ. | | 17.78 | Typ. | |
| E | .020 | .030 | | .508 | .387 | |
| F | .100 | Typ. | | 2.54 | Typ. | |
| G | .310 | .375 | | 7.87 | 9.53 | |
| H | .018 | .022 | | .457 | .559 | |
| I | .008 | .012 | | .203 | .305 | |
| J | .200 | Typ. | | 5.08 | Typ | |
| K | .125 | .150 | | 3.18 | 3.81 | |
| L | .300 | Typ. | | 7.62 | Typ. | |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# 10 Base-T Interface Module

## EPA2013D

The circuit below is a guideline for interconnecting PCA's EPA2013D with a typical 10 Base-T PHY chip over UTP cable. Further details of system design, such as chip pin-out, etc. can be obtained from the specific chip manufacturer.

Typical insertion loss of the isolation transformer/filter is 0.7dB. This parameter covers the entire spectrum of the encoded signals in 10 Base-T protocols. However, the predistortion resistor network introduces some loss which has to be taken into account in determining how well your design meets the Standard Template requirements. Additionally, the following need to be considered while selecting resistor values :

a. The filter needs 100Ω termination, thus the Thevenin's equivalent resistance seen by the filter looking into the transmit outputs from the chip must be equal to a value close to 100Ω. The typical driver output impedance is 5Ω. Thus choose R1 and R2 values that are lowered by 5Ω on each leg. Following these guidelines will guarantee that the return loss specifications are satisfied at all extremes of cable impedance (i.e. 85Ω to 115Ω) while the module is installed in your system.
b. That the template requirements are satisfied under the worst case Vcc (i.e. 4.5V), will impose a further constraint on resistor selection, in that they ought to be the minimum derived from the calculations. Add R3 for more flexibility in setting voltage levels at the outputs.

Note that some systems have auto polarity detection and some do not. If not, be certain to follow the proper polarity.

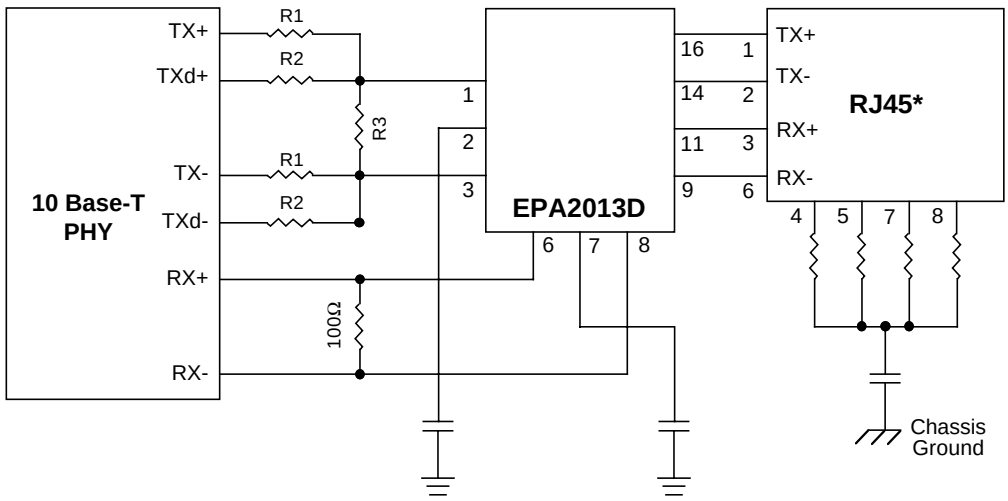
It is recommended that system designers ground the chip side center taps via a low voltage capacitor. Taking the cable side center taps to chassis via capacitors, is not recommended, as this will add cost without containing EMI. This may worsen EMI, specifically if the primary "common mode termination" is pulled to ground as shown.

The pulldown resistors used around the RJ45 connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.08 inches away from the chip side pins of EPA2013D. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50Ω, balanced and well coupled to achieve minimum radiation from these traces.

**Typical Application Circuit for UTP with external Resistor Network**




Notes : * Pin-outs shown are for NIC configurations.
For Hubs and Repeaters swap pins 1-2 with pins 3-6.

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