

EMX1DXV6T1, EMX1DXV6T5

Preferred Devices

Dual NPN General Purpose Amplifier Transistor

This NPN transistor is designed for general purpose amplifier applications. This device is housed in the SOT-563 package which is designed for low power surface mount applications, where board space is at a premium.

- Reduces Board Space
- High h_{FE} , 210–460 (Typical)
- Low $V_{CE(sat)}$, < 0.5 V
- Available in 7 inch Tape and Reel
- Pb-free Solder Plating

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{(BR)CBO}$	60	Vdc
Collector-Emitter Voltage	$V_{(BR)CEO}$	50	Vdc
Emitter-Base Voltage	$V_{(BR)EBO}$	7.0	Vdc
Collector Current – Continuous	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	–55 to +150	$^\circ\text{C}$

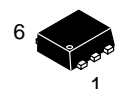
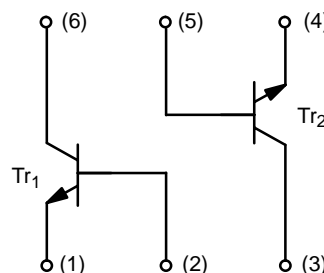
1. FR–4 @ Minimum Pad



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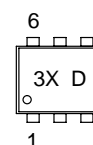
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DUAL NPN GENERAL PURPOSE AMPLIFIER TRANSISTORS SURFACE MOUNT



**SOT-563
CASE 463A
Style 1**

MARKING DIAGRAM



3X = Specific Device Code
D = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
EMX1DXV6T1	SOT-563	4 mm pitch 4000/Tape & Reel
EMX1DXV6T5	SOT-563	2 mm pitch 8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage ($I_C = 50\ \mu\text{Adc}$, $I_E = 0$)	$V_{(BR)CBO}$	60	–	–	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 1.0\ \text{mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	50	–	–	Vdc
Emitter-Base Breakdown Voltage ($I_E = 50\ \mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	7.0	–	–	Vdc
Collector-Base Cutoff Current ($V_{CB} = 60\ \text{Vdc}$, $I_E = 0$)	I_{CBO}	–	–	0.5	μA
Emitter-Base Cutoff Current ($V_{EB} = 7.0\ \text{Vdc}$, $I_B = 0$)	I_{EBO}	–	–	0.5	μA
Collector-Emitter Saturation Voltage ⁽²⁾ ($I_C = 50\ \text{mAdc}$, $I_B = 5.0\ \text{mAdc}$)	$V_{CE(sat)}$	–	–	0.4	Vdc
DC Current Gain ⁽²⁾ ($V_{CE} = 6.0\ \text{Vdc}$, $I_C = 1.0\ \text{mAdc}$)	h_{FE}	120	–	560	–
Transition Frequency ($V_{CE} = 12\ \text{Vdc}$, $I_C = 2.0\ \text{mAdc}$, $f = 30\ \text{MHz}$)	f_T	–	180	–	MHz
Output Capacitance ($V_{CB} = 12\ \text{Vdc}$, $I_C = 0\ \text{Adc}$, $f = 1\ \text{MHz}$)	C_{OB}	–	2.0	–	pF

2. Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, D.C. $\leq 2\%$.

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TYPICAL ELECTRICAL CHARACTERISTICS

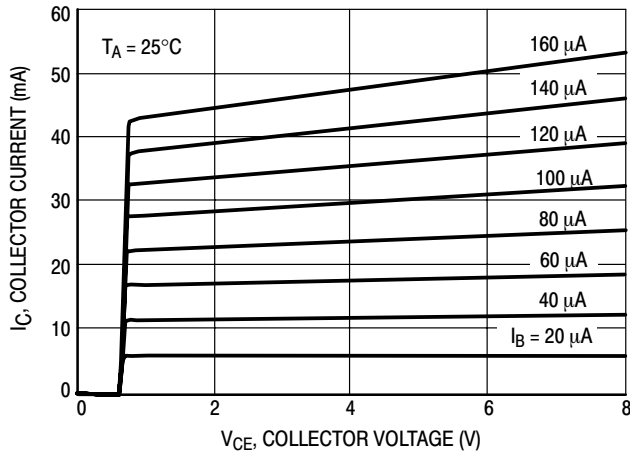


Figure 1. $I_C - V_{CE}$

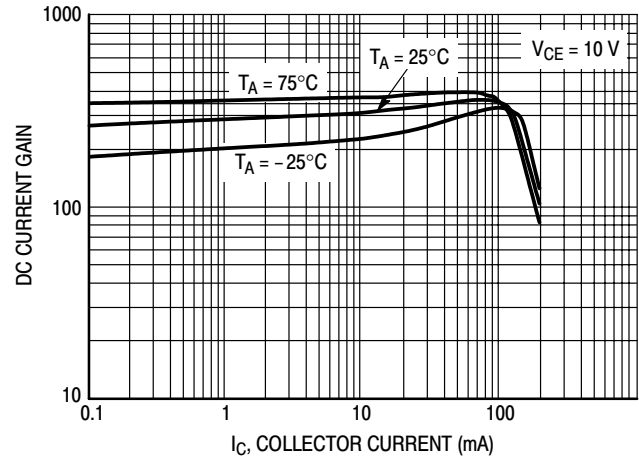


Figure 2. DC Current Gain

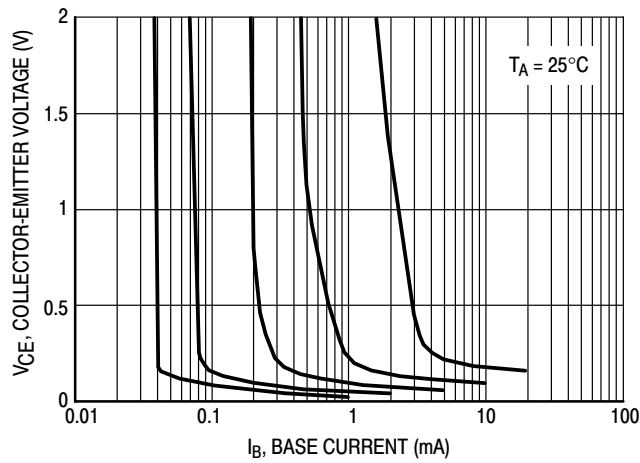


Figure 3. Collector Saturation Region

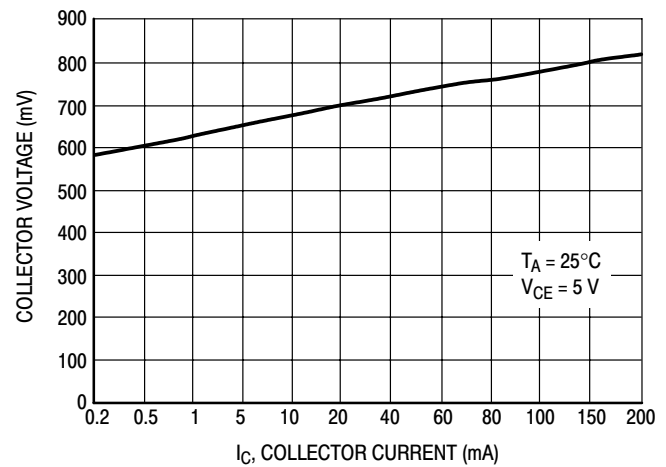


Figure 4. On Voltage

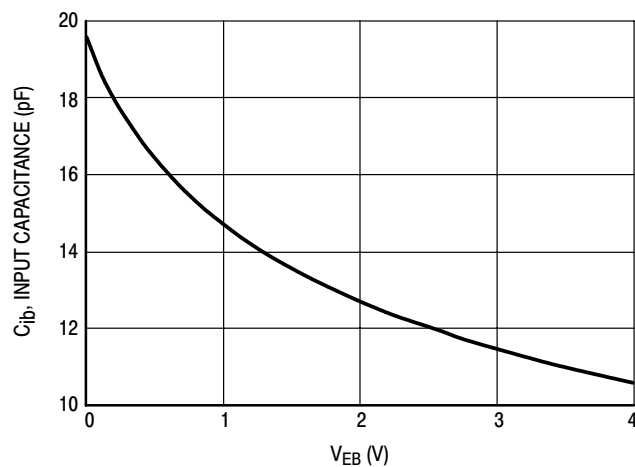


Figure 5. Capacitance

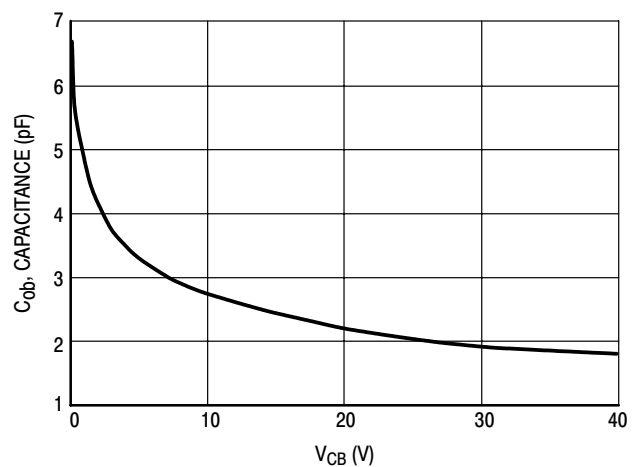
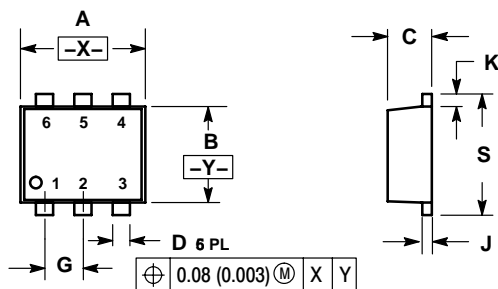


Figure 6. Capacitance

EMX1DXV6T1, EMX1DXV6T5

PACKAGE DIMENSIONS

SOT-563, 6 LEAD
CASE 463A-01
ISSUE D



NOTES:

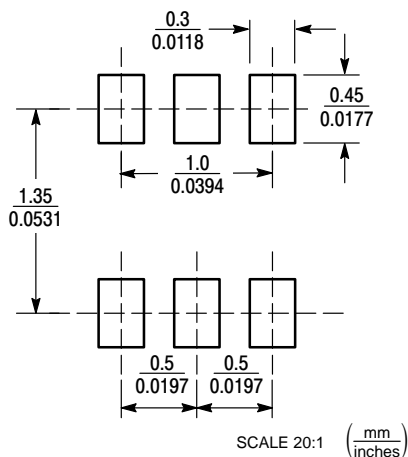
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

STYLE 1:

- PIN 1. EMITTER 1
- BASE 1
- COLLECTOR 2
- EMITTER 2
- BASE 2
- COLLECTOR 1

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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