Triple 80MHz Video Amplifier w/Disable

élantec

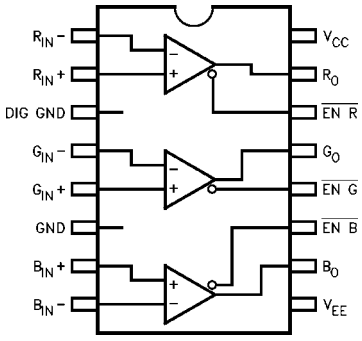
The EL4393 is three wideband current-feedback amplifiers optimized for video performance. Each amplifier can drive a load of 150Ω at video levels. Each amplifier has a disable capability, which is controlled by a TTL/CMOS compatible logic signal. The EL4393 operates on supplies as low as ±4V up to ±15V.

Being a current-feedback design, the bandwidth stays relatively constant at approximately 80MHz over the ±1 to ±10 gain range. The EL4393 has been optimized for use with 1300Ω feedback resistors at a gain of 2.

When the outputs are disabled, the supply current consumption drops, by about 4mA per channel that is disabled. This feature can be used to reduce power dissipation.

Pinout

EL4393
(16-PIN PDIP, SO)
TOP VIEW



Features

- 80MHz -3dB bandwidth for gains of 1 to 10
- 900V/µs slew rate
- 10MHz bandwidth flat to 0.1dB
- Excellent differential gain and phase
- TTL/CMOS compatible
- Available in SOL-16

Applications

- RGB drivers
- RGB multiplexers
- RGB gain blocks
- Video gain blocks
- Coax cable driver
- ADC drivers/input multiplexer

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL4393CN	-40°C to +85°C	16-Pin PDIP	MDP0031
EL4393CM	-40°C to +85°C	16-Pin SOL	MDP0027

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S- . . . . . +33V
Voltage at V_S+ . . . . . +18V
Voltage at V_S- . . . . . -18V
Voltage between V_{IN}+ and V_{IN}- . . . . . ±6V
Current into V_{IN}+ or V_{IN}- 5mA

Internal Power Dissipation . . . . . See Curves
Operating Ambient Temperature Range . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . 150°C
Storage Temperature Range . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

Supplies at ±15V, Load = 1kΩ

PARAMETER	DESCRIPTION	TEMP	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	+25°C		2	±15	mV
TCV_{OS}	Temperature Coefficient of V_{OS}	Full		50		µV/°C
I_B+	I_{IN}+ Input Bias Current	+25°C		0.2	5	µA
I_B-	I_{IN}- Input Bias Current	+25°C		10	65	µA
TCI_B-	Temperature Coefficient of I_B-	Full		25		nA/°C
CMRR	Common-Mode Rejection Ratio (Note 1)	+25°C	50	58		dB
-ICMR	I_{IN}- Input Common-Mode Current (Note 1)	+25°C		3	8	µA/V
PSRR	Power Supply Rejection Ratio (Note 2)	+25°C	50	58		dB
-IPSR	I_{IN}- Current Supply Rejection (Note 2)	+25°C		2	5	µA/V
R_{OL}	Transimpedance	+25°C	100	217		kΩ
R_{IN}	IN+ Input Impedance	+25°C		2		MΩ
V_{IN}	IN+ Input Range	+25°C	±13	±13.5		V
V_O	Output Voltage Swing; R_L = 1kΩ	+25°C	±12	±13		V
I_{SC}	Short-Circuit Current (Note 3)	+25°C	40	70		mA
$I_{O, DIS}$	Output Current when Disabled	+25°C		5	150	µA
DIS V_{IL}	Disable Voltage for Logic Low	+25°C			0.8	V
DIS V_{IH}	Disable Voltage for Logic High	+25°C	2.2			V
DIS I_{IL}	Disable Logic Low Input Current	+25°C		3	25	µA
DIS I_{IH}	Disable Logic High Input Current	+25°C		0	5	µA
$I_{CC (en)}$	Positive Supply Current all Channels Enabled	+25°C	15	20	±29	mA
$I_{CC (dis)}$	Positive Supply Current all Channels Disabled	+25°C	6	11	16	mA
$I_{EE (en)}$	Negative Supply Current all Channels Enabled	+25°C	13	18	±28	mA
$I_{EE (dis)}$	Negative Supply Current all Channels Disabled	+25°C	4	9	14	mA

NOTES:

1. V_{CM} = ±10V for V_S = ±15V.
2. V_{OS} is measured at V_S = ±4.5V and V_S = ±16V, both supplies are changed simultaneously.
3. Only one output short-circuited. Pulse test or use heatsink.

AC Electrical Specifications

Supplies at ±15V, Load = 150Ω and 15pF, except where noted. Rf1 and Rf2 = 1500Ω; A_V = 2, T_A = 25°C.(Note 1)

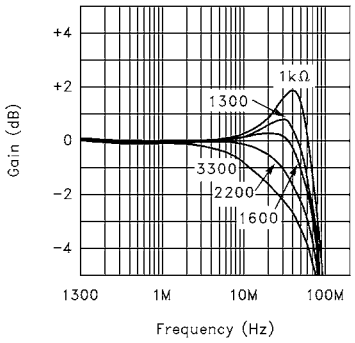
PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
SR	Slew Rate (Note 2)		960		V/µs
SR	Slew Rate w/±5V Supplies (Note 3)		470		V/µs
t_S	Settling Time to 1% $5V_{P-P}$ 5V Step (Note 4)		32		ns
BW	Bandwidth, -3dB ±5V Supplies, -3dB		80 60		MHz MHz
BW	Bandwidth, -0.1dB ±5V Supplies, -0.1dB		16 21		MHz MHz
Peaking	-3dB BW Tests		0.6		dB
dG	Differential Gain at 3.58MHz at ±5V Supplies (Note 5)		0.03 0.30		% %
dθ	Differential Phase at 3.58MHz at ±5V Supplies (Note 5)		0.088 0.096		(°) (°)

NOTES:

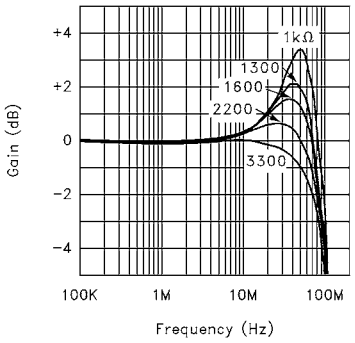
1. Test fixture was designed to minimize capacitance at the I_N+ input. A “good” fixture should have less than 2pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.
2. R_L = 300Ω, -5V to +5V swing, SR measured at 20% to 80%
3. -2V to +2V swing, SR measured at 20% to 80%.
4. R_L = 300Ω.
5. DC offset from -0.7V through +0.7V AC amplitude is $286mV_{P-P}$, equivalent to 40 ire.

Typical Performance Curves

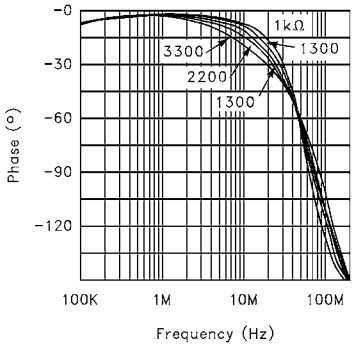
Gain Flatness vs Rf at ± 5V



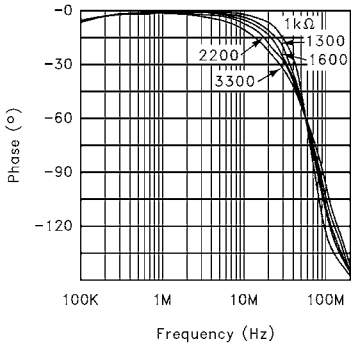
Gain Flatness vs Rf at ± 15V



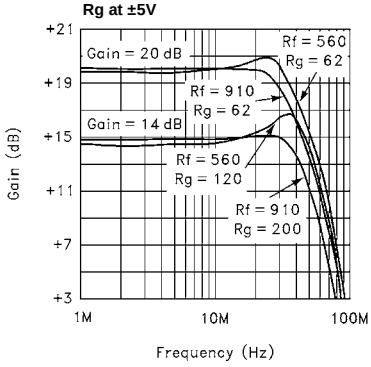
Phase vs Rf at ± 5V



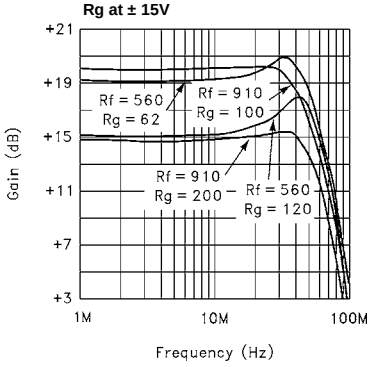
Phase vs Rf at ±15V



Gain of 5, 10 vs Various Rf, Rg at ±5V

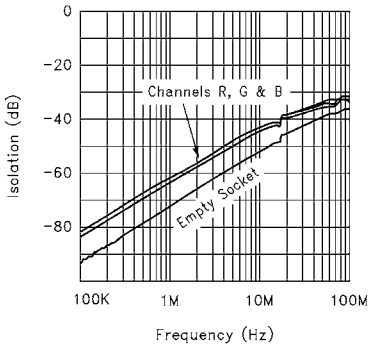


Gain of 5, 10 vs Rf, Rg at ± 15V

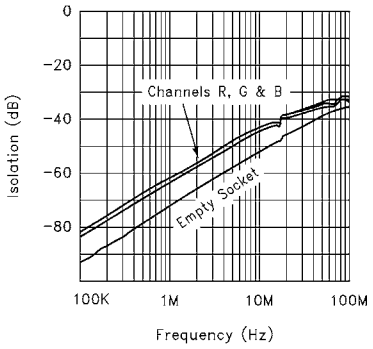


Typical Performance Curves (Continued)

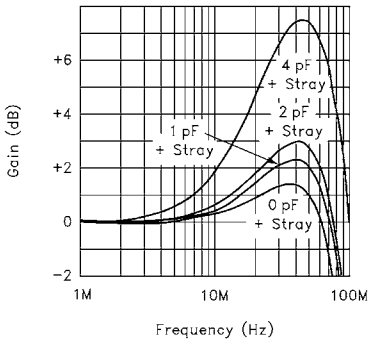
Disabled Isolation Test at ±5V



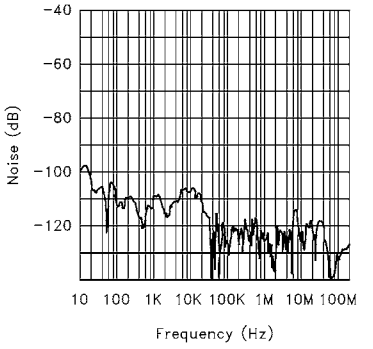
Disabled Isolation Test at ± 15V



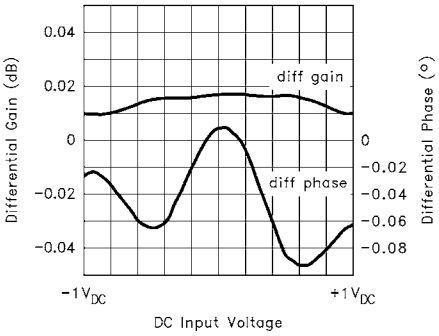
Cin—vs Peaking



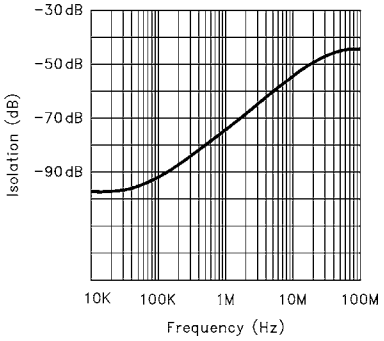
Voltage Noise



Differential Gain & Phase at 3.58MHz

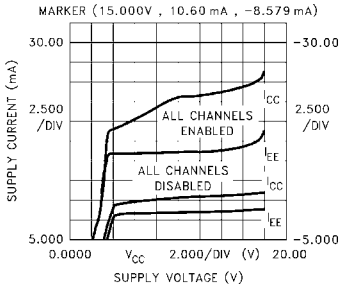


EL4393 MUX Channel Channel Isolation

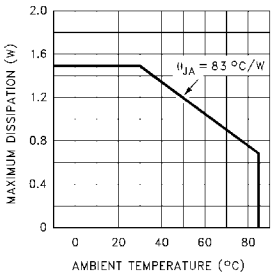


Typical Performance Curves (Continued)

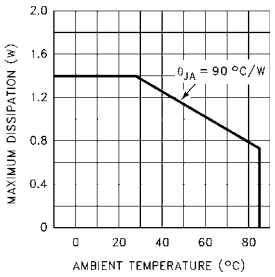
Supply Current vs Supply Voltage



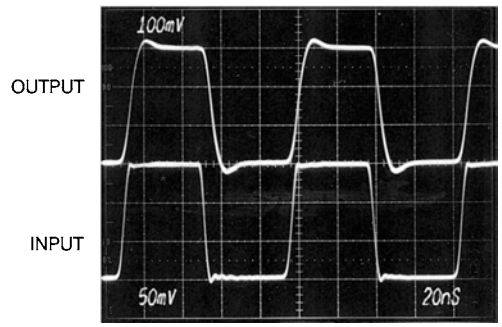
Maximum Power Dissipation vs Ambient Temperature— 16-Pin PDIP



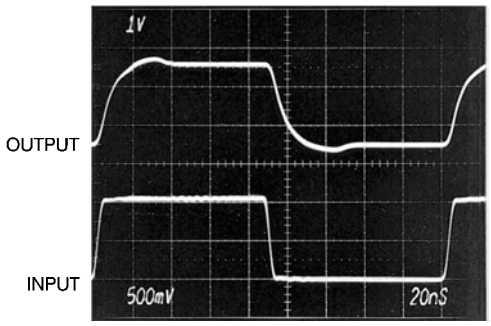
Maximum Power Dissipation vs Ambient Temperature— 16-Pin SOL



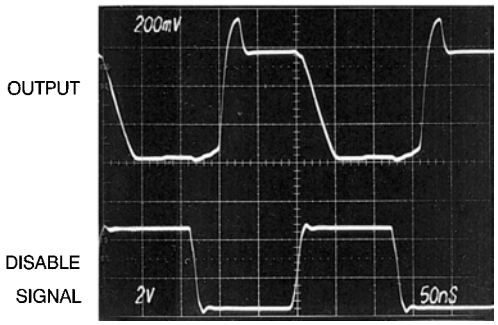
Small Signal Pulse Response



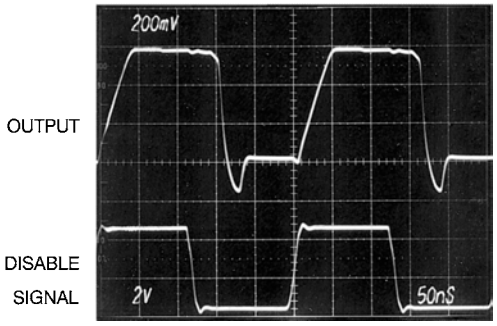
Large Signal Pulse Response



Small Signal Enable/Disable with +VE Voltage



Enable/Disable with -VE Voltage Output



Typical Application for EL4393, and General Rules for PCB Layout

The figure shows two EL4393s configured as a 2:1 RGB multiplexer, and cable driver, driving 75Ω, back terminated cables. Each channel of the EL4393 is configured to give a gain of two, to make up for the losses of the back terminating resistor.

In this example, the Disable pins of each RGB section are driven by a complementary TTL “select” signal. Larger multiplexers can be assembled, with a 1-of-n TTL decoder selecting each RGB triplet.

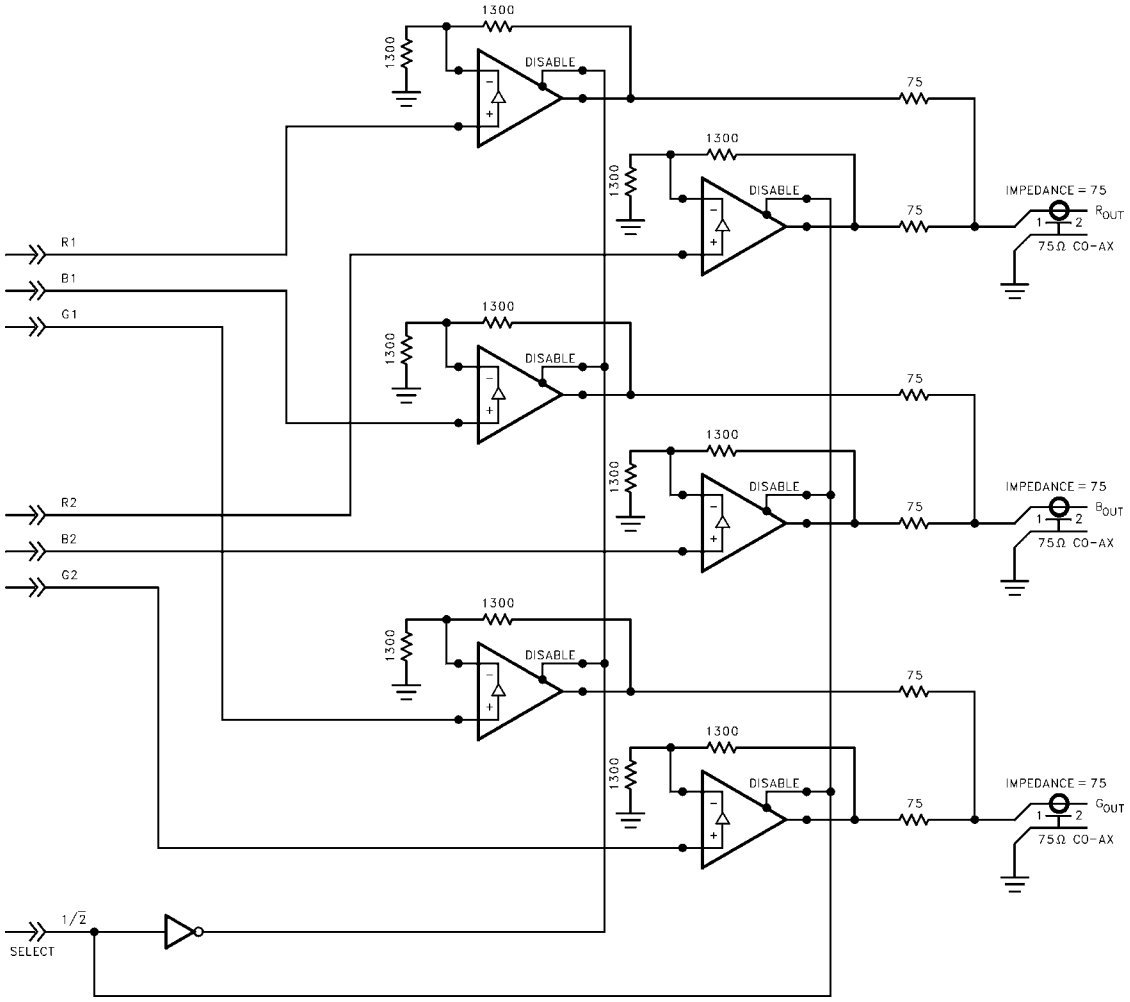
The circuit gives channel isolations of typically better than -50dB at 10MHz, and with a 20dB/decade slope, extending down to better than -90dB at frequencies below 100kHz.

The schematic does not show things like power supply decoupling, or pcb layout, grounding and signal returns, but these will all affect the overall performance of the circuit, and care should be taken with these aspects.

It is recommended that the V_{CC} and V_{EE} pins each be decoupled by a 0.1µF NPO or X7R dielectric ceramic capacitors to ground within 0.1 inch of the part, and in parallel with the 0.1µF, a 47µF tantalum capacitor, also to ground. The 47µF capacitors should be within 0.25 inch of their power

pins. The ground plane should be underneath the package, but cut away from the In- inputs. Care should be taken with the center channel feedback—it must be kept away from any of the In+ or In- pins, if it has to go under the package. Route the G-out line between the pin 3 ground and the pin 4 In- if going under the package is essential. Otherwise, loop the G-out trace around all the other circuitry, to its Rf resistor. The Rf and if used, Rg resistors should be on the input side of the package, to minimize trace length on the In- pins.

The digital input disables are on the output side of the package, so that a good ground plane down the center of the board underneath the package will isolate any fast edges from the sensitive inputs.

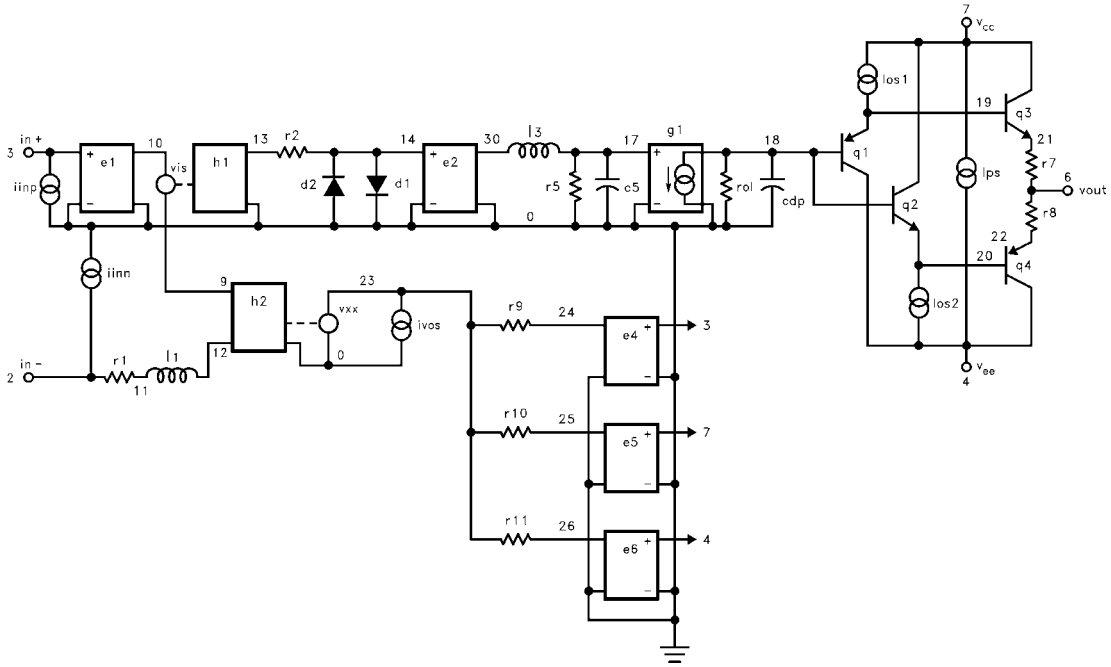


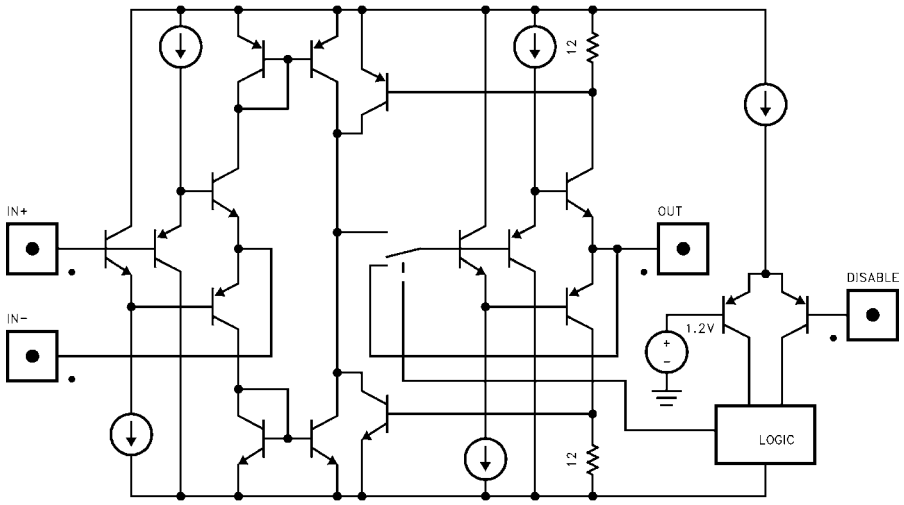
TYPICAL APPLICATION CIRCUIT

EL4393 Macromodel

```
* Revision A, July 1993
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                   |     -Input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     Putput
*                   |     |     |     |     |
* subckt EL4393/EL  3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l 1 11 12 29 nH
iinp 3 0 0.2 µA
iinm 2 0 10 µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l5 30 17 1.2 µH
c5 17 0 1 pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 250k
cdp 18 0 2.2 pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2.5 mA
ios2 20 4 2.5 mA
*
* Error Terms
*
ivos 0 23 2 mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 1K
```

```
r10 25 23 1K
r11 26 33 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.2nS)
.model qp pnp (is=5e-15 bf=100 tf=0.2nS)
.model dclamp d (is=1e-30 ibv=0.266 bv=1.5 n=4)
.ends
```





SIMPLIFIED SCHEMATIC OF ONE CHANNEL OF EL4393