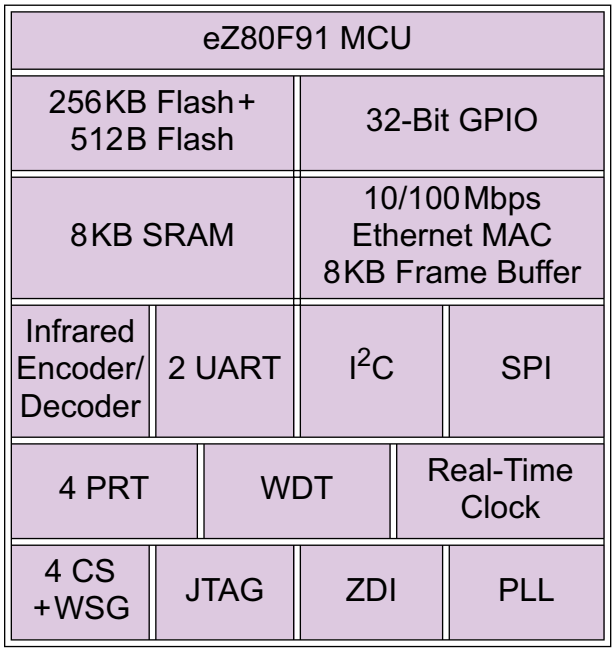
eZ80Acclaim!™ Flash Microcontrollers

eZ80F91 Product Brief

PB013502-0104

Product Block Diagram



Features

The eZ80F91 microcontroller is a member of ZiLOG's eZ80Acclaim!™ product family, which offers on-chip Flash versions of ZiLOG's eZ80® processor core. The eZ80F91 offers the following features:

- 50MHz High-Performance eZ80® CPU
- 256KB Flash Program Memory plus extra 512B device configuration Flash memory
- 32 bits of General-Purpose I/O
- 16KB total on-chip high-speed SRAM:
  - 8KB for general-purpose use
  - 8KB for 10/100BaseT Ethernet Media Access Controller (EMAC) high-speed frame buffer
- IrDA™-compatible Infrared Encoder/Decoder
- 2 UARTs with independent baud rate generators
- I^2C with independent clock rate generator
- SPI with independent clock rate generator
- Four Counter/Timers with prescalers supporting event counting, input capture, output compare, and PWM modes
- Watch-Dog Timer with internal RC clocking option
- Real-time clock with on-chip 32kHz oscillator, selectable 50/60Hz input, and separate RTC_V_{DD} pin for battery backup.
- Glueless external memory interface with 4 Chip-Selects/Wait-State Generators and external $\overline{WAIT}$ input pin. Supports Intel and Motorola buses.
- JTAG Interface supporting emulation features
- Low-power PLL and on-chip oscillator
- Programmable-priority vectored interrupts, non-maskable interrupts, and interrupt controller
- New DMA-like eZ80® CPU instructions
- Power management features supporting HALT/ SLEEP modes and selective peripheral power-down controls
- 144-pin BGA or 144-pin LQFP package
- 3.0–3.6 V supply voltage with 5 V tolerant inputs
- Operating Temperature Ranges:
  - Standard: 0ºC to +70ºC
  - Extended: –40ºC to +105ºC

General Description

The eZ80F91 device is an industry first, featuring a high-performance 8-bit microcontroller with an integrated 10/100 BaseT Ethernet Media Access controller (EMAC). It is a power-efficient, optimized pipeline architecture microcontroller with a maximum operating speed of 50 MHz. Offering on-chip Flash memory, SRAM, Ethernet MAC, and rich peripherals, the eZ80F91 is well-suited for industrial, communication, automation, security, and embedded Internet applications.

ZiLOG Worldwide Headquarters • 532 Race Street • San Jose, CA 95126
Telephone: 408.558.8500 • Fax: 408.558.8300 • www.ZiLOG.com

eZ80® CPU Core

The eZ80® CPU can operate in Z80-compatible (64 KB) mode or full 24-bit (16 MB) addressing mode. Considering both the increased clock speed and processor efficiency, the eZ80®'s processing power rivals the performance of 16-bit microprocessors. The eZ80® improves on the world-famous Z80 architecture. Like the Z80, it features dual bank registers for fast context switching.

eZ80F91 Peripherals Description

On-Chip Memory

The eZ80F91 device offers 256 KB of Flash program memory. A separate page of 512 bytes Flash memory is available for general device configuration data.

- Single power supply operation
- Page erase feature: 1024 bytes/page
- Fast page erase and byte program operation
- 60 ns maximum access time
- Endurance: 20,000 write cycles (typical)
- Data retention: greater than 100 years @ room temperature

In addition, 16 KB of high-speed, relocatable SRAM is available on-chip. 8 KB is for general-purpose use, and another 8 KB is used by the EMAC for Ethernet operation, but is also user-accessible for general use when Ethernet functionality is not required.

General-Purpose Input/Output

There are 32 bits of General-Purpose Input or Output (GPIO). All GPIO pins are individually programmable and support the following I/O modes: input, output, open drain, open source, level-triggered interrupts (High or Low), edge-triggered interrupts (High or Low), dual edge-triggered interrupts, and alternate function. Eight of the output pins can drive 10 mA each (Port A), while 16 other pins feature Schmitt-trigger input buffers (Ports B and C).

10/100 BaseT Ethernet MAC

The eZ80F91 device features an integrated IEEE 802.3 Ethernet controller with a total of 8 KB of dynamically-configurable Tx/Rx frame buffer. It supports speeds of 10 and 100 Mbps, full duplex operation, and an industry-standard Media Independent Interface (MII) for simple connection to an external Physical Layer interface (PHY) device. The eZ80F91 delivers high performance and overall cost effectiveness as an embedded network microcontroller.

High performance is achieved by optimizing the internal bus design of the eZ80® CPU with shared memories, dedicated Ethernet Tx/Rx DMAs, and Tx/Rx FIFOs. This bus design provides the highest data throughput over the Ethernet interface, yet requires minimum eZ80® CPU intervention and minimizes system loading.

Infrared Encoder/Decoder

- Supports IrDA SIR format
- Operates seamlessly with on-chip UART
- Interfaces with IrDA-compliant transceivers
- Supports transmit/receive to 115 Kbps

Universal Asynchronous Receiver/Transmitter

Each of the two Universal Asynchronous Receiver/Transmitter (UART) channels contains a transmitter, a receiver, control logic/registers, and a Baud Rate Generator (BRG).

- The Baud Rate Generator produces a lower-frequency bit clock from the system clock. All standard baud rates up to 115 Kbps (and higher) are supported.
- The UART module implements all of the logic required to support asynchronous communications, hardware flow control, and 9-bit character format. The module also contains separate 16-byte-deep transmit and receive FIFOs.

Inter-Integrated Circuit

The Inter-Integrated Circuit (I^2C) channel contains control registers and its own clock rate generator. The I^2C interface operates in four modes: Master Transmit or Receive, and Slave Transmit or

Receive. A standard and fast I^2C speed of 100kbps and 400kbps are supported.

Serial Peripheral Interface

The Serial Peripheral Interface (SPI) channel contains control registers and its own clock rate generator. The SPI is a synchronous serial interface allowing multiple SPI devices to be interconnected. The SPI interface may be configured to operate as a master or a slave.

Programmable Reload Timers

The eZ80F91 provides four independent Programmable Reloadable Counter Timers (PRT) to handle complex timing functions. Each timer is a 16-bit downcounter and offers a 4-bit clock prescaler with four selectable taps for CLK ÷ 4, CLK ÷ 16, CLK ÷ 64 and CLK ÷ 256. The timers can operate in basic mode supporting SINGLE-PASS or CONTINUOUS count. Additional features include 4 input captures, 4 output compares, 2 external event counters, and 4 PWMs that can operate independently or in unison. Any one of the input capture pins can be programmed as master PWM power-trip inputs.

Watch-Dog Timer

The Watch-Dog Timer (WDT) features four programmable time-out periods: 2^{18}, 2^{22}, 2^{25}, or 2^{27} system clock cycles. It can operate from either the main system clock, the on-chip 32kHz oscillator (from the RTC), or the internal RC oscillator. The time-out action of the WDT is user-programmable for either a hardware reset or a nonmaskable interrupt to the eZ80® CPU. The source of action taken after a WDT time-out is indicated by a WDT status bit.

Real-Time Clock

The real-time clock (RTC) allows counting of seconds, minutes, hours, days-of-the-week, day-of-the-month, month, year, and century. Alarms and interrupts can be set for seconds, minutes, hours, and day-of-the-week. The real-time clock input can be taken from the on-chip 32kHz oscillator or from a 50/60Hz input. The real-time clock operates from an isolated RTC_V_{DD} pin to allow constant operation from a battery.

Chip-Select/Wait State Generator and $\overline{\text{WAIT}}$ Pin

Four independent chip selects are available to facilitate glueless interface to system memory and external devices. Each chip select can be configured for up to 7 wait states, and supports either memory or I/O space. Memory chip selects can be individually programmed on a 64KB boundary. I/O chip selects can choose a 256-byte section of I/O space. The WAIT input pin allows interface with slow peripherals. Z80, Intel, and Motorola bus modes are supported.

JTAG Interface

An IEEE 1149.1-compatible five-pin test access port (TAP) is provided to interface with on-chip test logic defined by that standard. This TAP also includes Boundary Scan functions. For IEEE 1149.1 compliance, a pull-up resistor is required on pin TDI. Additionally, the TAP is used to control the on-chip emulation/debugging capabilities. Some included features are: software break points, a 64-word trace buffer, complex break points using address and data masks, and cascadable triggers.

PLL and On-Chip Crystal Oscillator

The eZ80F91 features a complete, low-power, programmable PLL that can be selected to generate the system clock. Taking its input from the on-chip crystal oscillator, the PLL can generate system clock speeds up to 50MHz from low-cost, low-frequency external crystals in the range of 1–10MHz..

ZiLOG Debug Interface

The ZiLOG Debug Interface (ZDI) incorporates most of the functions of an In-Circuit Emulator on-chip. ZDI allows the user to single-step code, change registers, edit programs, and view status of internal registers.

Block Transfer Instructions

Block transfer instructions with expanded repeat capability have been added to the eZ80® CPU. They provide high-performance data transfer similar to hardware DMAs.

Power Management

Several power management features are supported on the eZ80F91. Two peripheral power-down registers allow independent clock gating of on-chip peripherals under software control while operating under normal conditions. The eZ80® CPU can write to these control registers to disable the clock from driving any one of the peripherals when they are inactive.

In addition, execution of the HALT instruction suspends eZ80® CPU operation and eliminates clock power associated with the eZ80® CPU core. Normal operation can be restored via external and peripheral interrupts or hardware reset.

Execution of a sleep (SLP) instruction provides the lowest power consumption. In SLEEP mode, only the on-chip RTC 32kHz crystal oscillator remains active to drive the RTC and the WDT. All other peripherals, the system clock, and the primary oscillator are disabled. An RTC alarm, a WDT time-out, or hardware reset can reset the device.

Electrical Features Summary

- Power supply: 3.3V ± 0.3V
- Standard temperature: 0ºC to 70ºC
- Extended temperature: -40ºC to +105ºC
- Supply current @ 50MHz: 50mA (typical)
- Supply current in HALT mode with peripherals powered down: <5mA (typical)
- Supply current in SLEEP mode: <50µA (typical)

Support Tools

The following development tools are available to program and debug the eZ80F91 device:

- eZ80® Development Platform with plug-in eZ80F91 Module
- ZILOG TCP/IP software suite
- Operating system
- ANSI C-Compiler
- ZiLOG Developer's Studio Integrated Development Environment (ZDS IDE) including assembler, linker, debugger, and simulator

Related Products

Other integrated devices of interest are:

eZ80190	50 MHz eZ80® CPU, 8KB SRAM, 16x16 Multiply with 40-bit Accumulators, 32 bits GPIO, 6 Counter Timers with Prescalers, WDT, 4 channel CS+WSG, 2-Channel DMA, 2 UZI Channels, ZDI, On-Chip Oscillator.
eZ80L92	20MHz and 50MHz eZ80® CPU, low-power modes, 24 bits GPIO, IrDA, 2 UART, I^2C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4-channel CS, JTAG, ZDI.
eZ80F92	20MHz eZ80® CPU, low-power modes, 128KB+256B Flash, 8KB SRAM, 24 bits GPIO, IrDA, 2 UART, I^2C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4 channel CS+WSG, JTAG, ZDI, PLL.
eZ80F93	20MHz eZ80® CPU, low-power modes, 64KB+256B Flash, 4KB SRAM, 24 bits GPIO, IrDA, 2 UART, I^2C, SPI, 6 Counter Timers with I/O features, WDT, RTC, 4 channel CS+WSG, JTAG, ZDI.
Z80S180™	Improved Z80 CPU, 1MB MMU, 2 DMA, 2 16-bit PRTs, 2 UARTs, CSIO, up to 33MHz clock speed.
Z80181	Z8S180 CPU, SCC, CTC, 16-bit GPIO, up to 33MHz clock speed.
Z80182	Z8S180 CPU, 2 ESCC, 24-bit GPIO, 16550 Mimic interface, up to 33MHz clock speed.
Z84C00	Z80™ CPU (up to 20MHz).
Z84C15	Z80™ CPU, 2 SIO, 4x8 CTC, 2 PIO, WDT, up to 16 MHz clock speed.

Block Diagram

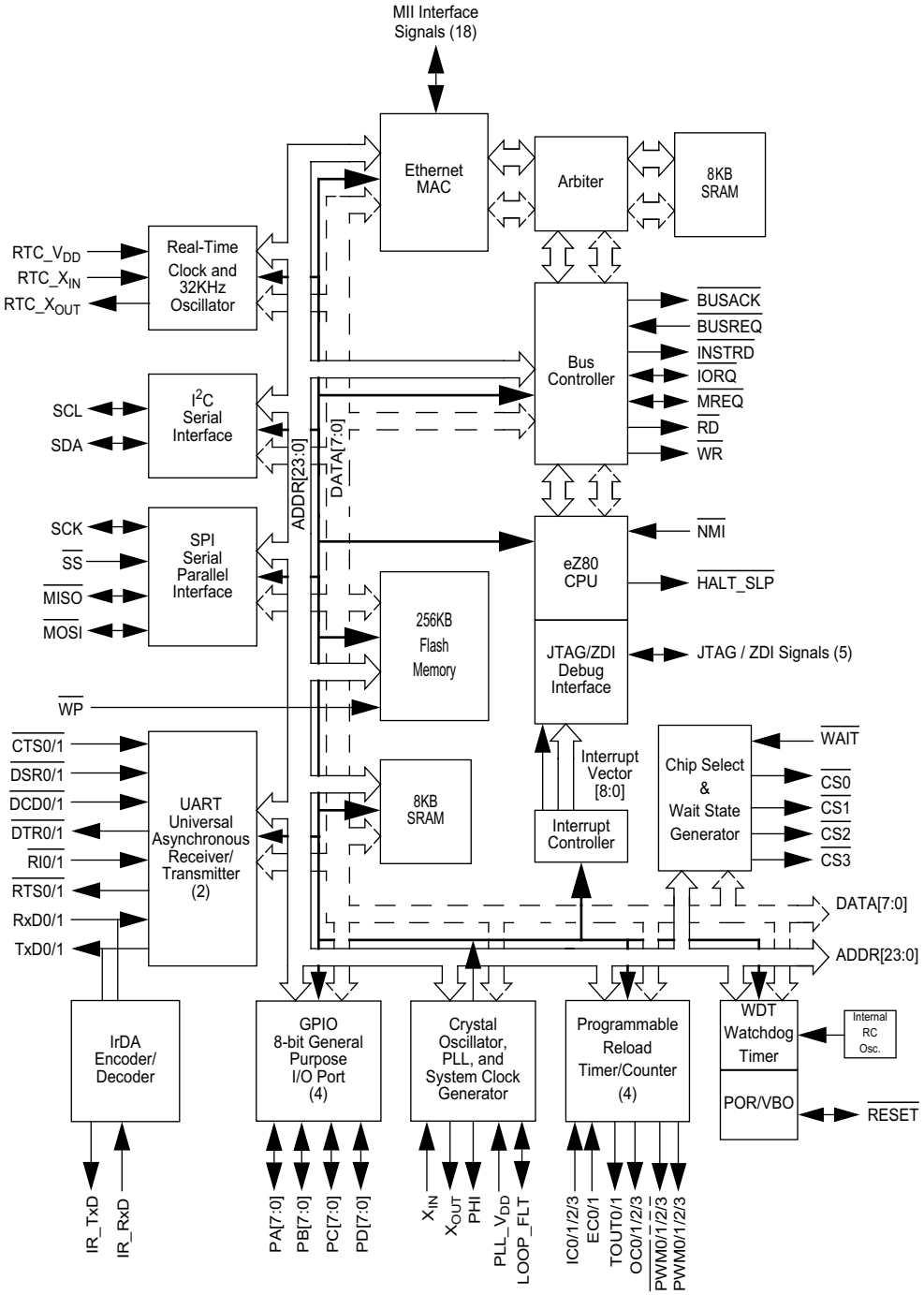


Figure 1. eZ80F91 Block Diagram

Pin Diagrams

144-Pin LQFP

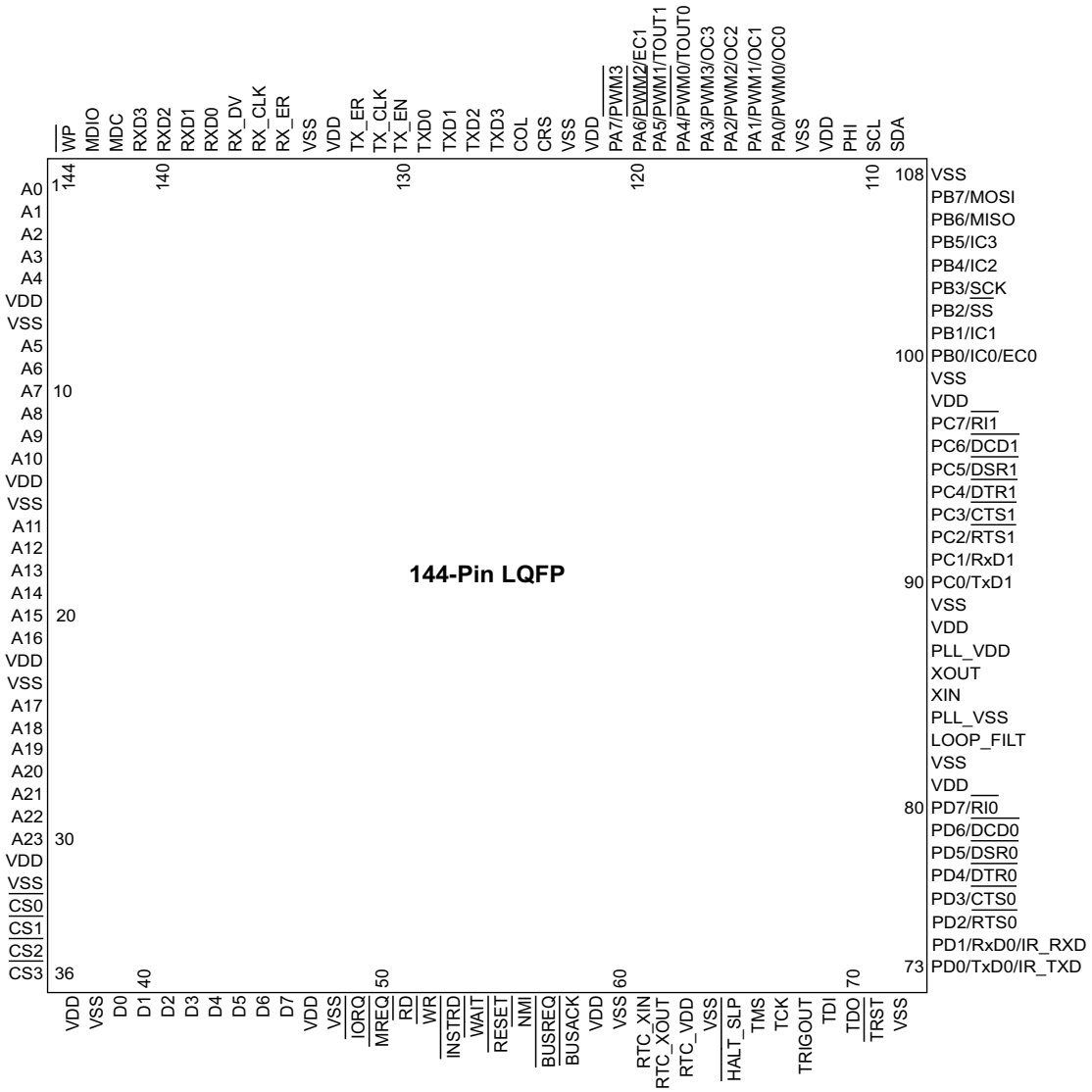


Figure 2. eZ80F91 144-Pin LQFP Pin Configuration

144-Pin BGA

Table 1. eZ80F91 144-Pin BGA Pin Configuration

	12	11	10	9	8	7	6	5	4	3	2	1
A	SDA	SCL	PA0	PA4	PA7	COL	TxD0	V_{DD}	Rx_DV	MDC	WPn	A0
B	V_{SS}	PHI	PA1	PA3	V_{DD}	TxD3	Tx_EN	V_{SS}	RxD1	MDIO	A2	A1
C	PB6	PB7	V_{DD}	PA5	V_{SS}	TxD2	Tx_CLK	Rx_ CLK	RxD3	A3	V_{SS}	V_{DD}
D	PB1	PB3	PB5	V_{SS}	CRS	TxD1	Rx_ER	RxD2	A4	A8	A6	A7
E	PC7	V_{DD}	PB0	PB4	PA2	Tx_ER	RxD0	A5	A11	V_{SS}	V_{DD}	A10
F	PC3	PC4	PC5	V_{SS}	PB2	PA6	A9	A17	A15	A14	A13	A12
G	V_{SS}	PC0	PC1	PC2	PC6	PLL_ V_{SS}	V_{SS}	A23	A20	V_{SS}	V_{DD}	A16
H	XOUT	XIN	PLL_ V_{DD}	V_{DD}	PD7	TMS	V_{SS}	D5	V_{SS}	A21	A19	A18
J	V_{SS}	V_{DD}	LOOP FILT_ OUT	PD4	TRIGOUT	RTC_ V_{DD}	NMIn	WRn	D2	CS0n	V_{DD}	A22
K	PD5	PD6	PD3	TDI	V_{SS}	V_{DD}	RESETn	RDn	V_{DD}	D1	CS2n	CS1n
L	PD1	PD2	TRSTn	TCK	RTC_ XOUT	BUSACKn	WAITn	MREQn	D6	D4	D0	CS3n
M	PD0	V_{SS}	TDO	HALT_ SLPn	RTC_ XIN	BUSREQn	INSTRDn	IORQn	D7	D3	V_{SS}	V_{DD}

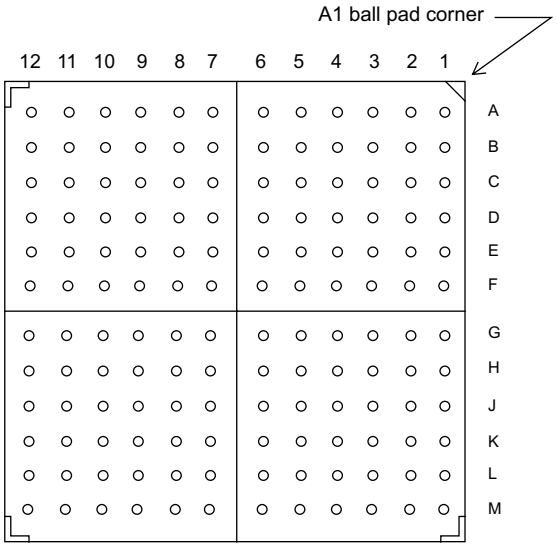


Figure 3. Bottom View of 144-Pin eZ80F91 BGA Device

Ordering Information

Part	PSI	Description
eZ80F91AZ050SC	50 MHz, Standard Temperature	eZ80F91 device, 144-LQFP
eZ80F91AZ050EC	50 MHz, Extended Temperature	eZ80F91 device, 144-LQFP
eZ80F91NA050SC	50 MHz, Standard Temperature	eZ80F91 device, 144-BGA
eZ80F91NA050EC	50 MHz, Extended Temperature	eZ80F91 device, 144-BGA
eZ80F910200ZCO	Development Kit, standard version	Complete eZ80F91 Development Kit

This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

ZiLOG Worldwide Headquarters
532 Race Street
San Jose, CA 95126
USA
Telephone: 408.558.8500
Fax: 408.558.8300
www.ZiLOG.com