PCA ELECTRONICS INC.

10 Base-T Multiport Module with Enhanced Common Mode Attenuation

EPE6117G

PRELIMINARY

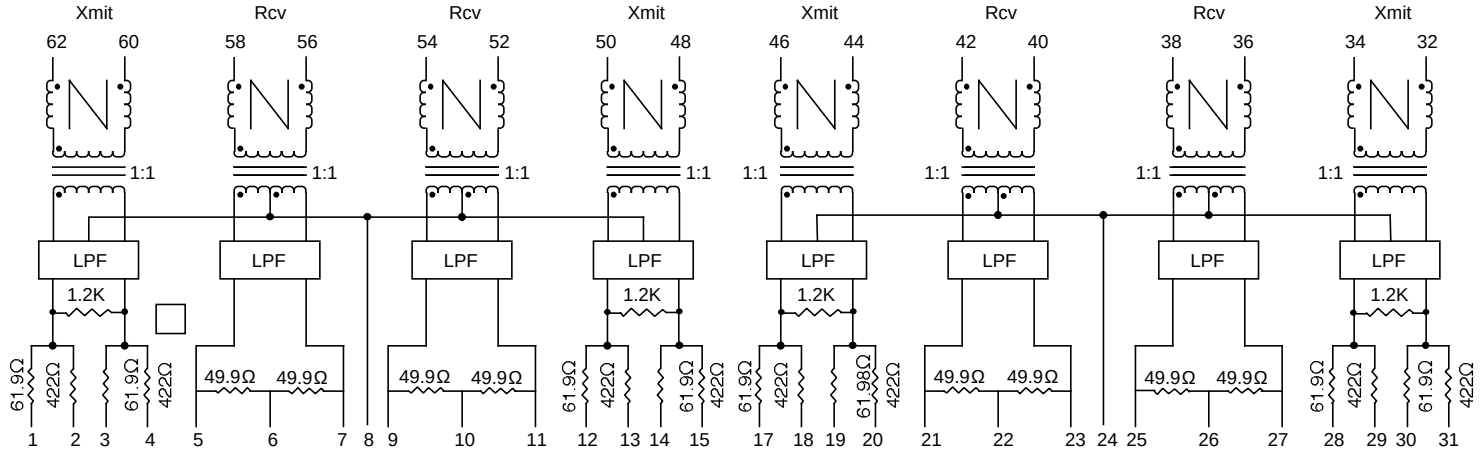
- Optimized for AMD Repeater Chips •
- Robust construction allows for severe solder processes •
- Low Crosstalk enhances network reliability •
- Complies with or exceeds IEEE 802.3, 10 Base-T Requirements •

Electrical Parameters @ 25° C

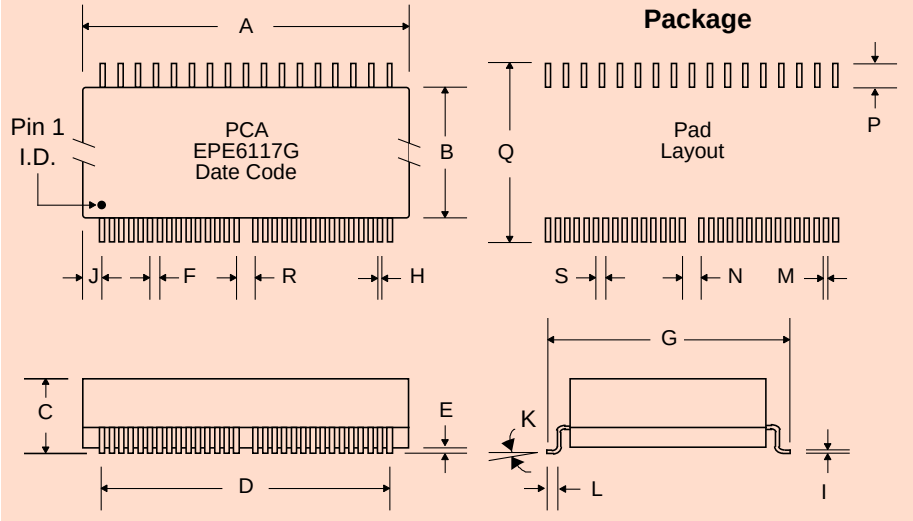
Cut-off Frequency (MHz)		Insertion Loss (dB Max.)		Return Loss (dB Min.)		Attenuation (dB Min.)								Common Mode Rejection (dB Min.)						Crosstalk (dB Min.)	
		1-10 MHz		5-10 MHz		@ 20 MHz		@ 25 MHz		@ 30 MHz		@ 40 MHz		@ 50 MHz		@ 100 MHz		@ 200 MHz		@ 1-10 MHz	
Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv
17	17	-1	-1	-15	-15	-7	-5	-18	-11	-30	-18	-35	-26	-30	-30	-30	-30	-----	-----	-35	-35

• **Isolation** : meets or exceeds 802.3 IEEE Requirements • **Characteristic Filter Impedance** : 100 Ω •

Schematic



Package



Dimensions

Dim.	(Inches) Min.	Max.		(Millimeters) Min.	Max.	
A	1.680	1.700		42.67	43.18	
B	1.015	1.025		25.78	26.04	
C	.380	.400		9.65	10.16	
D	1.49	1.51		37.85	38.35	
E	.003	.020		.076	.508	
F	.050	Typ.	34 Plcs	1.27	Typ.	34 Plcs
G	1.140	1.160		28.96	29.46	
H	.016	.022		.406	.559	
I	.008	.012		.203	.305	
J	.095	Typ.		2.41	Typ.	
K	0°	8°		0°	8°	
L	.025	.045		.635	1.14	
M			.030			.762
N			.100			2.54
P			.090			2.29
Q			1.240			31.50
R	.100	Typ.	16 Plcs	2.54	Typ.	16 Plcs
S			.050			1.27

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The circuit below is a guideline for interconnecting PCA's EPE6117G with AMD integrated repeater chips as a reference controller. Further details of system design, such as chip pin-out, etc. can be obtained from the specific chip manufacturer.

Typical insertion loss of the isolation transformer/filter is 0.7dB. This parameter covers the entire spectrum of the encoded signals in 10 Base-T protocols. However, the predistortion resistor network introduces some loss which has to be taken into account in determining how well your design meets the Standard Template requirements. Users are encouraged to verify that the resistor network suits their needs with the chip manufacturer before choosing their particular set of values. The Thevenin's effective termination is 2(61.9//422)///200 or approx. 100Ω. So, return loss is measured in bench by shorting all inputs on the xmit channel.

Note that some systems have auto polarity detection and some do not. If not, be certain to follow the proper polarity.

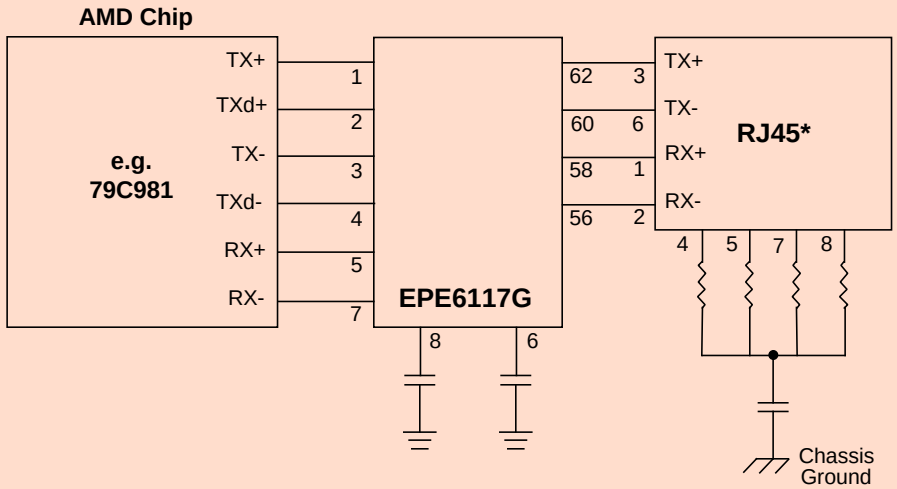
It is recommended that system designers ground the chip side center taps via a low voltage capacitor. Taking the cable side center taps to chassis via capacitors, is not recommended, as this will add cost without containing EMI. This may worsen EMI, specifically if the primary "common mode termination" is pulled to ground as shown.

The phantom resistors shown around the RJ45 connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.08 inches away from the chip side pins of EPE6117G. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP (Only one port shown)



Notes : * Pin-outs shown are for multiport, DCE configurations : e.g. Hubs, Repeaters

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