

Features

- Single power supply voltage of 2.7V to 3.6V
- Power down features using CE1# and CE2
- Low operating current : 25mA(max. for 70 ns)
- Maximum Standby current : 10 μ A at 3.6 V
- Data retention supply voltage: 1.5V to 3.6V
- Direct TTL compatibility for all input and output
- Wide operating temperature range: -40°C to 85°C
- Package type: 36-ball TFBGA, 6x8mm

asserted low. There are three control inputs. CE1# and CE2 are used to select the device and for data retention control, and output enable (OE#) provides fast memory access. Data byte control pin (LB#,UB#) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range from -40°C to 85°C, the EM562081 can be used in environments exhibiting extreme temperature conditions.

Ordering Information

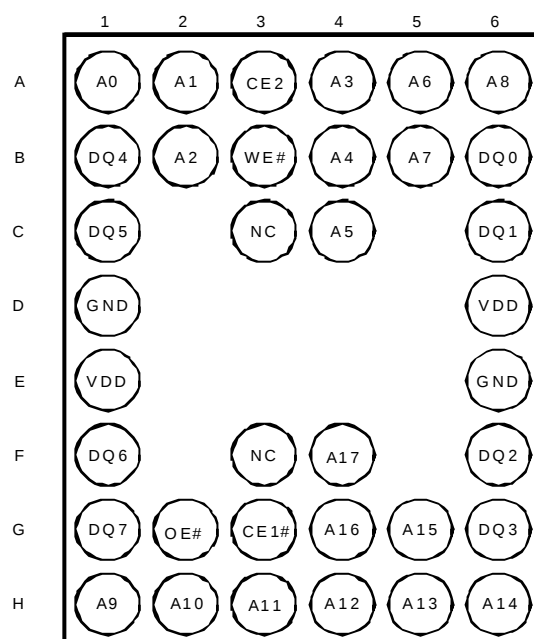
Part Number	Speed	IDDs2	Package
EM562081BC-70	70 ns	10 μ A	6x8 BGA
EM562081BC-85	85 ns	10 μ A	6x8 BGA

Pin Names

Symbol	Function
A0 - A17	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
CE1#,CE2	Chip Enable Inputs
OE#	Output Enable
WE#	Read/Write Control Input
GND	Ground
VDD	Power Supply
NC	No Connection

Pin Assignment

1. 36-Ball BGA (CSP), Top View



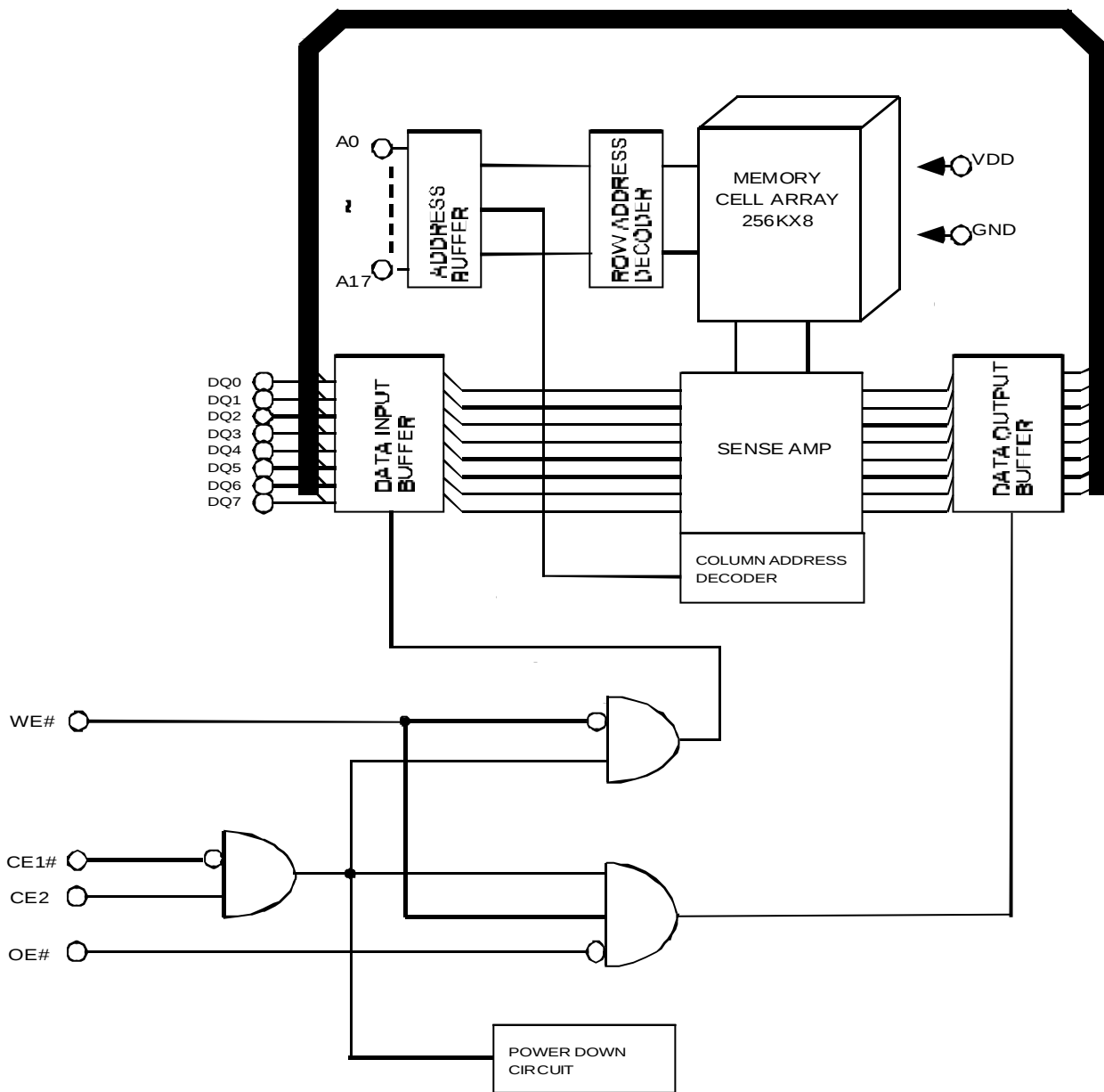
Overview

The EM562081 is a 2,097,152-bit SRAM organized as 262,144 words by 8 bits. It is designed with advanced CMOS technology. This Device operates from a single 2.7V to 3.6V power supply. Advanced circuit technology provides both high speed and low power. It is automatically placed in low-power mode when chip enable (CE1#) is asserted high or (CE2) is

Etron Technology, Inc.

No. 6, Technology Rd. V, Science-Based Industrial Park, Hsinchu, Taiwan 30077, R.O.C
TEL: (886)-3-5782345 FAX: (886)-3-5778671

Block Diagram



Operating Mode

Mode	CE1#	CE2	OE#	WE#	DQ0~DQ7	Power
Read	L	H	L	H	D _{OUT}	Active
Write	L	H	X	L	D _{IN}	Active
Output Deselect	L	H	H	H	High-Z	Active
Standby	H	X	X	X	High-Z	Standby
	X	L	X	X	High-Z	Standby

Note: X = don't care. H = logic high. L = logic low.

Absolute Maximum Ratings

Supply voltage, V _{DD}	-0.3 to +4.6V
Input voltages, V _{IN}	-0.3 to +4.6V
Input and output voltages, V _{I/O}	-0.5 to V _{DD} + 0.5V
Operating temperature, T _{OPR}	-40 to +85°C
Storage temperature, T _{STRG}	-55 to +150°C
Soldering Temperature (10s), T _{SOLDER}	240°C
Power dissipation, P _D	0.6 W

DC Recommended Operating Conditions (Ta=-40° C to 85° C)

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD}	Power Supply Voltage	2.7	–	3.6	V
V _{IH}	Input High Voltage	2.2	–	V _{DD} + 0.3 ⁽¹⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽²⁾	–	0.6	V
V _{DR}	Data Retention Supply Voltage	1.5	–	3.6	V

Note:

(1) Overshoot : V_{DD} +2.0V in case of pulse width ≤ 20ns

(2) Undershoot : -2.0V in case of pulse width ≤ 20ns

DC Characteristics (Ta = -40° C to 85° C, V_{DD} = 2.7V to 3.6V)

Parameter	Symbol	Test Conditions		Min	Typ*	Max	Unit
Input low current	I _{IL}	I _{IN} = 0V to V _{DD}		- 1	–	1	μA
Output low voltage	V _{OL}	I _{OL} = 2.1 mA		-	–	0.4	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA		2.2	–	–	V
Operating current	I _{DD1}	V _{DD} = 3.6 V , CE1# = V _{IL} and CE2 = V _{IH} and I _{OUT} = 0mA Other Input = V _{IH} / V _{IL}	Cycle time = min	–	10	25	mA
	I _{DD2}		Cycle time = 1μs	–	–	5	
Standby current	I _{DDS1}	CE1# = V _{IH} or CE2 = V _{IL}		–	–	0.5	mA
	I _{DDS2**} (Note)	CE1# ≥ V _{DD} - 0.2V or CE2 ≤ 0.2V ,		–	1	10	μA

Notes:

* Typical value are measured at Ta = 25°C, and not 100% tested.

** In standby mode with CE1# ≥ V_{DD} - 0.2V, these limits are assured for the condition CE2 ≥ V_{DD} - 0.2V or CE2 ≤ 0.2V.

Capacitance (Ta = 25° C; f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C _{IN}	–	–	10	pF	V _{IN} = GND
Output capacitance	C _{OUT}	–	–	10	pF	V _{OUT} = GND

Notes: This parameter is periodically sampled and is not 100% tested.

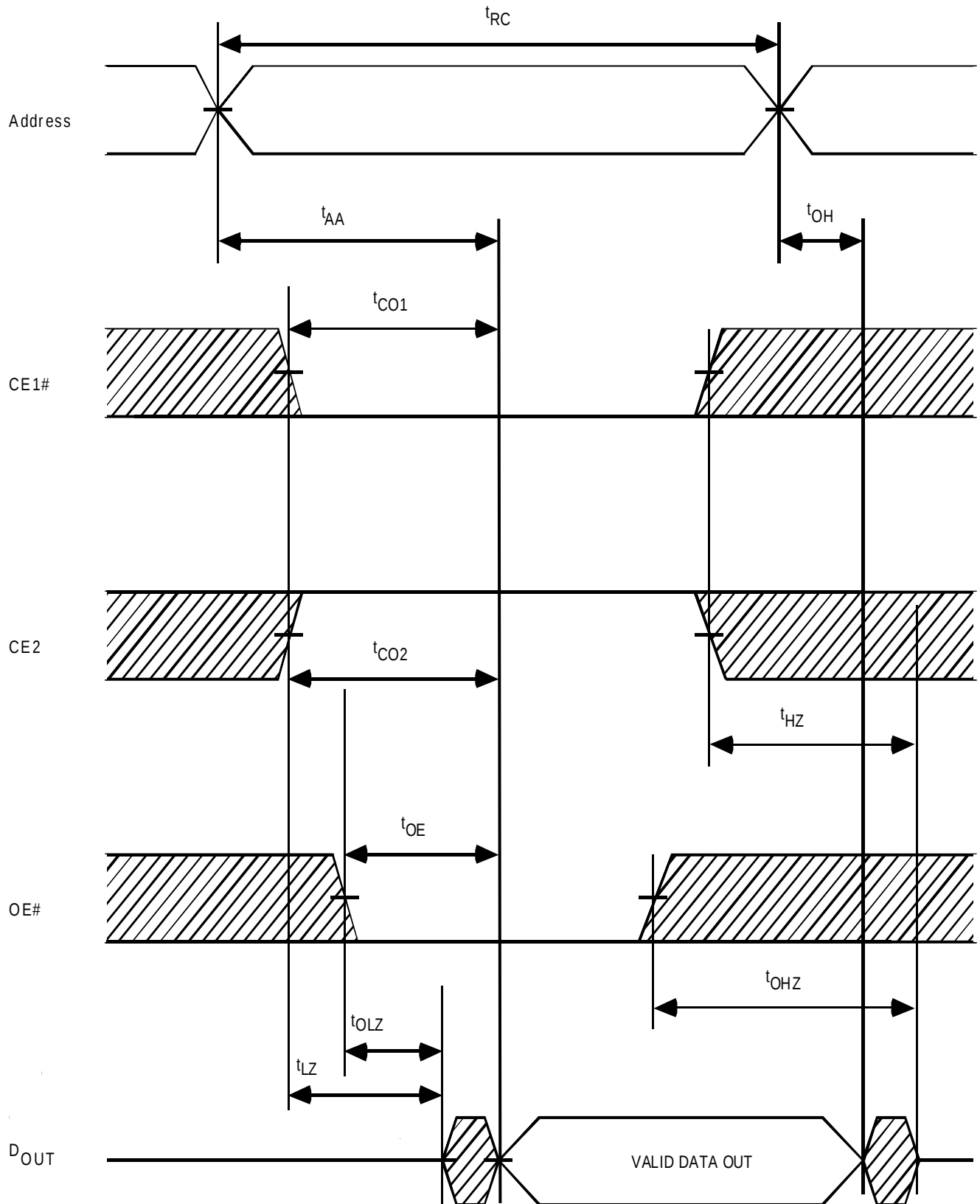
AC Characteristics and Operating Conditions (Ta = -40° C to 85° C, VDD = 2.7V to 3.6V)

Read Cycle						
Symbol	Parameter	EM562081				Unit
		-85		-70		
		Min	Max	Min	Max	
t _{RC}	Read cycle time	85	–	70	–	ns
t _{AA}	Address access time	–	85	–	70	
t _{CO1}	Chip Enable (CE1#) Access Time	–	85	–	70	
t _{CO2}	Chip Enable (CE2) Access Time	–	85	–	70	
t _{OE}	Output enable access time	–	45	–	35	
t _{LZ}	Chip Enable Low to Output in Low-Z	10	–	10	–	
t _{OLZ}	Output enable Low to Output in Low-Z	3	–	3	–	
t _{HZ}	Chip Enable High to Output in High-Z	–	35	–	25	
t _{OHZ}	Output Enable High to Output in High-Z	–	35	–	25	
t _{OH}	Output Data Hold Time	10	–	10	–	
Write Cycle						
Symbol	Parameter	EM562081				Unit
		-85		-70		
		Min	Max	Min	Max	
t _{WC}	Write cycle time	85	–	70	–	ns
t _{WP}	Write pulse width	55	–	55	–	
t _{CW}	Chip Enable to end of write	70	–	60	–	
t _{AS}	Address setup time	0	–	0	–	
t _{WR}	Write Recovery time	0	–	0	–	
t _{WHZ}	WE# Low to Output in High-Z	–	35	–	30	
t _{OW}	WE# High to Output in Low-Z	5	–	5	–	
t _{DS}	Data Setup Time	35	–	30	–	
t _{DH}	Data Hold Time	0	–	0	–	

AC Test Condition

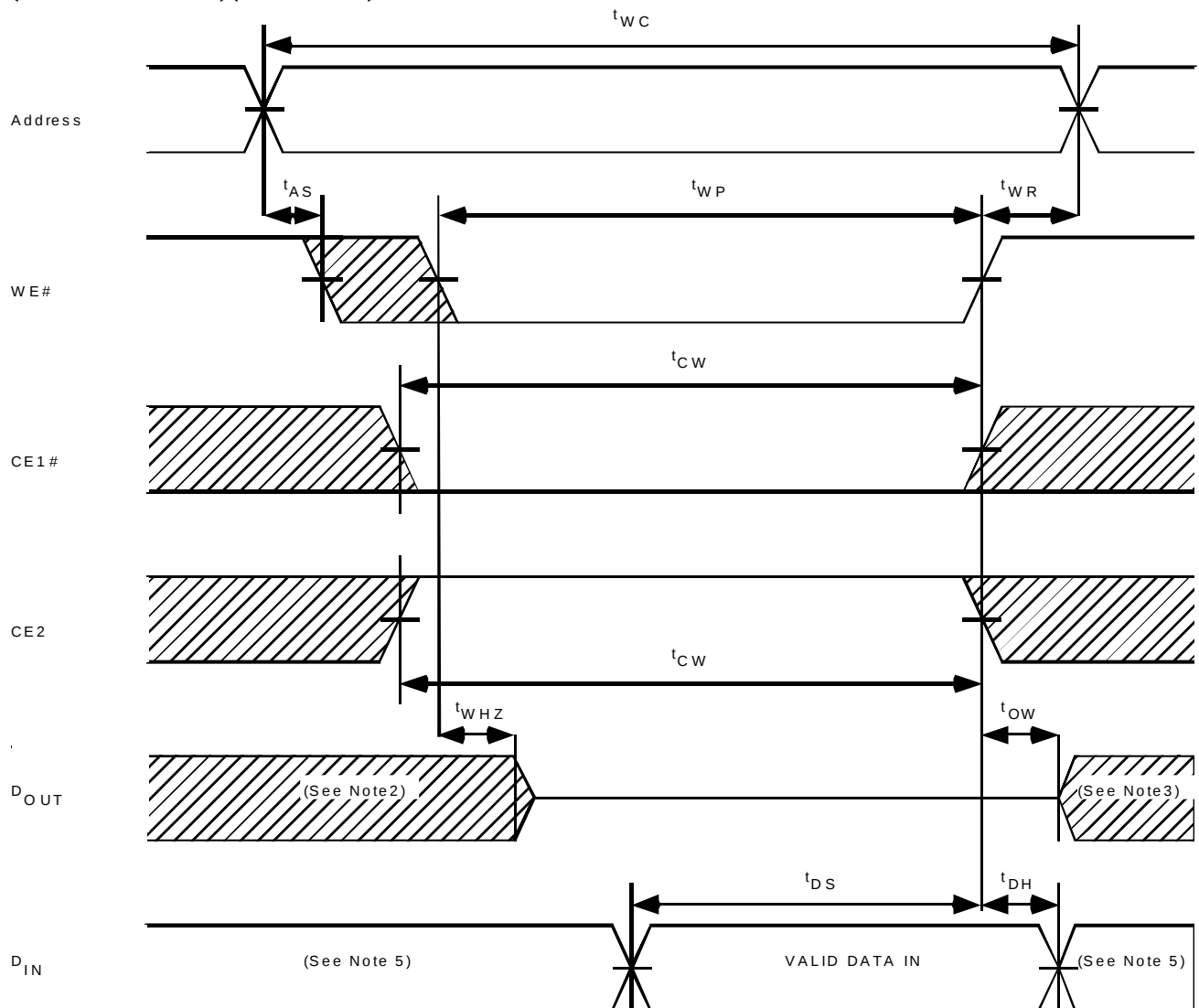
- Output load: 50pF + one TTL gate
- Input pulse level: 0.4V, 2.4V
- Timing measurements: 0.5 x VDD
- tR, tF: 5ns

Read Cycle (See Note 1)



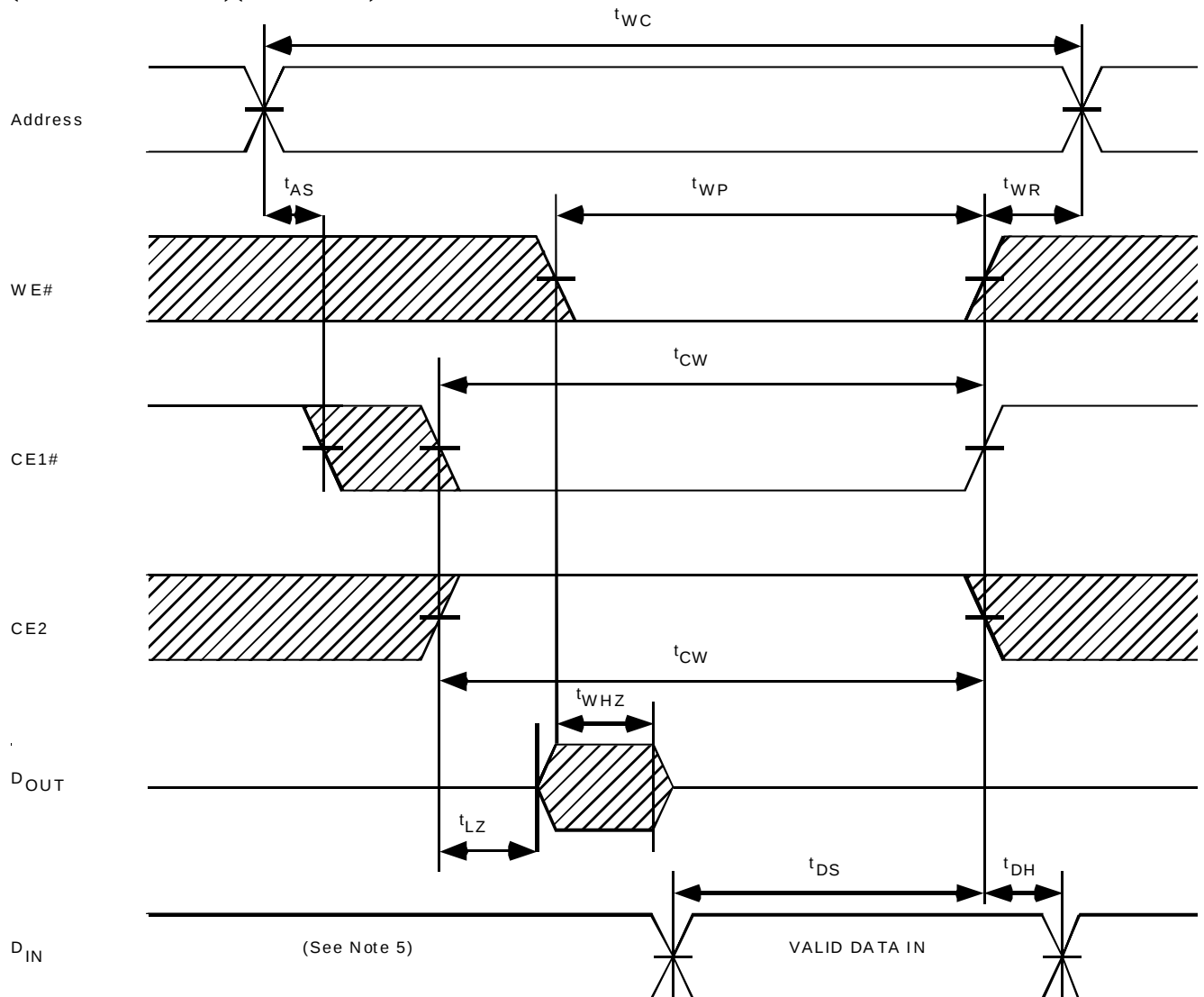
Write Cycle1

(WE# Controlled)(See Note 4)

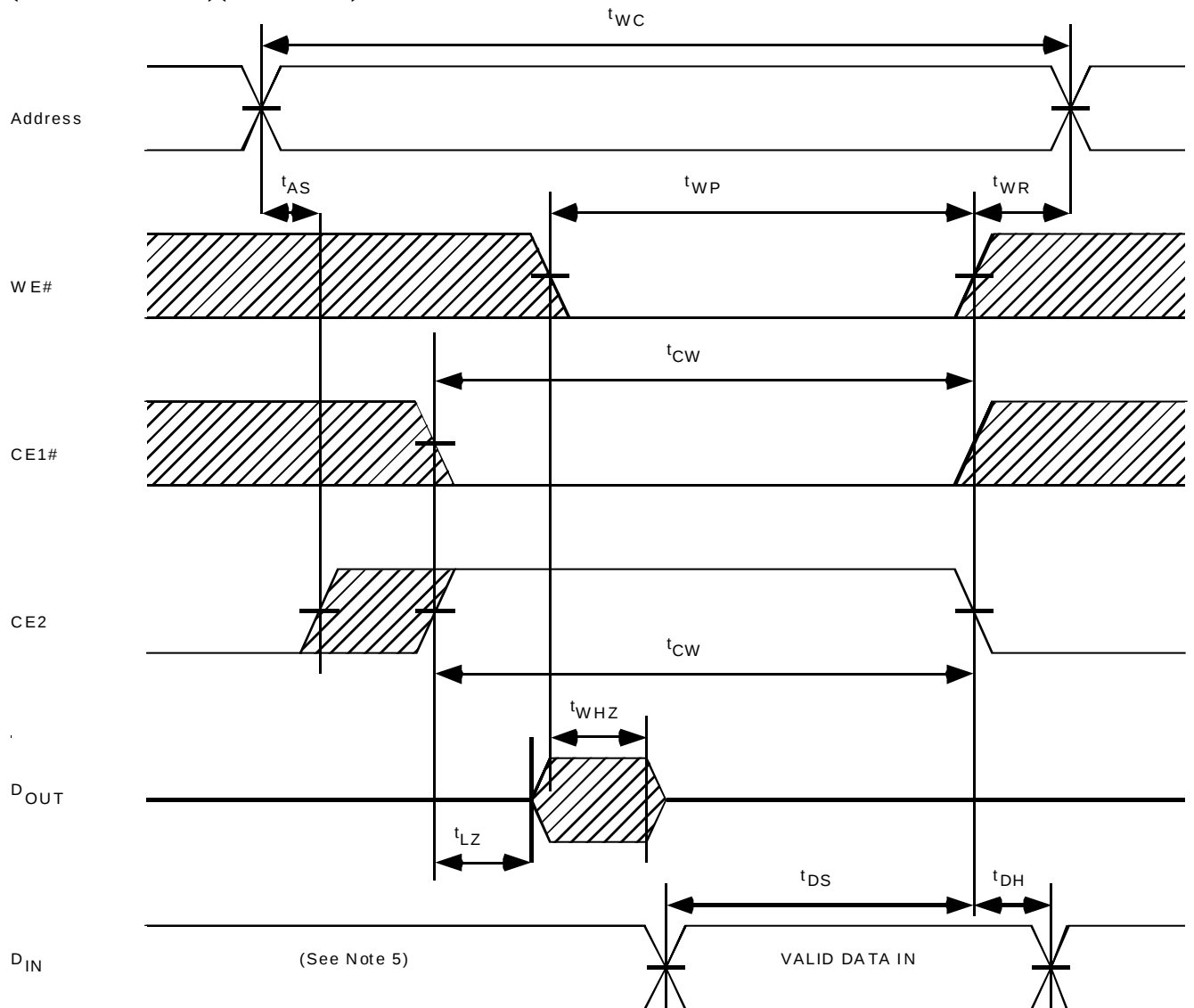


Write Cycle 2

(CE1# Controlled)(See Note 4)

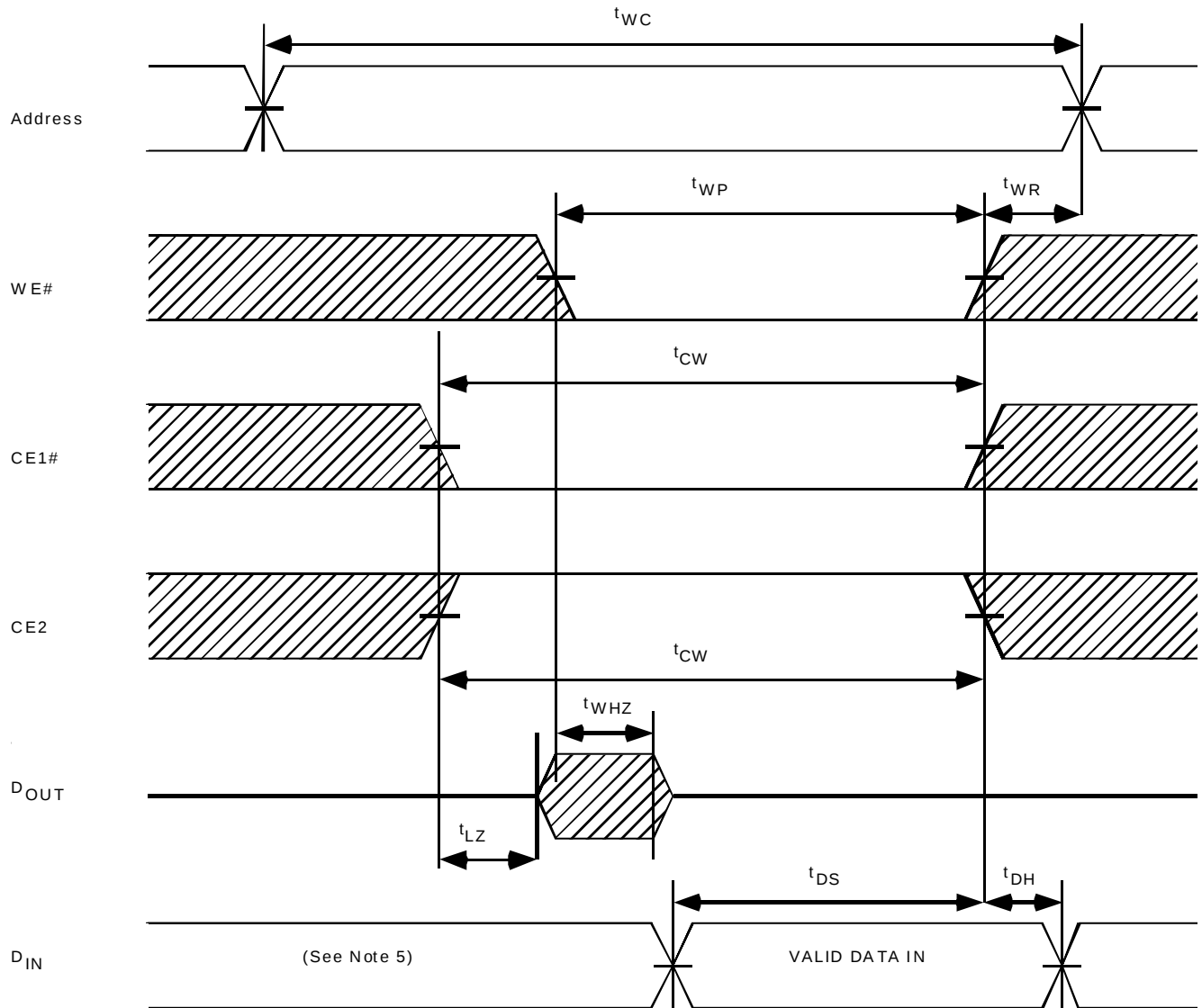


Write Cycle 3 (CE2 Controlled)(See Note 4)



Write Cycle4

(UB#, LB# Controlled)(See Note 4)



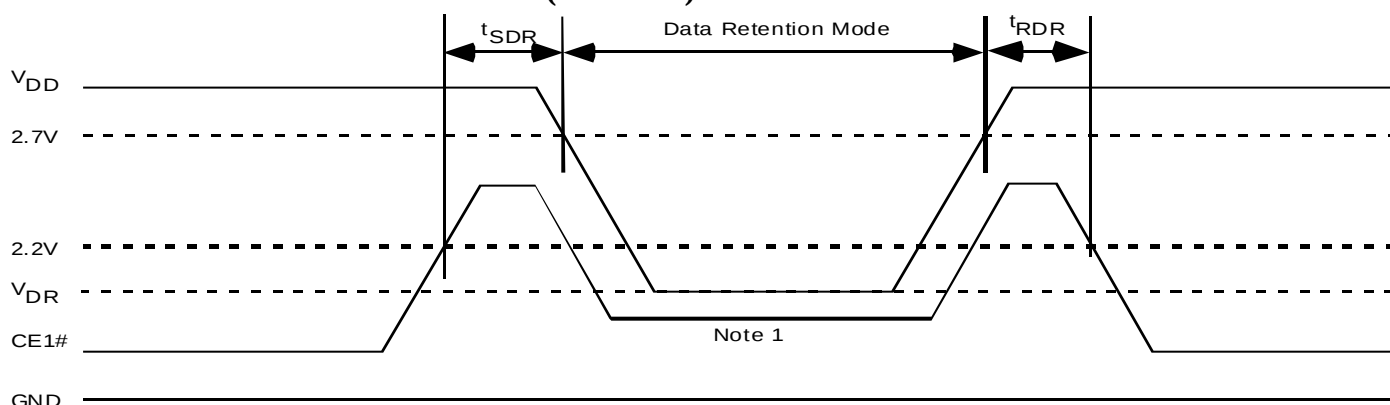
Note:

- (1) WE# remains HIGH for the read cycle.
- (2) If CE1# goes LOW (or CE2 goes HIGH) with or after WE# goes LOW, the outputs will remain at high impedance.
- (3) If CE1# goes HIGH (or CE2 goes LOW) coincident with or before WE# goes HIGH, the outputs will remain at high impedance.
- (4) If OE# is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

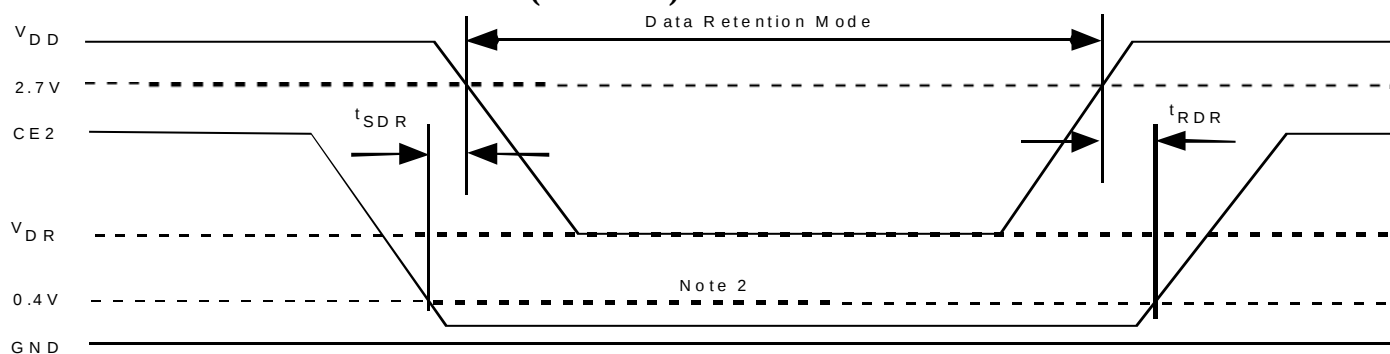
Data Retention Characteristics (Ta = -40° C to 85° C)

Symbol	Parameter		Min	Typ	Max	Unit
V_{DR}	Data Retention Supply Voltage	$CE1\# \geq V_{DD} - 0.2V$, $CE2 \leq 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$	1.5	–	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.5V$, $CE1\# \geq V_{DD} - 0.2V$, $CE2 \leq 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$	–	0.5	3	μA
t_{SDR}	Chip Deselect to Data Retention Mode Time		0	–	–	ns
t_{RDR}	Recovery Time		t_{RC}	–	–	ns

CE1# Controlled Data Retention Mode (see Note1)



CE2 Controlled Data Retention Mode (see Note2)



Note:

- (1) If $CE1\#$ controlled data retention mode, minimum standby current mode is entered when $CE2 \leq 0.2V$ or $CE2 \geq V_{DD} - 0.2V$.
- (2) In $CE2$ controlled data retention mode, minimum standby current mode is entered when $CE2 \leq 0.2V$.

BGA (CSP) Package Diagrams

36-Ball (6.00mm x 8.00mm) BGA (CSP)

Units in mm

TOP VIEW

BOTTOM VIEW

