4M x 32 Low Power SDRAM

Advance 07/2002

Features

- Fast clock rate : 133/100 MHz
- Fully synchronous operation
- Internal pipelined architecture
- Four internal banks (1M x 32bit x 4bank)
- Programmable Mode
  -CAS# Latency : 1, 2 & 3
  -Burst Length : 1,2,4,8, & full page
  -Burst Type : Sequential & Interleave
- Burst-Read-Single-Write
- Burst stop function
- Individual byte controlled by DQM0-3
- Auto Refresh and Self Refresh
- 4096 refresh cycles / 64ms
- 2.5V power supply
- Interface : LVTTL
- Package : 90 ball-FBGA, 11x13mm

Pin Assignment : Top View

	1	2	3	4	5	6	7	8	9
A	DQ26	DQ24	VSS				VDD	DQ23	DQ21
B	DQ28	VDDQ	VSSQ				VDDQ	VSSQ	DQ19
C	VSSQ	DQ27	DQ25				DQ22	DQ20	VDDQ
D	VSSQ	DQ29	DQ30				DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC				NC	DQ16	VSSQ
F	Vss	DQM3	A3				A2	DQM2	VDD
G	A4	A5	A6				A10	A0	A1
H	A7	A8	NC				NC	BA1	A11
J	CLK	CKE	A9				BA0	CS#	RAS#
K	DQM1	NC	NC				CAS#	WE#	DQM0
L	VDDQ	DQ8	VSS				VDD	DQ7	VSSQ
M	VSSQ	DQ10	DQ9				DQ6	DQ5	VDDQ
N	VSSQ	DQ12	DQ14				DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VSSQ				VDDQ	VSSQ	DQ4
R	DQ13	DQ15	VSS				VDD	DQ0	DQ2

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Pin Descriptions

Table 1. Pin Details of 4Mx32 LPSDRAM

Symbol	Type	Description
CLK	Input	**Clock:** CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	**Clock Enable:** CKE activates(HIGH) and deactivates(LOW) the CLK signal. If CKE goes low synchronously with clock(set-up and hold time same as other inputs), the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes. CKE is synchronous except after the device enters Power Down and Self Refresh modes, where CKE becomes asynchronous until exiting the same mode. The input buffers, including CLK, are disabled during Power Down and Self Refresh modes, providing low standby power.
BA0, BA1	Input	**Bank Select:** BA0 and BA1 defines to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied. BS is also used to program the 11th bit of the Mode and Special Mode registers.
A0-A11	Input	**Address Inputs:** A0-A10 are sampled during the BankActivate command (row address A0-A10) and Read/Write command (column address A0-A7 with A10 defining Auto Precharge) to select one location out of the 256K available in the respective bank. During a Precharge command, A10 is sampled to determine if all banks are to be precharged (A10 = HIGH). The address inputs also provide the op-code during a Mode Register Set or Special Mode Register Set command.
CS#	Input	**Chip Select:** CS# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CS# is sampled HIGH. CS# provides for external bank selection on systems with multiple banks. It is considered part of the command code.
RAS#	Input	**Row Address Strobe:** The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CLK. When RAS# and CS# are asserted "LOW" and CAS# is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the WE# signal. When the WE# is asserted "HIGH," the BankActivate command is selected and the bank designated by BS is turned on to the active state. When the WE# is asserted "LOW," the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.
CAS#	Input	**Column Address Strobe:** The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CLK. When RAS# is held "HIGH" and CS# is asserted "LOW," the column access is started by asserting CAS# "LOW." Then, the Read or Write command is selected by asserting WE# "LOW" or "HIGH."
WE#	Input	**Write Enable:** The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the positive edges of CLK. The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
DQM0 - DQM3	Input	**Data Input/Output Mask: Data Input Mask:** DM0-DM3 are byte specific. Input data is masked when DM is sampled HIGH during a write cycle. DM3 masks DQ31-DQ24, DM2 masks DQ23-DQ16, DM1 masks DQ15-DQ8, and DM0 masks DQ7-DQ0.
DQ0-DQ31	Input/ Output	**Data I/O:** The DQ0-31 input and output data are synchronized with the positive edges of CLK. The I/Os are byte-maskable during Reads and Writes.
NC	-	**No Connect:** These pins should be left unconnected.
V_{DDQ}	Supply	**DQ Power:** Provide isolated power to DQs for improved noise immunity.

V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity.
V_{DD}	Supply	**Power Supply:** +2.5V±0.2V
V_{SS}	Supply	**Ground**

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 2 shows the truth table for the operation commands.

Table 2. Truth Table (Note (1) , (2))

Command	State	CKE_{n-1}	CKE_n	DQM(6)	BA0,1	A10	A11, A9-0	CS#	RAS#	CAS#	WE#
Bank Activate	Idle(3)	H	X	X	V	Row address		L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	X	V	L	Column address (A0 ~ A7)	L	H	L	L
Write and Auto Precharge	Active(3)	H	X	X	V	H		L	H	L	L
Read	Active(3)	H	X	X	V	L	Column address (A0 ~ A7)	L	H	L	H
Read and Auto precharge	Active(3)	H	X	X	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	OP code			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Any(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

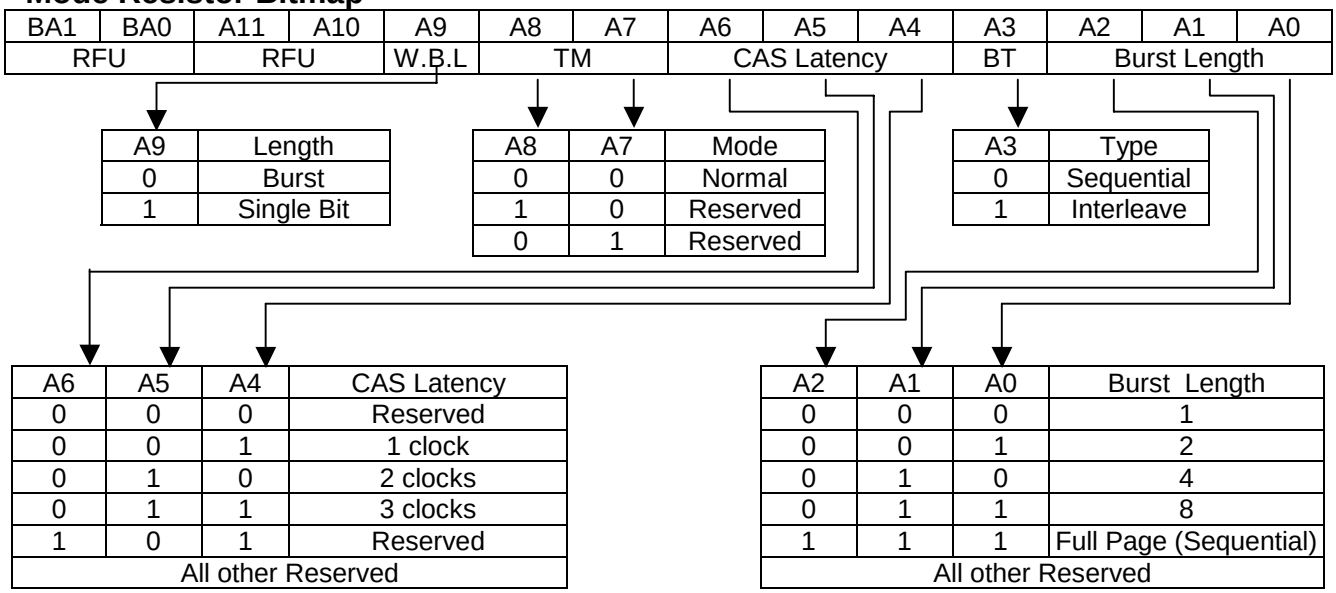
Note: 1. V = Valid, X = Don't care, L = Logic low, H = Logic high
2. CKE_n signal is input level when commands are provided.
CKE_{n-1} signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BA signal.
4. Device state is 1, 2, 4, 8, and full page burst operation.
5. Power Down Mode can not enter in the burst operation.
When this command is asserted in the burst cycle, device state is clock suspend mode.
6. DQM0-3

Mode Register Set (MRS)

The mode register is divided into various fields depending on functionality.

- Burst Length Field (A2, A1, A0) :This field specifies the data length of column access and selects the Burst Length.
- Addressing Mode Select Field (A3) : The Addressing Mode can be Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 1, 2, 4 and 8. Full page burst length is only for Sequential mode.
- CAS# Latency Field (A6, A5, A4) : This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS# Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field. $t_{CAC}(min) \leqq$ CAS# Latency X t_{CK}
- Test Mode Field (A7, A8) : These two bits must be programmed to "00" in normal operation.
- W.B.L : Write Burst Length Field (A9) : This bit is used to select the burst write length.

Mode Resistor Bitmap



A9	Length
0	Burst
1	Single Bit

A8	A7	Mode
0	0	Normal
1	0	Reserved
0	1	Reserved

A3	Type
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1 clock
0	1	0	2 clocks
0	1	1	3 clocks
1	0	1	Reserved
All other Reserved			

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	1	1	Full Page (Sequential)
All other Reserved			

Burst Definition, Addressing Sequence of Sequential and Interleave Mode

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
2	X	X	0	0, 1	0, 1
	X	X	1	1, 0	1, 0
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Absolute Maximum Rating

Symbol	Item	Rating	Unit	Note
V_{IN}, V_{OUT}	Input, Output Voltage	- 1.0 ~ +4.6	V	
V_{DD}, V_{DDQ}	Power Supply Voltage	-1.0 ~ +4.6	V	
T_{OPR}	Operating Temperature	-25 ~ +85	°C	
T_{STG}	Storage Temperature	- 55~ +150	°C	
T_{SOLDER}	Soldering Temperature (10s)	240	°C	
P_D	Power Dissipation	1.0	W	
I_{OUT}	Short Circuit Output Current	50	mA	

Recommended DC Operating Conditions

All units are in Volts

Parameter/ Condition	Symbol	Min	Typ	Max	Notes
DRAM Core Supply VOLTAGE	V_{DD}	2.3	2.5	2.7	
I/O Supply Voltage	V_{DDQ}	2.3	2.5	2.7	
Input High (Logic 1) Voltage	V_{IH}	0.9 x V_{DDQ}	2.5	V_{DDQ}+0.3	
Input Low (Logic 0) Voltage	V_{IL}	-0.3	0	0.3	
Data Output High (Logic 1) Voltage	V_{OH}	0.95 x V_{DDQ}	-	-	1
Data Output High (Logic 1) Voltage	V_{OL}	-	-	0.2	2

Notes 1 : for I_{OUT} = - 2.0mA

Notes 2 : for I_{OUT} = + 2.0mA

Capacitance (V_{DD} = 2.5V, f = 1MHz, Ta = 25°C)

Symbol	Parameter	Min.	Max.	Unit
C_I	Input Capacitance	4	5	pF
$C_{I/O}$	Input/Output Capacitance	6	8	pF

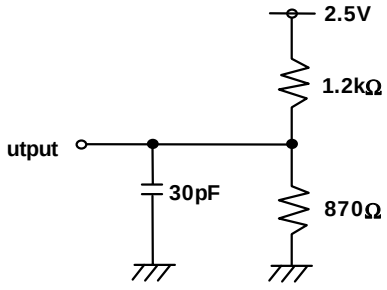
Note: These parameters are periodically sampled and are not 100% tested.

DC Characteristics (Ta = -25~85°C)

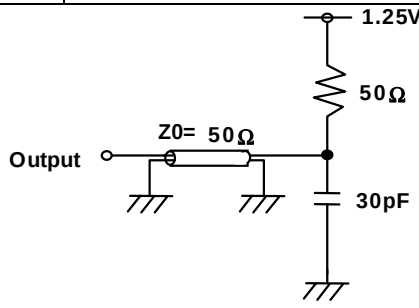
Description/Test condition		Symbol	- 75/1H/1L Max.	Unit	Note
Operating Current $t_{RC} \geq t_{RC}$(min), Outputs Open, Input signal one transition per one cycle	1 bank operation	I_{CC1}	150/140/130	mA	
Precharge Standby Current in power down mode t_{CK} = 15ns, CKE ≤ V_{IL}(max)		I_{CC2P}	2		
Precharge Standby Current in power down mode t_{CK} = ∞, CKE ≤ V_{IL}(max)		I_{CC2PS}	2		
Precharge Standby Current in non-power down mode t_{CK} = 15ns, CS# ≥ V_{IH}(min), CKE ≥ V_{IH} Input signals are changed once during 30ns.		I_{CC2N}	30		
Precharge Standby Current in non-power down mode t_{CK} = ∞, CLK ≤ V_{IL}(max), CKE ≥ V_{IH}		I_{CC2NS}	12		
Active Standby Current in power down mode CKE ≤ V_{IL}(max), t_{CK} = 15ns		I_{CC3P}	6		
Active Standby Current in power down mode CKE & CLK ≤ V_{IL}(max), t_{CK} = ∞		I_{CC3PS}	6		
Active Standby Current in non-power down mode CKE ≥ V_{IH}(min), CS# ≥ V_{IH}(min), t_{CK} = 15ns		I_{CC3N}	60		
Active Standby Current in non-power down mode CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CK} = ∞		I_{CC3NS}	50		
Operating Current (Burst mode) t_{CK} = t_{CK}(min), Outputs Open, Multi-bank interleave		I_{CC4}	220/180/170		
Refresh Current $t_{RC} \geq T_{RC}$(min)		I_{CC5}	250/220/210		
Self Refresh Current CKE ≤ 0.2V		I_{CC6}	800	uA	

LVTTL Interface

Reference Level of Output Signals	0.5 x V_{DDQ}
Output Load	Reference to the Under Output Load (B)
AC Input Signal Levels(Vih/Vil)	2.3V / 0.2V
Transition Time (Rise and Fall) of Input Signals	1ns
Reference Level of Input Signals	0.5 x V_{DDQ}



LVTTL D.C. Test Load (A)



LVTTL A.C. Test Load (B)

A.C Electrical Characteristics Conditions

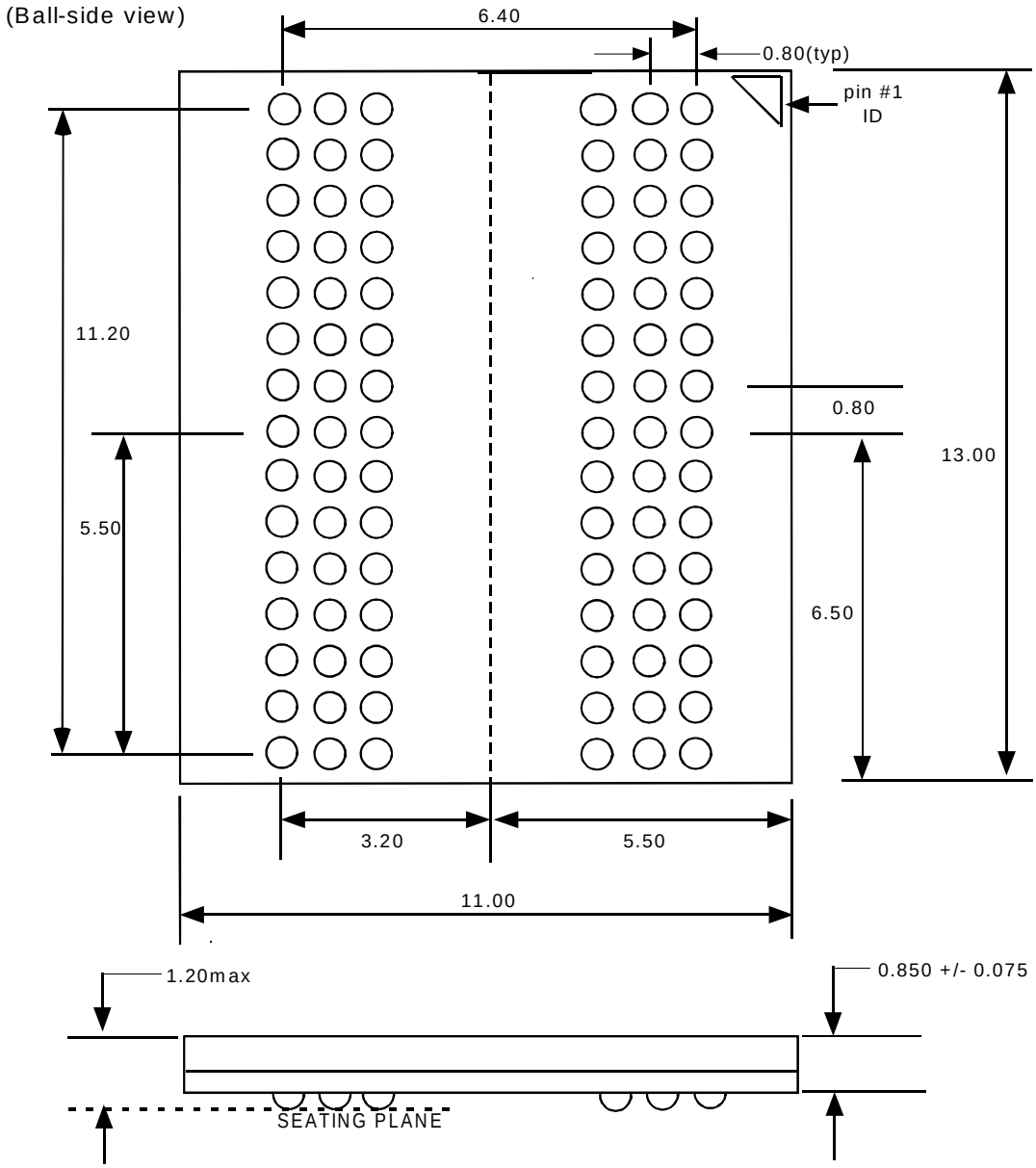
(V_{DD} = 2.3V ~ 2.5V, Ta = -25 ~ 85°C) (Note : 5,6,7,8)

Symbol	A.C. Parameter		- 75/1H/1L		Unit	Note
			Min.	Max.		
t_{RC}	Row cycle time(same bank)		65/70/84		ns	9
t_{RCD}	RAS# to CAS# delay (same bank)		20/20/24			9
t_{RP}	Precharge to refresh / row activate command (same bank)		20/20/24			9
t_{RRD}	Row activate to row active delay (different banks)		15/20/20			9
t_{RAS}	Row activate to percharge time (same bank)		45/50/60	100,000		
t_{RDL}	Last data in to row precharge		10		ns	
t_{CK1}	Clock cycle time	CL* = 1	- /- /25		ns	
t_{CK2}		CL* = 2	10/10/12			
t_{CK3}		CL* = 3	7.5/10/10			
t_{CH}	Clock high time		2.5/3/3			
t_{CL}	Clock low time		2.5/3/3			
t_{AC1}	Access time from CLk (positive edge)	CL* = 1		- / -/18		
t_{AC2}		CL* = 2		6/6/6		
t_{AC3}		CL* = 3		5.5/6/6		
t_{CCD}	CAS# to CAS# Delay time		1		CLK	
t_{OH}	Data output hold time		2		ns	
t_{LZ}	Data output low impedance		1			
t_{HZ1}	Data output high impedance	CL* = 1		-/-/18		
t_{HZ2}		CL* = 2		6/6/6		
t_{HZ3}		CL* = 3		5.5/6/6		
T_{IS}	Data/Address/Control Input set-up time		2.5/3/3			
t_{IH}	Data/Address/Control Input hold time		1.5		ns	

* CL is CAS# Latency.

Features of the Low-Power SDRAM Package:

- 90-FBGA, 11mm x 13mm plastic package
- 9x15 ball array with 3 depopulated rows in center
- 0.8mm ball pitch
- Low-profile, 1.2mm max height



All dimensionns are in mm.