Edge628
Very High-Speed Dual- and Quad-Channel ECL Delay Lines

SEMTECH

HIGH-PERFORMANCE PRODUCTS – ATE

Description

The Edge628 is a quad delay and deskew element. Manufactured in a high performance bipolar process, it is designed primarily for channel deskew applications in Memory Test Equipment.

The part offers a full scale delay range of 6.6 ns with independent 1.5 ns adjustment of the falling edge.

The Edge628 has a drive mode, where one input signal is routed to all of the outputs. This mode is particularly useful in a fanout application.

The delay value (and resolution) is controlled via an external voltage DAC.

This deskew element is designed specifically to be monotonic and stable while delaying a very narrow pulse over a wide delay range.

The Edge628 is a pin and functionally compatible upgrade to the Edge624 with the following differences:

- modes 0 and 2 only
- 6.6 ns typical delay range
- 1.5 ns trailing edge adjust
- higher performance
- lower power
- smaller package (optional).

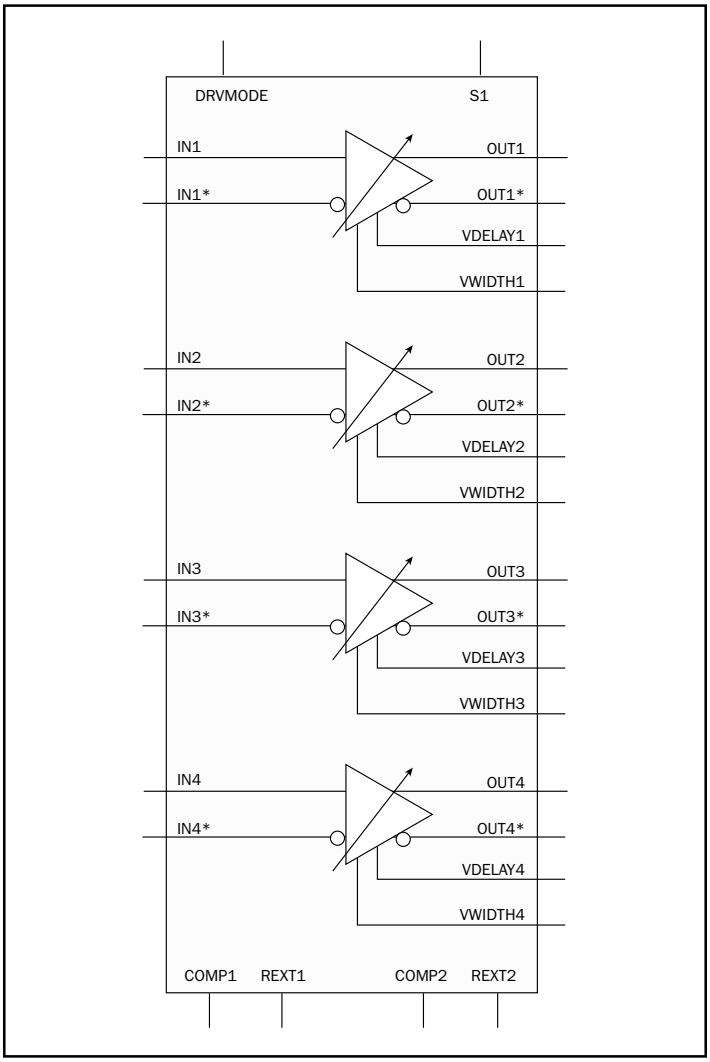
Applications

- Automatic Test Equipment
- Memory Tester Drive On Channel Deskew

Features

- Pin and Functionally Compatible with the Edge624 in Modes 0 and 2
- Independent Delay Adjustments for Positive and Negative Transitions
- Fanout Mode for One Input Distributed to All Channels
- 44-pin Plastic (PLCC) Package with Internal Heat Spreader or 44-pin MQFP Package with Internal Heat Spreader or Die Form

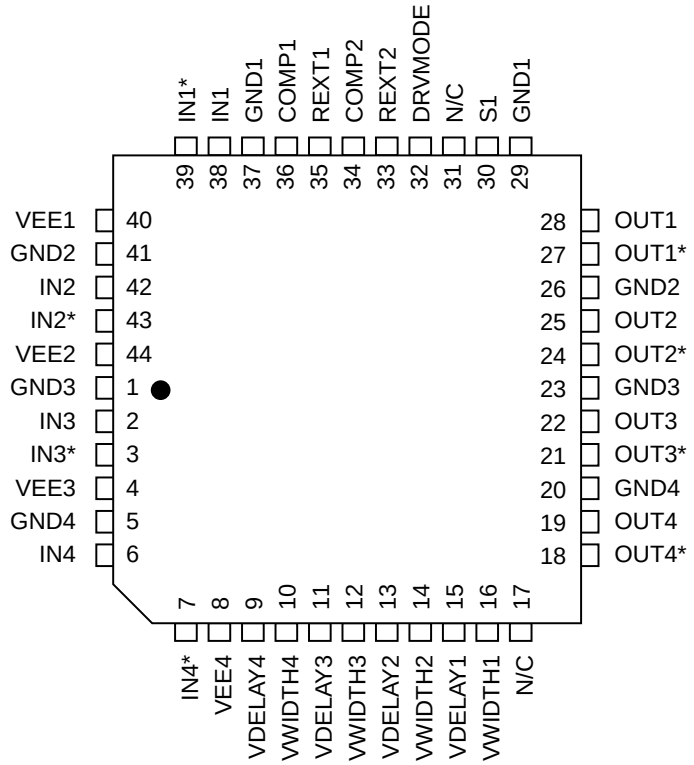
Functional Block Diagram



PIN Description

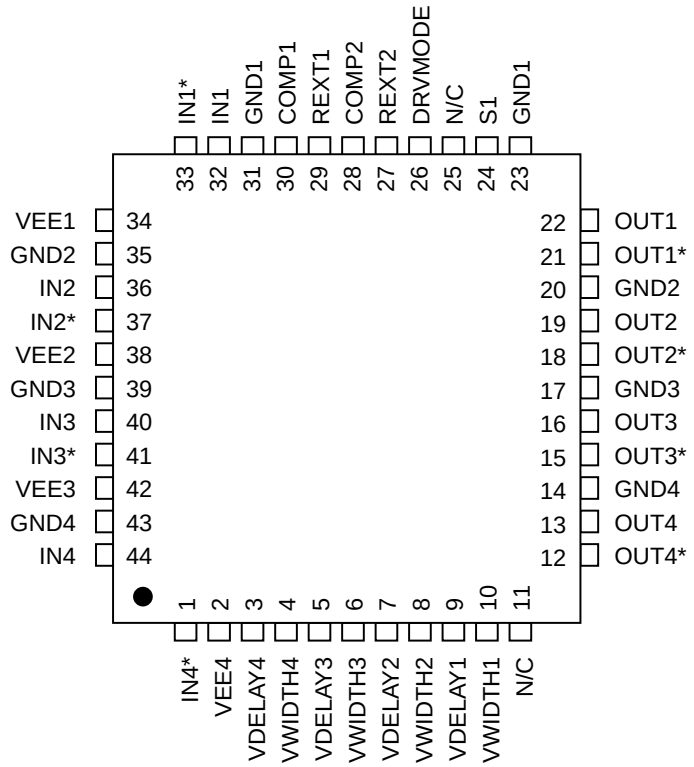
Pin Name	PLCC Pin #	PQFP Pin #	Description
DIGITAL			
IN, IN*	38, 39 42, 43 2, 3 6, 7	32, 33 36, 37 40, 41 44, 1	The input signal to be delayed. (Differential digital inputs.)
OUT, OUT*	28, 27 25, 24 22, 21 19, 28	22, 21 19, 18 16, 15 13, 12	The corresponding delayed output signal. (Differential ECL compatible outputs.)
DRVMODE	32	26	Single-ended 10KH ECL compatible input which determines whether the part is in fanout mode.
S1	30	24	Single-ended 10 KH ECL compatible input which defines the operating mode.
ANALOG			
VDELAY	15, 13, 11, 9	9, 7, 5, 3	Analog voltage input which controls the amount of propagation delay for each channel.
VWIDTH	16, 14, 12, 10	10, 8, 6, 4	Analog voltage input which controls the amount of falling edge delay for each channel.
REXT1	35	29	Analog input current used to establish the bias current for the VDELAY and VWIDTH inputs.
REXT2	33	27	Analog input current used to establish the bias level for the delay cells.
COMP1	36	30	Compensation pin. A 0.1 µF ceramic capacitor must be connected between COMP1 and VEE.
COMP2	34	28	Compensation pin. A 0.1 µF ceramic capacitor must be connected between COMP2 and VEE.
POWER			
GND	1, 5, 20, 23, 26, 29, 37, 41	39, 43, 14, 17, 20, 23, 31, 35	Device ground.
VEE	4, 8, 40, 44	42, 2, 34, 38	Device power supply.
N/C	17, 31	11, 25	No connect. There is no circuitry connected to these pins inside the package. These pins are not wire bonded to the die.

PIN Description *(continued)*



E628AHJ

44-Pin PLCC
w/Internal Heat Spreader



E628AHF

44-Pin MQFP
w/Internal Heat Spreader
10 mm x 10 mm Body Size

Circuit Description

Chip Overview

The Edge628 is a quad delay line and deskew element offering a 6.6 ns typical delay (Tspan), where the VDELAY inputs adjust the overall propagation delay of the part. In addition, the parts support a separate rising and falling edge delay of ± 750 ps (Twidth), where the VWIDTH inputs control the falling edge delay. There is also a drive mode, where the channel 2 input drives all four Edge628 outputs, with all other inputs ignored.

The Edge628 is designed to be monotonic and very stable in all modes of operation. Figures 1 shows a simplified block diagram.

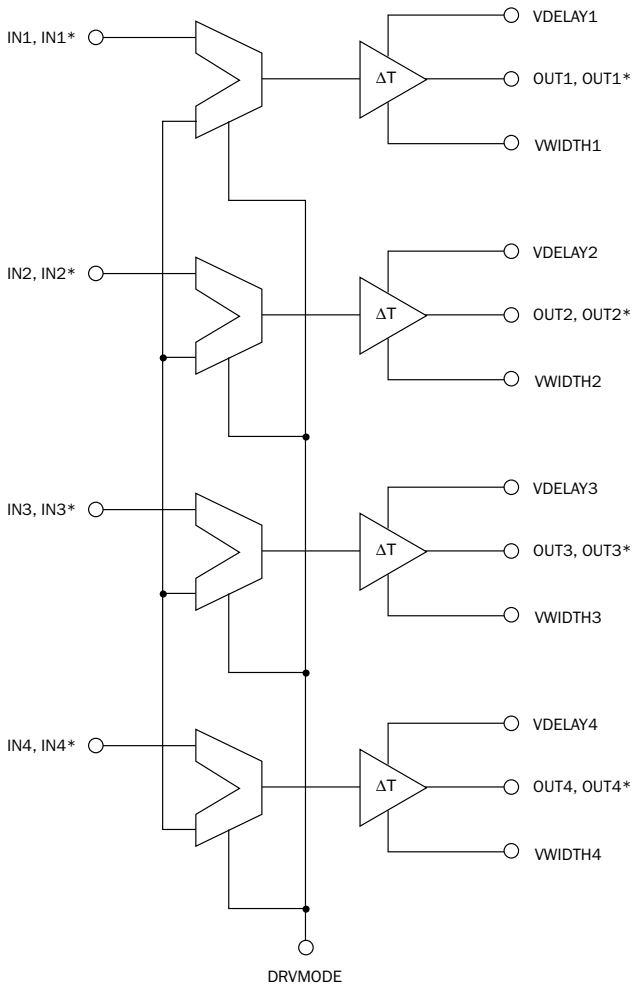


Figure 1. Edge628 Block Diagram

Operating Modes

The Edge628 has two modes of operation (described in Table 1.)

Mode	S1	TSPAN	TWIDTH
0	0	6.6 ns	N/A
2	1	6.6 ns	±750 ps

Table 1. Delay Ranges Versus Mode

Mode 0

Mode 0 is a simple delay mode (see Figures 2 and 3). The input signal for each channel is delayed by some programmable amount determined by the analog input VDELAY.

The rising and falling edges are delayed equally. The VWIDTH analog input has no function in mode 0. The propagation delay for a rising and falling edge is defined as

$$Tpd+, Tpd- = Tpd(min) + Tspan$$

where Tpd(min) is the raw propagation delay of the part with minimum programmed delay, and Tspan is the additional delay programmed via the VDELAY input.

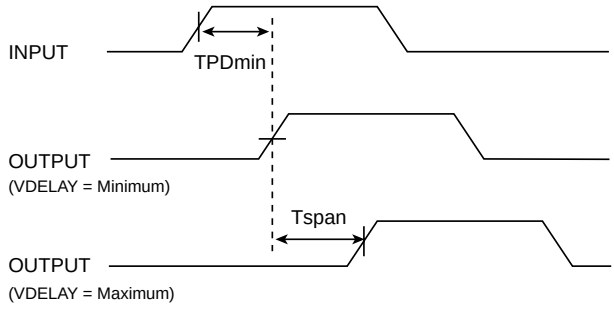


Figure 2. Mode 0 VDELAY Control

Circuit Description *(continued)*

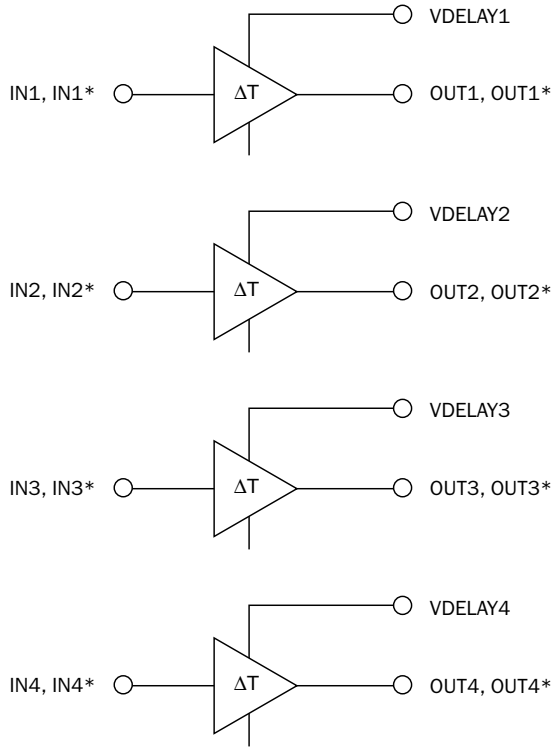


Figure 3. Mode 0 Functional Diagram

Analog Delay Inputs

VDELAY and VWIDTH are analog voltage inputs which control the delay of the rising and falling edge. VDELAY and VWIDTH vary from +0.1V (minimum delay) to -1.1V (maximum delay).

The transfer function for Tspan vs. VDELAY is shown in Figure 4.

These inputs are designed to sink a constant input current over the entire operating range. The fact that the VDELAY and VWIDTH inputs have internal current sources allows a voltage DAC capable of generating only positive voltages and an external resistor network to be pulled down to the Edge628's negative input voltage compliance. These current sources are designed to be constant over temperature, so changes in system temperature will not translate into a delay voltage shift.

The VDELAY and VWIDTH inputs require current flow. If mode 0 is used, connect all VWIDTH inputs to ground. Also, connect any unused VDELAY and VWIDTH inputs to ground.

The equation used to establish the VDELAY and VWIDTH input currents is:

$$I\ (VWIDTH, VDELAY) = (1.267 / REXT1) * 2.283$$

where 1.267 equals the typical voltage at the REXT1 pin, and 2.283 equals the typical gain factor. For example, the VDELAY and VWIDTH input currents would be 1.0 mA with REXT1 = 2.87 KΩ.

Using a different REXT1 will program a different input current. Any voltage DAC used to drive these inputs directly needs to be capable of sourcing a current at least equal to the programmed current. Any current DAC used needs to factor in this constant input current as well.

However, the value of this current does not affect deskew range or performance. The ability to vary this current allows a more flexible interface to a variety of DAC programming techniques.

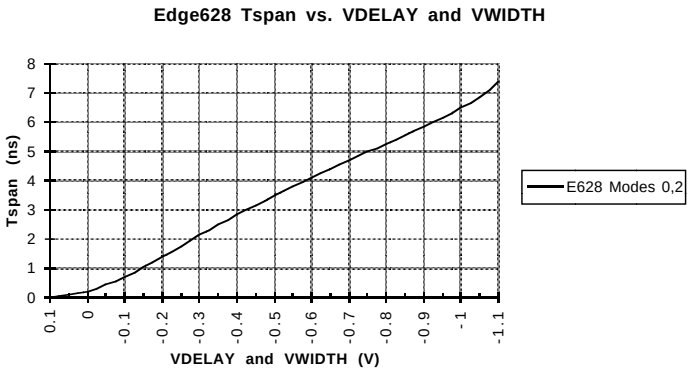


Figure 4. Tspan Transfer Function

Circuit Description *(continued)*

Mode 2

Mode 2 allows independent adjustment of the rising and falling edges (see Figures 5 and 6). The propagation delay for a rising edge is defined as

$$Tpd+ = Tpd(min) + Tspan$$

where Tpd(min) is the raw propagation delay of the part with minimum programmed delay, and Tspan is the additional delay programmed via the VDELAY input.

The propagation delay for a falling edge is defined as

$$Tpd- = Tpd(min) + Tspan + Twidth$$

where Twidth is defined as the additional delay incurred by adjusting the VWIDTH input. Notice that Twidth can be either positive or negative, allowing the part to either expand or contract an input signal (see Figure 5).

Notice also that Tpd+ is a function of VDELAY only, while Tpd– is a function of VDELAY and VWIDTH. The transfer function for Tspan vs. VDELAY is shown for both modes in Figure 4. The transfer function for Twidth vs. VWIDTH and VDELAY is shown in Figure 7.

Programming Sequence

VDELAY, in addition to affecting the placement of the rising edge, also affects the falling edge. Therefore, when calibrating a system, VDELAY should be adjusted first. As VWIDTH affects only the falling edge, it should be adjusted only after VDELAY is established.

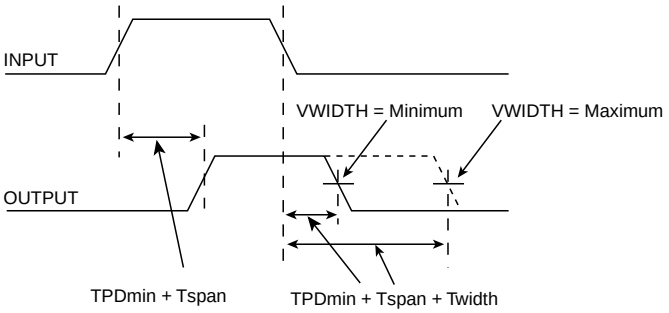


Figure 5. Mode 2 VDELAY and VWIDTH Controls

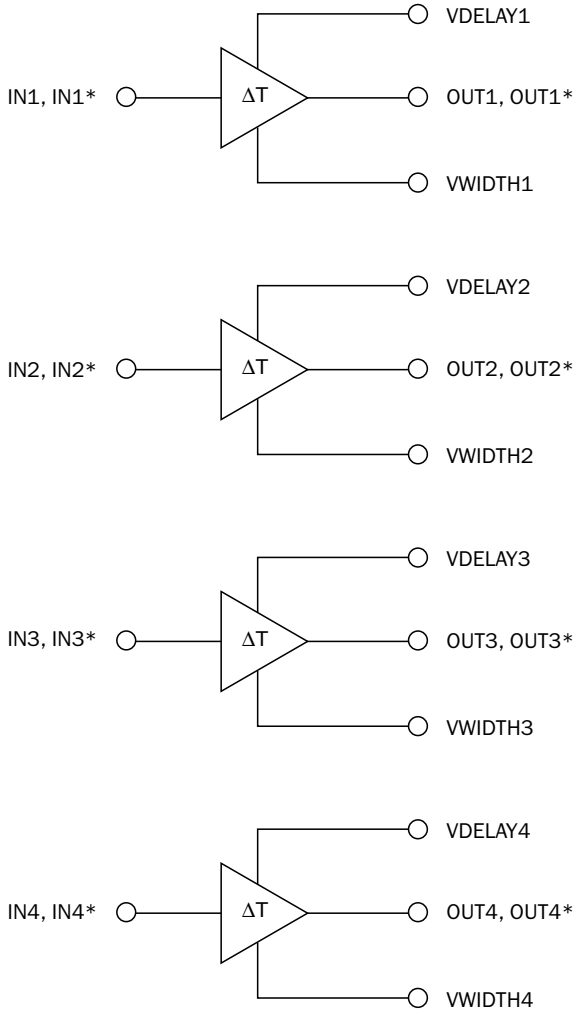


Figure 6. Functional Model in Mode 2.

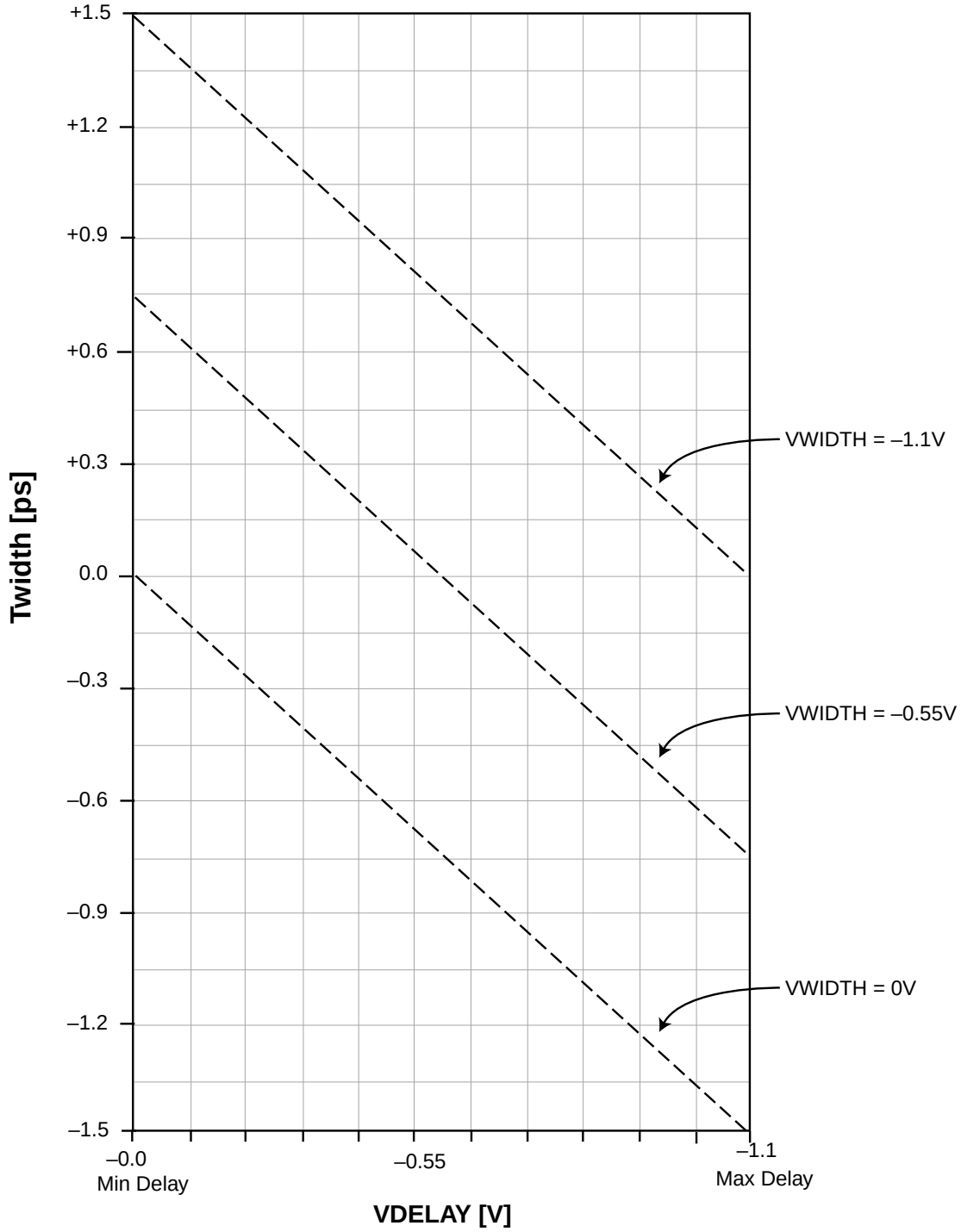


Figure 7. Mode 2 Transfer Function

Circuit Description *(continued)*

Drive Mode

With DRVMODE = 1, the input signal on channel 2 will be routed to all Edge628 delay paths. In drive mode, operating mode 0 and 2 still offer the same delay range and edge control features. The only difference is that the input signal now comes from channel 2, while all other inputs (In/In*) are ignored.

Figures 8 and 9 show a simplified model for drive mode.

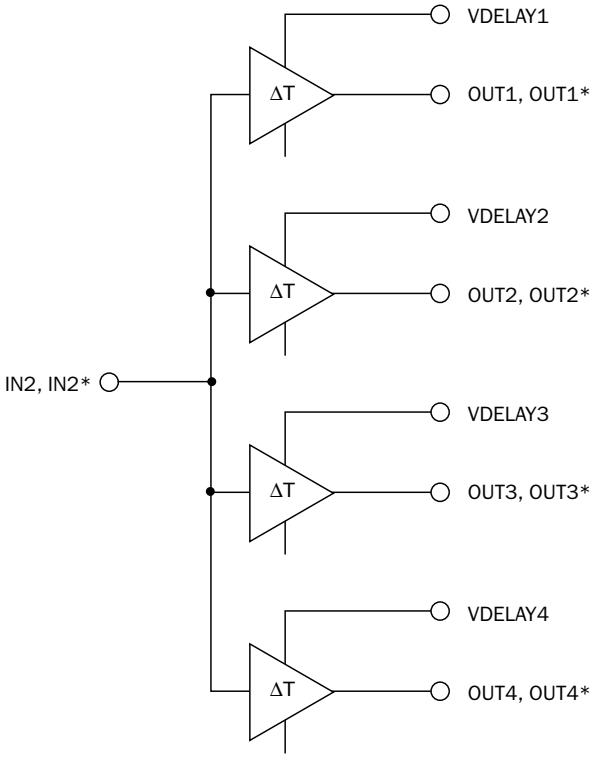


Figure 8. Edge628 Drive Mode for Operating Mode 0

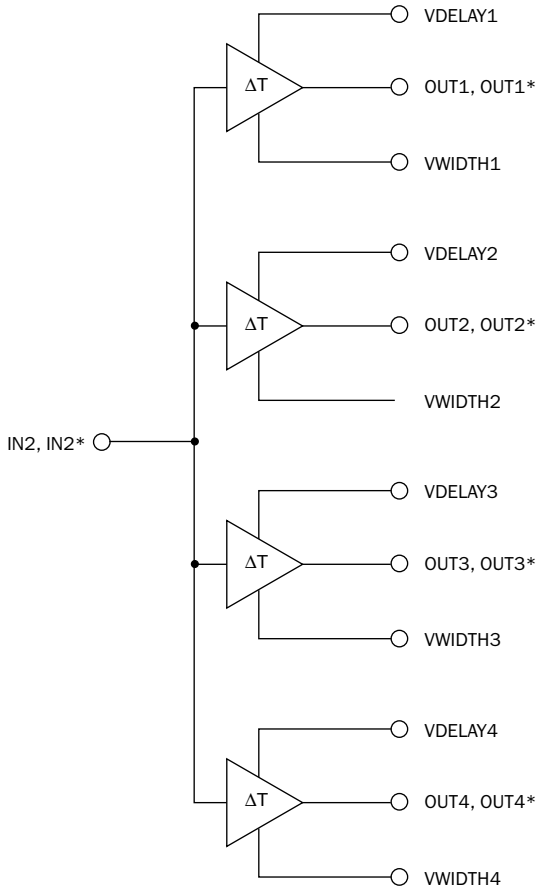


Figure 9. Edge628 Drive Mode for Operating Mode 2

Application Information

Power Up Initialization

Note: Mode 2 uses an SR flip-flop at the output stage; modes 0 does not. Therefore, upon power up in mode 2, or when operating modes are being changed into mode 2, the SR flip-flop is in an indeterminate state and the output may not reflect the input condition. A rising or falling edge that propagates through the channel will correctly reset the part. Therefore, in mode 2, a dummy edge should be applied before calibration or real time execution.

Notice also that in mode 0 there is NO flip-flop. The output will therefore always reflect the status of the inputs.

Minimum Pulse Width

The minimum pulse width that the part can support is a function of the operating mode and the programmed delay value. Figure 10 documents the maximum usable delay as a function of pulse width.

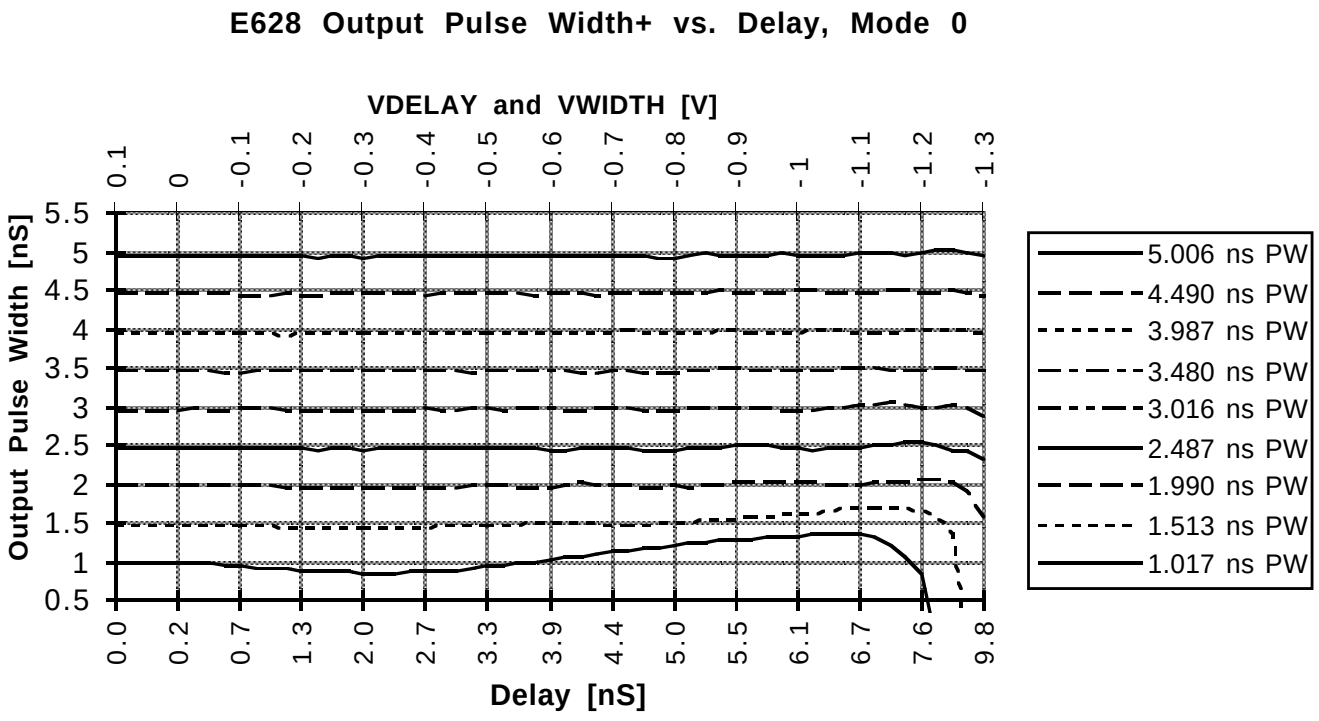
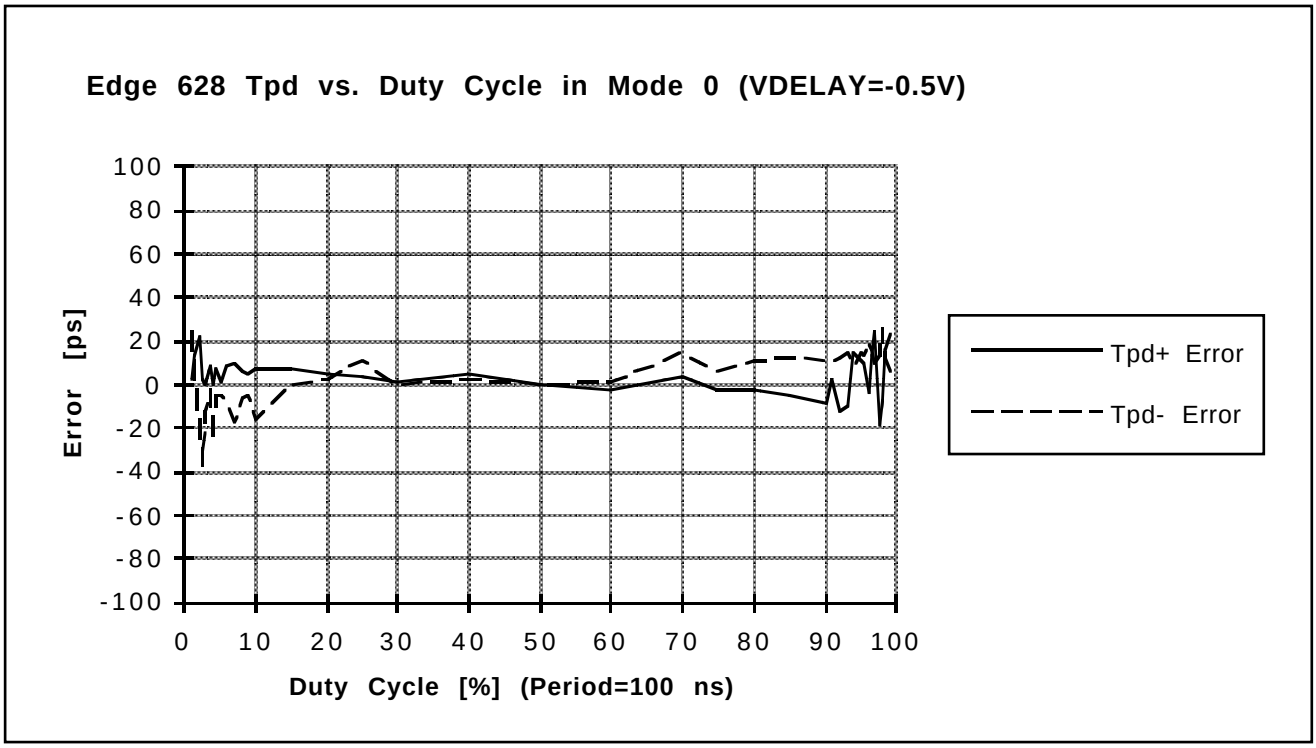
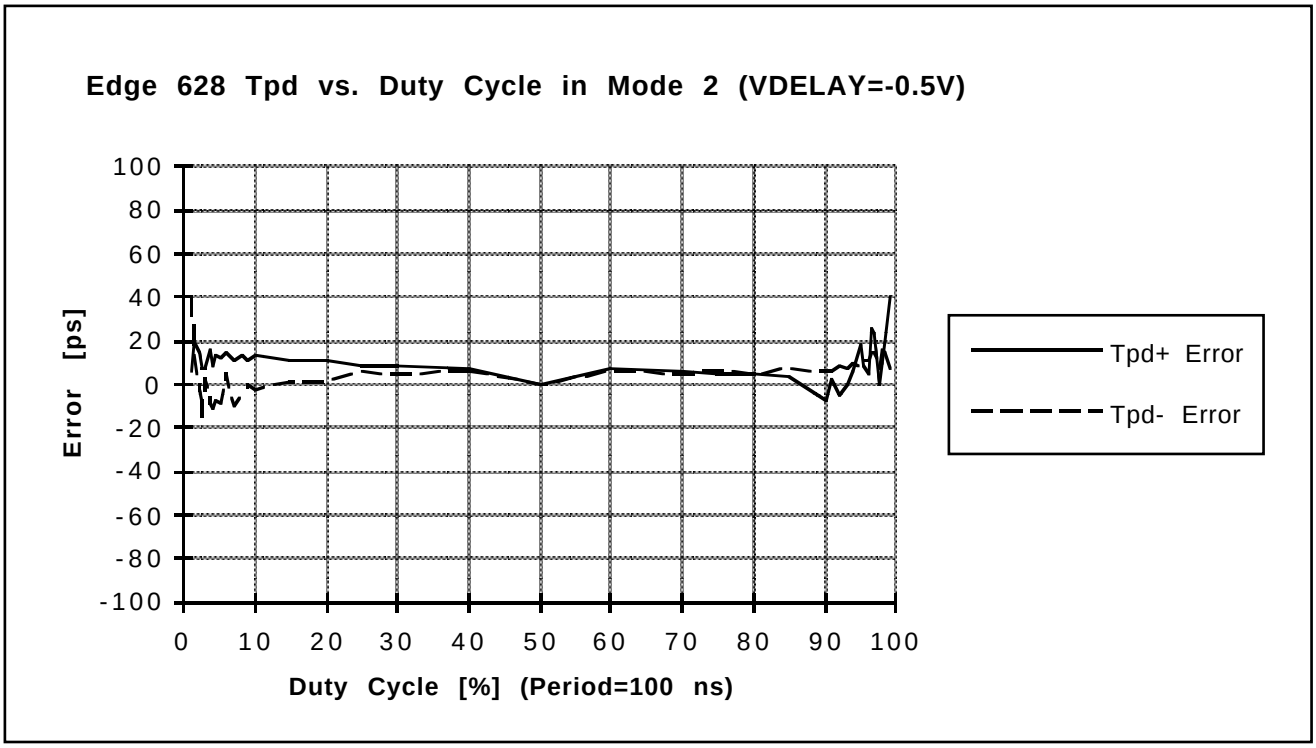


Figure 10. Minimum Pulse Width Capability

Application Information *(continued)*



Figures 11 and 12. Timing Error vs. Duty Cycle for Modes 0 and 2.

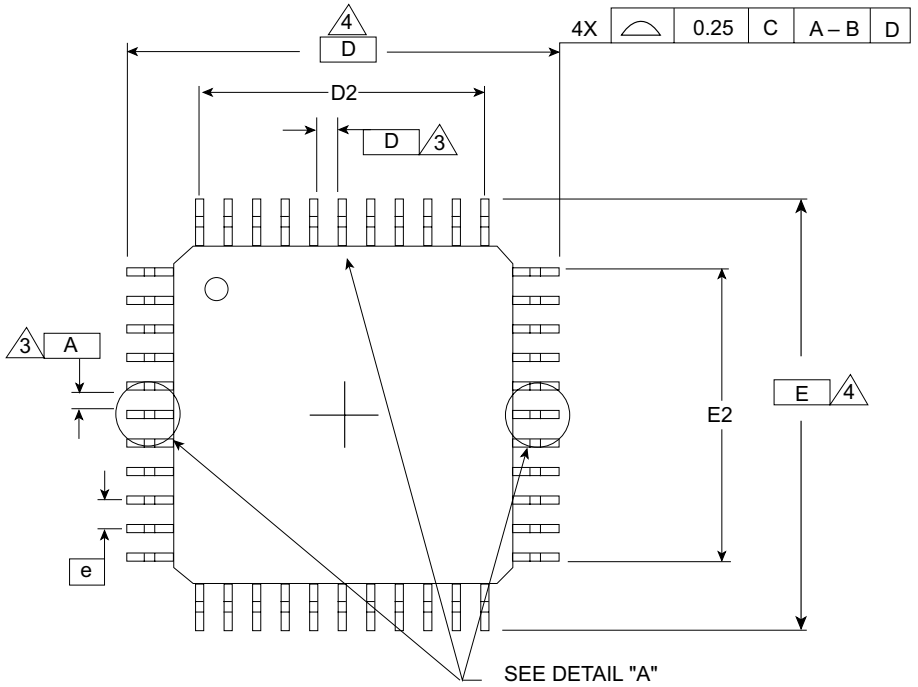


Application Information *(continued)*

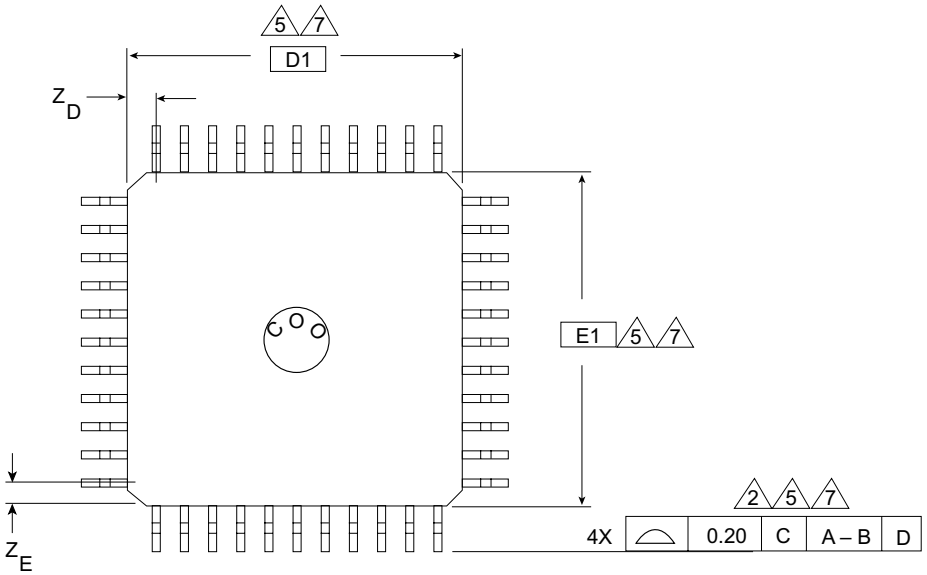
Parameter	Symbol	Min	Typ	Max	Units
Thermal Resistance					
PLCC w/Heat Spreader					
Junction to Air					
Still Air	θJA		41		˚C/W
50 LFPM of Airflow	θJA		33		˚C/W
400 LFPM of Airflow	θJA		21		˚C/W
MQFP w/Heat Spreader					
Junction to Air					
Still Air	θJA				˚C/W
50 LFPM of Airflow	θJA				˚C/W
400 LFPM of Airflow	θJA		32		˚C/W

Package Thermal Data

44-Pin MQFP Package

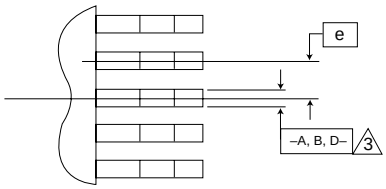


TOP VIEW

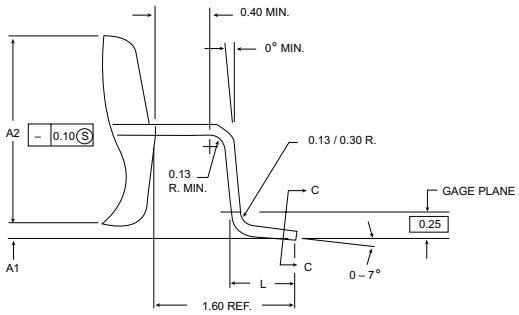


BOTTOM VIEW

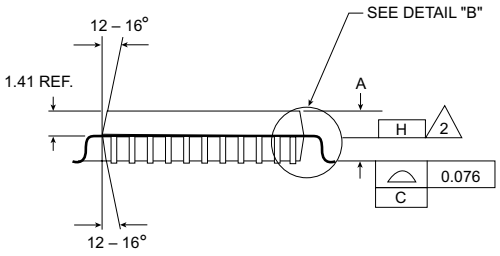
44-Pin MQFP Package *(continued)*

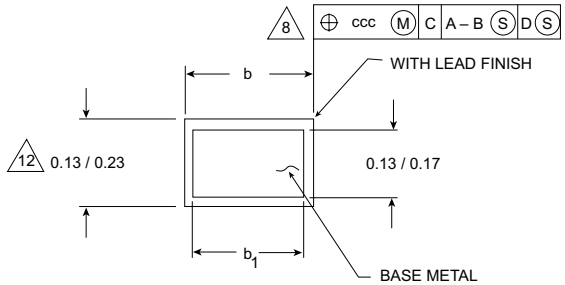


DETAIL "A"



DETAIL "B"





SECTION C-C

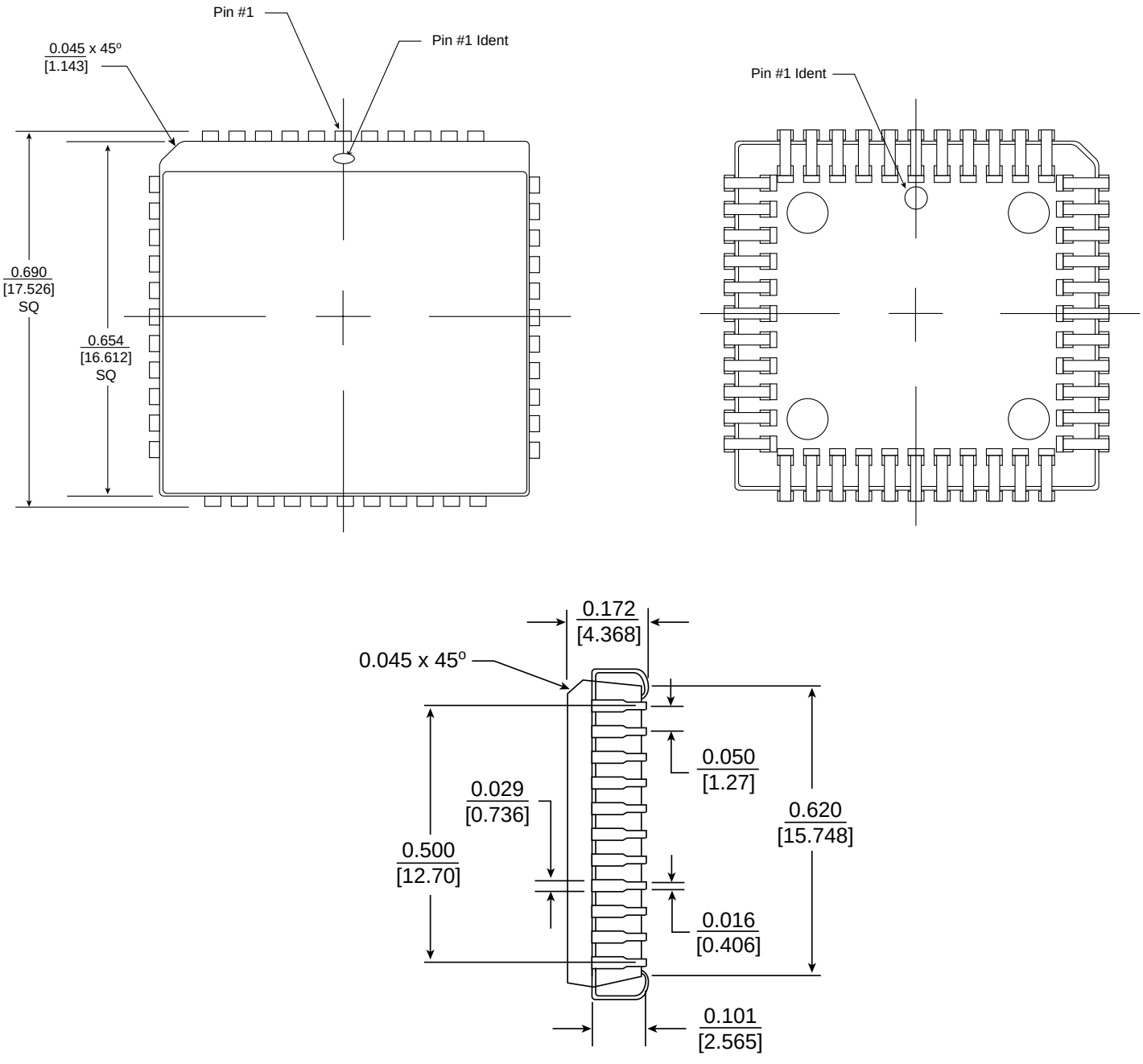
Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined where centerline between leads exits plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane -H-.
6. "N" is the total # of terminals.
7. Package top dimensions are smaller than bottom dimensions by 0.20 mm, and top of package will not overhang bottom of package.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
9. All dimensions are in millimeters.
10. Maximum allowable die thickness to be assembled in this package family is 0.635 millimeters.
11. This drawing conforms to JEDEC registered outline MS-108.
12. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

Symbol	Min	Nom	Max	Note	Comments
A		2.15	2.35		Height above PCB
A1	0.10	0.15	0.25		PCB Clearance
A2	1.95	2.00	2.10		Body Thickness
D		13.20 BSC		4	
D1		10.00 BSC		5	Body Length
D2		8.00 REF			
ZD		1.00 REF			
E		13.20 BSC		4	
E1		10.00 BSC		5	Body Width
E2		8.00 REF			
ZE		1.00 REF			
L	0.73	0.88	1.03		
N		44		6	Pin Count
e		0.80			Lead Pitch
b	0.30		0.45	8	
b1	0.30	0.30	0.40		
aaa		0.16			

Package Information *(continued)*

44-Pin PLCC Package



Notes: (unless otherwise specified)

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	GND	0	0	0	V
Negative Power Supply	VEE	–4.2	–5.2	–5.5	V
Ambient Operating Temperature	TA	0		+70	˚C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (relative to GND)		–6.0		+0.5	V
Voltage on any Digital Pin		VEE		GND	V
Output Current		–50		50	mA
Ambient Operating Temperature	TA	–55		125	˚C
Storage Temperature	TS	–65		150	˚C
Junction Temperature	TJ			150	˚C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	˚C

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Digital Input High Voltage (Note 1) IN, IN*	IN – IN*	250			mV
Digital Input Low Voltage (Note 1) IN, IN*	IN* – IN	250			mV
Digital Input High Voltage (Note 1) DRVMODE, S1	VIH	–1070		0	mV
Digital Input Low Voltage (Note 1) DRVMODE, S1	VIL	VEE		–1450	mV
Input Common Mode Range	IN, IN*	–2.0		–0.5	V
Input High Current (Vin = VILmax) IN, DRVMODE, S1 IN*	 IIH IIH	 –50	 130 –15	 250 	 µA µA
Input Low Current (Vin = VILmin) IN, DRVMODE, S1 IN*	 IIL IIL	 –100	 80 –45	 150 	 µA µA
Outputs					
Digital Output High Voltage	OUT – OUT*	500			mV
Digital Output Low Voltage	OUT* – OUT	500			mV
Output Common Mode Range	$\frac{OUT + OUT^*}{2}$	–1.5	–1.3	–1.1	V
VEE Supply Current @ REXT2 = 2.94K	IEE	–365		–200	mA
VEE Supply Current @ REXT2 = 2.1K	IEE	–380		–230	mA
Voltage Level at REXT1 Pin	VEXT1	–1.30		–1.20	V
Current Gain, IEXT1 to IDELAY and IWIDTH	IGAIN	2.15		2.35	

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REXT1 = 2.94 KΩ, and REXT2 = 2.1 KΩ. All parameters specified at 0°C are guaranteed by characterization and are not production tested. The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delays					
Minimum Delays (Pulse Width > 3 ns)					
MODE *S1* *VDELAY* *VWIDTH*					
0 0 +0.1V X	TPDmin	1.5	2.1	2.6	ns
2 1 +0.1V +0.1V	TPDmin	1.6	2.2	2.7	ns
Delay Range vs. Pulse Width					
(VWIDTH = VDELAY in Mode 2)					
Input Pulse Width > 3.0 ns (Note 1) (–1.1V < VDELAY < +0.1V)	Tspan	4.5	6.6	10.0	ns
Input Pulse Width > 1.9 ns (Note 1) (–0.9V < VDELAY < +0.1V)	Tspan	4.2	6.6	9.0	ns
Input Pulse Width > 1.4 ns (Note 1) (–0.8V < VDELAY < +0.1V)	Tspan	4.0	6.5	8.0	ns
VWIDTH Range of Adjustment (Mode 2 Only)					
Input Pulse Width > 3.0 ns (Note 1) (–1.1V < VWIDTH < +0.1V)	Twidth	1.1	1.5		ns
Input Pulse Width > 1.9 ns (Note 1) (–0.9V < VWIDTH < +0.1V)	Twidth	1.0	1.3		ns
Input Pulse Width > 1.4 ns (Note 1) (–0.8V < VWIDTH < +0.1V)	Twidth	0.8	1.0		ns
Propagation Delay Tempco, Rising Edge (Note 1)					
–0.9V <= VDELAY <= +0.1V	TEMPCO+	1	2.5	4	ps / ˚C
–1.1V <= VDELAY <= –0.9V		3	10	15	ps / ˚C
Propagation Delay Tempco, Falling Edge (Note 1)					
–0.9V <= VWIDTH <= +0.1V, VDELAY => –0.9V	TEMPCO–	1	2.5	4	ps / ˚C
–1.1V <= VWIDTH <= –0.9V, VDELAY = –0.9V		3	5.5	6	ps / ˚C
Output Rise / Fall Times (20 to 80%) (Note 1)	Tr, Tf	250	375	450	ps

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with TA = 25 ˚C with 400 LFPM of airflow, and all outputs terminated with 50 Ω to –2.0 V. Timing reference points at the differential crossing points for input and output signals, REXT1 = 2.94 KΩ, and REXT2 = 2.1 KΩ. All input signals are fully differential. Values are based on nominal temperature and a supply voltage of –5.5 V.

Note 1: Based upon characterization data. Not production tested.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board..

AC Characteristics *(continued)*

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delays					
Minimum Rising Edge Delay for Guaranteed –300 ps Falling Edge Adjustment Range; VDELAY = –.19V, VWIDTH = +0.1V	TPD+min	3.45		4.35	ns
Rising Edge Delay Range for Guaranteed +/–300 ps Falling Edge Adjustment Range; VDELAY = –.19V, VWIDTH = +0.1V to VDELAY = –.9V, VWIDTH = –1.2V	Tspan+	3.50		4.50	ns
Rising Edge Span –1.1V < VDELAY < .1V	Tspan+	4.5		10.0	ns
VWIDTH Range –1.1V < VWIDTH < +0.1V	Twidth	1.0			ns
Rising Edge Delay Range for Guaranteed +/–450 ps Falling Edge Adjustment Range; VDELAY = –.3V, VWIDTH = +0.1V to VDELAY = –.9V, VWIDTH = –1.3V	Tspan+	2.70		3.70	ns
Tpd– vs. Tpd+ (Note 2) VDELAY = –.19V, VWIDTH = +0.1V	Tskew–	–1.00		–0.20	ns
Tpd– vs. Tpd+ (Note 2) VDELAY = –.3V, VWIDTH = +0.1V	Tskew–	–1.00		–0.35	ns
Tpd– vs. Tpd+ (Note 2) VDELAY = –.9V, VWIDTH = –1.2V	Tskew–	0.20		1.00	ns
Tpd– vs. Tpd+ (Note 2) VDELAY = –.9V, VWIDTH = –1.3V	Tskew–	0.35		1.00	ns
Propagation Delay Tempco, Rising Edge (Note 1) –0.84V <= VDELAY <= –0.18V	TEMPCO+	0	2.5	4	ps / ˚C
Propagation Delay Tempco, Fallilng Edge (Note 1)	TEMPCO–				
–1.15V <= VWIDTH <= +0.1V, VDELAY > –0.84V		0	3.5	5	ps / ˚C
–1.25V <= VWIDTH <= +0.1V, VDELAY > –0.84V		0	7.5	10	ps / ˚C
1 Sigma Jitter, <100 mV P-P VEE Noise, 1 Hz to 20 MHz (Note 1)	PSRR		8	10	ps

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with TA = 25 ˚C with 400 LFPM of airflow, and all outputs terminated with 50 Ω to –2.0 V. Timing reference points at the differential crossing points for input and output signals, REXT1 = 2.94 KΩ, and REXT2 = 2.94 KΩ. All input signals are fully differential. Values are based on nominal temperature and a supply voltage of –5.2 V.

Note 1: Based upon characterization data. Not production tested.

Note 2: Guaranteed by design. Not production tested.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device mounted either in the test socket or on the printed circuit board.

Ordering Information

Model Number	Package
E628AHF	44 Pin MQFP w/Internal Heat Spreader 10 mm X 10 mm Body Size
E628AHJ	44 Pin PLCC w/Internal Heat Spreader
D628	Die

Contact Information

Semtech Corporation
High-Performance Division
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Revision Histor y

Current Revision Date: May 4, 2001
Previous Revision Date: April 25, 2001

Page #	Section Name	Previous Revision	Current Revision
2	Pin Description	N/C	*Add:* There is no circuitry to these pins inside the package. These pins are not wire bonded to the die.
15	Ab Max Ratings	VEE (relative to GND), Max: 6.0	VEE (relative to GND), Max: +0.5 Soldering Temp, Max: 260

Current Revision Date: April 25, 2001
Previous Revision Date: March 8, 2001

Page #	Section Name	Previous Revision	Current Revision
			Remove: "Preliminary"
16	DC Characteristics	Digital Input Low Voltage, Min: –1.8V	Digital Input Low Voltage, Min: VEE

Current Revision Date: March 8, 2001
Previous Revision Date: January 10, 2001

Page #	Section Name	Previous Revision	Current Revision
3	Pin Description	Bottom Drawing Title: E628AHJ 44-Pin PLCC	Bottom Drawing Title: E628AHF 44-Pin MQFP
12-14	Package Information		*Add*: Titles to Package Drawings
18	AC Characteristics	Rising Edge Delay Range VDELAY = –.9V, VWIDTH = –1.15V	Rising Edge Delay Range VDELAY = –.9V, VWIDTH = –1.2

Revision Histor y

Current Revision Date: January 10, 2001
Previous Revision Date: January 8, 2001

Page #	Section Name	Previous Revision	Current Revision
16	DC Characteristics	Digital Input Low Voltage, Min: VEE Output Common Mode Range, Min: – 1.1, Max: – 1.5 VEE Supply Current @ REXT2 = 2.94K, Min: 270, Max: 365 VEE Supply Current @ REXT2 = 2.1K Min: 335, Max: 380	Digital Input Low Voltage, Min: – 1.8V Output Common Mode Range, Min: – 1.5, Max: – 1.1 VEE Supply Current @ REXT = 2.94K Min: – 365, Max: – 200 VEE Supply Current @ REXT2 = 2.1K Min: – 380, Max: – 230

Current Revision Date: January 8, 2001
Previous Revision Date: October 23, 2000

Page #	Section Name	Previous Revision	Current Revision
15	Absolute Maximum Ratings	VEE (relative to GND), Max: -6.0 Voltage on any Digital Pin, Max: VEE Output Current, Max: -50	VEE (relative to GND), Max: 6.0 Voltage on any Digital Pin, Max: GND Output Current, Max: 50
16	DC Characteristics	VEE Supply Current @ REXT2 = 2.94K Min: -200, Max: -365 VEE Supply Current @ REXT2 = 2.1K Min: -230, Max: -380	VEE Supply Current @ REXT2 = 2.94K Min: 270, Max: 365 VEE Supply Current @ REXT2 = 2.1K Min: 335, Max: 380
17	AC Characteristics	Input Pulse Width > 1.9 ns, Min: 5.0 Input Pulse Width > 1.4 ns, Min: 5.0 Width Range of Adjustment, Min: 1.0	Input Pulse Width > 1.9 ns, Min: 4.2 Input Pulse Width > 1.4 ns, Min: 4.0 Width Range of Adjustment, Min: 1.1

Current Revision Date: October 23, 2000
Previous Revision Date: September 20, 2000

Page #	Section Name	Previous Revision	Current Revision
17	DC Characteristics	VEE Supply Current @ REXT = 2.94K Min: 270, Max: 365 VEE Supply Current @ REXT = 2.1K Min: 335, Max: 380	VEE Supply Current @ REXT = 2.94K Min: 200, Typ: , Max: 365 VEE Supply Current @ REXT = 2.1K Min: 230, Max: 380
19	AC Characteristics		*Add:* Rising Edge Span - Min: 4.5, Max 10.0 ns VWIDTH Range - Min: 1.0 ns

Revision Histor y

Current Revision Date: September 20, 2000
Previous Revision Date: September 11, 2000

Page #	Section Name	Previous Revision	Current Revision
17	DC Characteristics	VEE Supply Current @ REXT = 2.94K Min: 200, Typ: 265, Max: 300 VEE Supply Current @ REXT = 2.1K Min: 230, Max: 350	VEE Supply Current @ REXT = 2.94K Min: 270, Typ: , Max: 365 VEE Supply Current @ REXT = 2.1K Min: 335, Max: 380
		Voltage Level at REXT1 Pin Min: -1.305, Typ: 1.267, Max: -1.229	Voltage Level at REXT1 Pin Min: -1.30, Typ: , Max: -1.20
		Current Gain Min: 2.214, Typ: 2.283, Max: 2.351	Current Gain Min: 2.15, Typ: , Max: 2.35
18	AC Characteristics	Delay Range vs. Pulse Width (VWIDTH = VDELAY in Mode 2) Min: 5.5	Delay Range vs. Pulse Width (VWIDTH = VDELAY in Mode 2) Min: 4.5
19	AC Characteristics	Propagation Delays VDELAY = -.18V, Min: 3.75, Typ: 4.04, Max: 4.25	Propagation Delays VDELAY = -.19V, Min: 3.45, Typ: , Max: 4.35
		Rising Edge Delay Range for guaranteed +- 300 ps VDELAY= -0.18V, VDELAY = -0.84V Min: 4.00, Typ: 4.50, Max: 4.80	Rising Edge Delay Range for guaranteed +- 300 ps VDELAY - 0.19V, VDELAY = 0.9V Min: 3.50, Typ:, Max: 4.50
		Rising Edge Delay Range for guaranteed +-450 ps VDELAY = -0.27V, VDELAY = -0.84, VWIDTH = -1.25V Min: 3.20, Typ: 3.77, Max: 4.10	Rising Edge Delay Range for guaranteed +-450 ps VDELAY = -0.3V, VDELAY = -0.9V, VWIDTH = -1.3V Min: 2.70, Typ: , Max: 3.70
		Typ- vs. Tpd+ (Note 1) VDELAY = -0.18V Typ: -0.39, Max: -0.30	Typ- vs. Tpd+ (Note 2) VDELAY = -0.19V Typ: , Max: -0.20
		Typ- vs. Tpd+ (Note 1) VDELAY = -0.27V Typ: -0.57, Max: -0.45	Typ- vs. Tpd+ (Note 2) VDELAY = -0.3V Typ: , Max: -0.35
		Typ- vs. Tpd+ (Note 1) VDELAY = -0.84V, VWIDTH = -1.15V Min: 0.30, Typ: 0.42	Typ- vs. Tpd+ (Note 2) VDELAY = -0.9V, VWIDTH = -1.2V Min: 0.20, Typ:
		Typ- vs. Tpd+ (Note 1) VDELAY = -0.84V, VWIDTH = -1.25V Min: 0.45, Typ: 0.68	Typ- vs. Tpd+ (Note 2) VDELAY = -0.9V, VWIDTH = -1.3V Min: 0.35, Typ:
			Add: Note 1. Based upon characterization data. Not production tested.

Current Revision Date: September 11, 2000
Previous Revision Date: February 8, 2000

Page #	Section Name	Previous Revision	Current Revision
19	AC Characteristics		*Add:* "Note 1" to Tpd- vs. Tpd+

Current Revision Date: February 8, 2000
Previous Revision Date: March 26, 1999

Page #	Section Name	Previous Revision	Current Revision
13 - 15	Package Informtion		*Add:* Package Information