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EK7304 DATA SHEET	版 本 REV ：1.0
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1.0	2001/8/29	2001/8/29		新增訂

Eureka Microelectronics,Inc.

EK7304

256 Output TFT Gate Driver IC

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256- Output TFT Gate Driver IC

DESCRIPTION

The EK7304 is a 256-output TFT gate driver IC suitable for driving large/medium scale of TFT LCD panels. Through the use of TCP, it substantially decreases the size of the frame section of LCD module.

FEATURES

- Output channels: 256 outputs
- Driver operating frequency: max. 1200kHz
- LCD drive voltage: max. V_{EE}+43V
- Driver output levels: two ("L" level is changeable)
- Incorporates bi-directional shift register.
- Supports multi chip operation via output pins.
- Pulse width modulation function.

BLOCK DIAGRAM

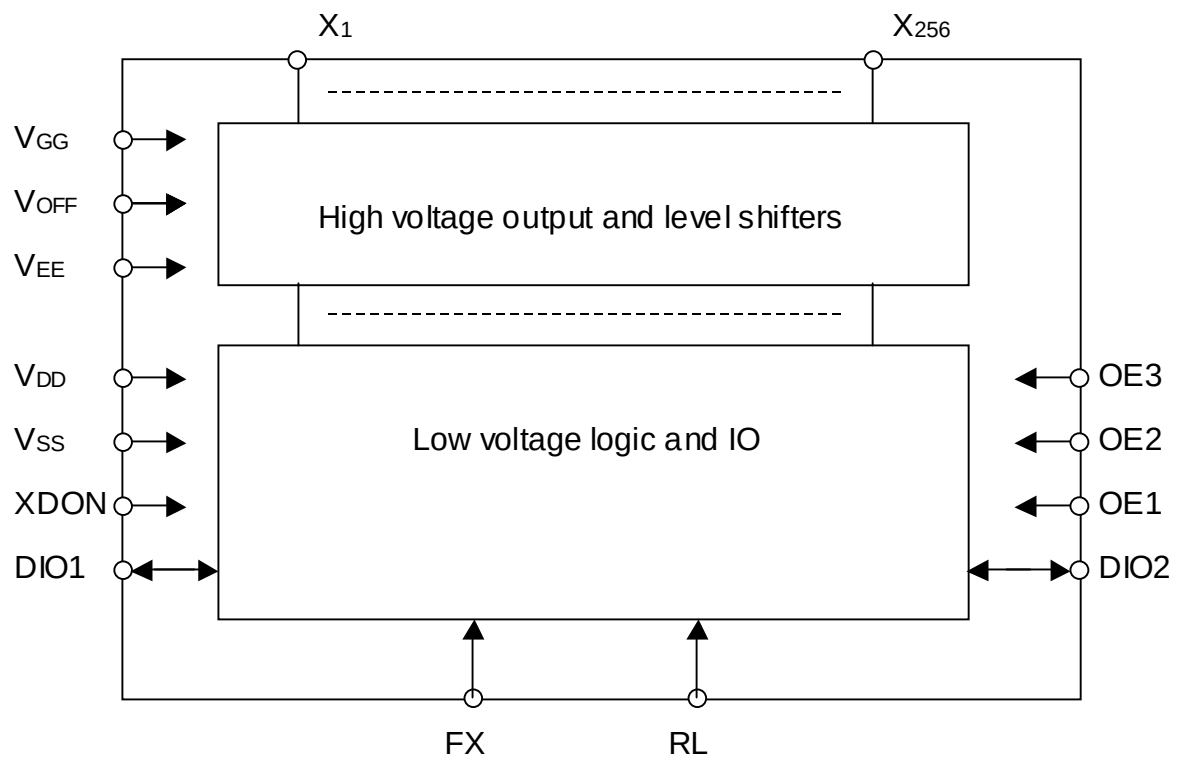

Fig. 1. Block diagram

PIN CONNECTIONS

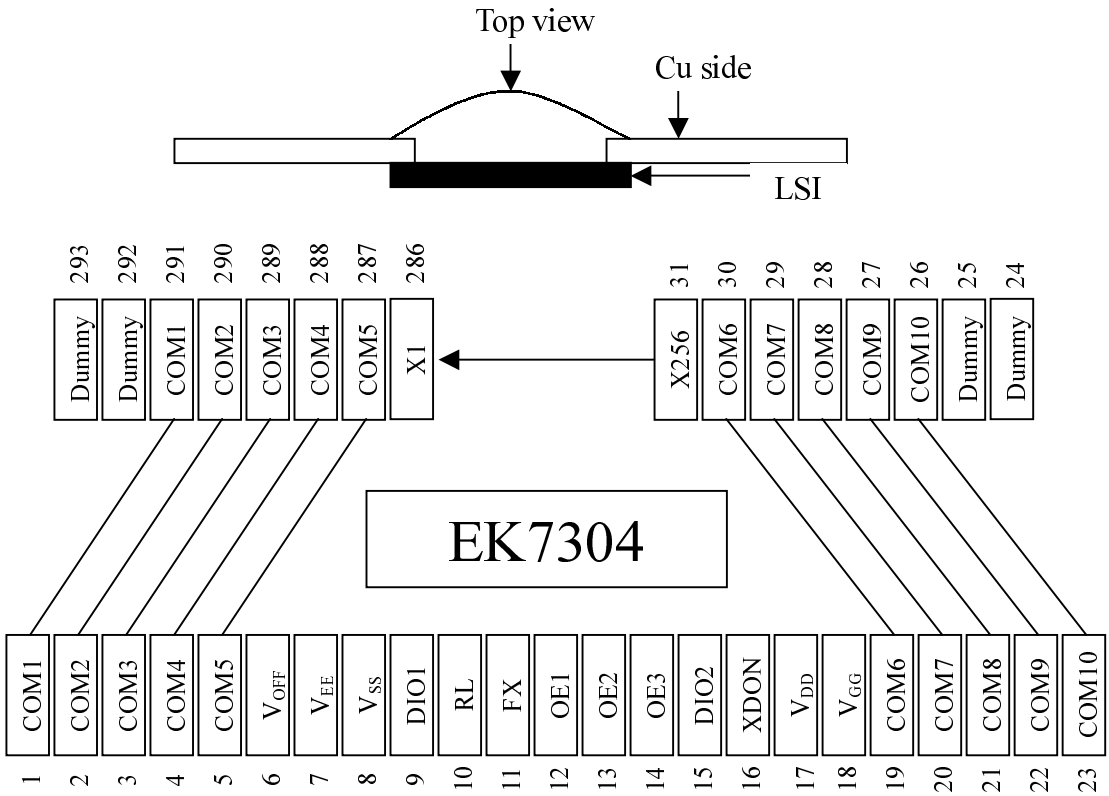

Fig. 2. Pin diagram

Terminal	Terminal Name	Terminal	Terminal Name	Terminal	Terminal Name	Terminal	Terminal Name	Terminal	Terminal Name	Terminal	Terminal Name	Terminal	Terminal Name
1	COM1	44	X243	87	X200	130	X157	173	X114	216	X71	259	X28
2	COM2	45	X242	88	X199	131	X156	174	X113	217	X70	260	X27
3	COM3	46	X241	89	X198	132	X155	175	X112	218	X69	261	X26
4	COM4	47	X240	90	X197	133	X154	176	X111	219	X68	262	X25
5	COM5	48	X239	91	X196	134	X153	177	X110	220	X67	263	X24
6	V_{OFF}	49	X238	92	X195	135	X152	178	X109	221	X66	264	X23
7	V_{EE}	50	X237	93	X194	136	X151	179	X108	222	X65	265	X22
8	V_{SS}	51	X236	94	X193	137	X150	180	X107	223	X64	266	X21
9	DIO1	52	X235	95	X192	138	X149	181	X106	224	X63	267	X20
10	RL	53	X234	96	X191	139	X148	182	X105	225	X62	268	X19
11	FX	54	X233	97	X190	140	X147	183	X104	226	X61	269	X18
12	OE1	55	X232	98	X189	141	X146	184	X103	227	X60	270	X17
13	OE2	56	X231	99	X188	142	X145	185	X102	228	X59	271	X16
14	OE3	57	X230	100	X187	143	X144	186	X101	229	X58	272	X15
15	DIO2	58	X229	101	X186	144	X143	187	X100	230	X57	273	X14
16	XDON	59	X228	102	X185	145	X142	188	X99	231	X56	274	X13
17	V_{DD}	60	X227	103	X184	146	X141	189	X98	232	X55	275	X12
18	V_{GG}	61	X226	104	X183	147	X140	190	X97	233	X54	276	X11
19	COM6	62	X225	105	X182	148	X139	191	X96	234	X53	277	X10
20	COM7	63	X224	106	X181	149	X138	192	X95	235	X52	278	X9
21	COM8	64	X223	107	X180	150	X137	193	X94	236	X51	279	X8
22	COM9	65	X222	108	X179	151	X136	194	X93	237	X50	280	X7
23	COM10	66	X221	109	X178	152	X135	195	X92	238	X49	281	X6
24	Dummy	67	X220	110	X177	153	X134	196	X91	239	X48	282	X5
25	Dummy	68	X219	111	X176	154	X133	197	X90	240	X47	283	X4
26	COM10	69	X218	112	X175	155	X132	198	X89	241	X46	284	X3
27	COM9	70	X217	113	X174	156	X131	199	X88	242	X45	285	X2
28	COM8	71	X216	114	X173	157	X130	200	X87	243	X44	286	X1
29	COM7	72	X215	115	X172	158	X129	201	X86	244	X43	287	COM5
30	COM6	73	X214	116	X171	159	X128	202	X85	245	X42	288	COM4
31	X256	74	X213	117	X170	160	X127	203	X84	246	X41	289	COM3
32	X255	75	X212	118	X169	161	X126	204	X83	247	X40	290	COM2
33	X254	76	X211	119	X168	162	X125	205	X82	248	X39	291	COM1
34	X253	77	X210	120	X167	163	X124	206	X81	249	X38	292	Dummy
35	X252	78	X209	121	X166	164	X123	207	X80	250	X37	293	Dummy
36	X251	79	X208	122	X165	165	X122	208	X79	251	X36		
37	X250	80	X207	123	X164	166	X121	209	X78	252	X35		
38	X249	81	X206	124	X163	167	X120	210	X77	253	X34		
39	X248	82	X205	125	X162	168	X119	211	X76	254	X33		
40	X247	83	X204	126	X161	169	X118	212	X75	255	X32		
41	X246	84	X203	127	X160	170	X117	213	X74	256	X31		
42	X245	85	X202	128	X159	171	X116	214	X73	257	X30		
43	X244	86	X201	129	X158	172	X115	215	X72	258	X29		

PINNING INFORMATION

Table 1. Pin description

PIN NO	SYMBOL	I/O	Function	DESCRIPTION		
286 to 31	X_1-X_{256}	O	TFT gate driver output	Under the control of the shift register data, OE1 or OE2 or OE3, and DIO1 or DIO2, the driver outputs are V_{GG} or V_{OFF} and change their value at the rising edge of FX		
6	V_{OFF}		Supply	Power supply for TFT driver output low level		
7	V_{EE}		Supply	Negative power supply for Level shifters. Chip ground		
8	V_{SS}		Supply	Logic ground, Reference of the voltages		
10	RL	I	Shift direction selection signal	RL = "H" : X1 → X256 (Shift left) RL = "L" : X256 → X1 (Shift right)		
9, 15	DIO1 DIO2	I/O	Start pulse input and output		**DIO1**	**DIO2**
				RL = "H"	Input	Output
				RL = "L"	Output	Input
16	XDON	I	Negative active input pin	When XDON = "L" then the driver outputs are at the V_{GG} level independant of any other input or register value.		
11	FX	I	Shift register clock input	The start pulse is sampled at the rising edge of FX, The carry pulse changes at the falling edge of FX.		
12 to14	OE1 OE2 OE3	I	Negative active input pin	When OE_N = "H" then the associated outputs are set to V_{OFF} independent of the register data. This function is not synchronized with FX.		
17	V_{DD}		Supply	Logic positive power		
18	V_{GG}		Supply	High voltage power and TFT driver output high level		

FUNCTIONAL DESCRIPTION

Power supply's

The TFT voltage is relative to the logic ground, it can be a negative voltage value.

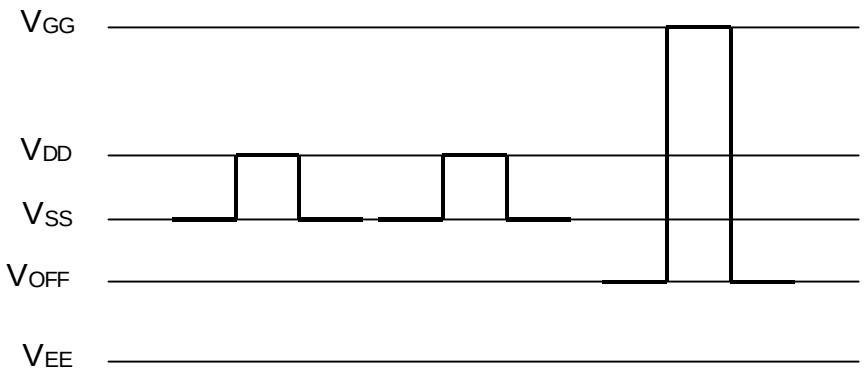

Fig. 3. Relative position of the different supply voltages

Shift direction

The input signals OE1,2,3 and the shift data control the value of the outputs (X_1 till X_{256}). Their value can be either V_{GG} or V_{OFF}.

The signal LR controls the shift direction of the shift register. The shift register takes its value from one of the input/output pins DIO at the rising edge of the clock FX and shifts the value to the other input/output pin DIO where it is presented at the falling edge of FX.

Table 2. RL shift direction relation

RL	Start pulse taken from:	Data shift direction	Output pulse given at:
RL="H"	DIO1	$X_1 \rightarrow X_{256}$	DIO2
RL="L"	DIO2	$X_{256} \rightarrow X_1$	DIO1

OE function

When the OE1, OE2, OE3 inputs are "H" than the outputs are driven to V_{OFF} regardless of the contents of the shift register. Each of the three inputs drives it own set of outputs. This function is not synchronized with FX. The signal XDON can override this function. In the Table below the relation between each OE1,2,3 and their related outputs is given.

Table 3. OE1,2,3 to Output relation

Non-signal input	Symbol	LCD driver outputs
OE1	X(3i+1) i =0~85	$X_1,X_4,X_7,X_{10},\cdots,X_{247},X_{250},X_{253},X_{256}$
OE2	X(3i+2) i =0~84	$X_2,X_5,X_8,X_{11},\cdots,X_{248},X_{251},X_{254}$
OE3	X(3i+3) i =0~84	$X_3,X_6,X_9,X_{12},\cdots,X_{249},X_{252},X_{255}$

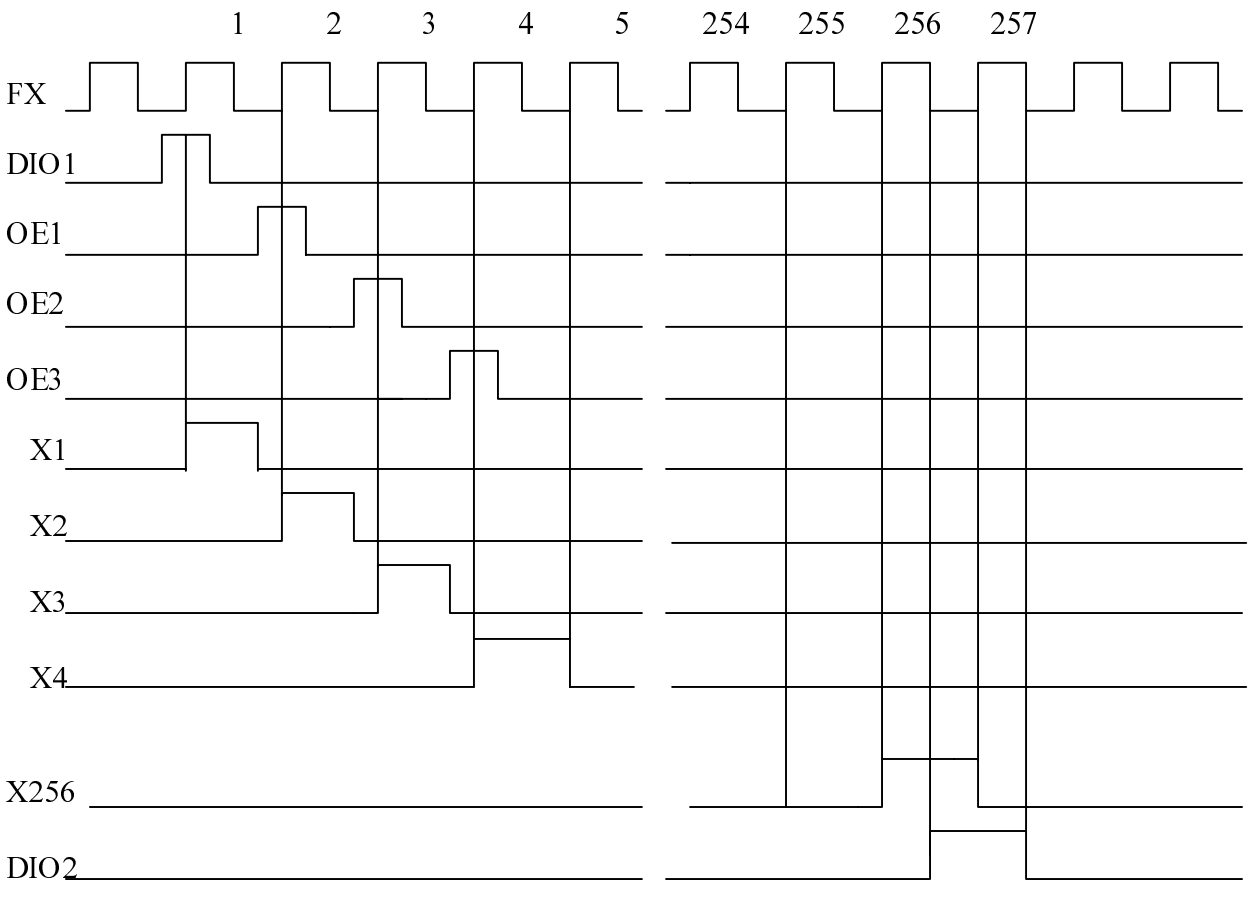

Fig. 4. OEn Functionality RL= "H"

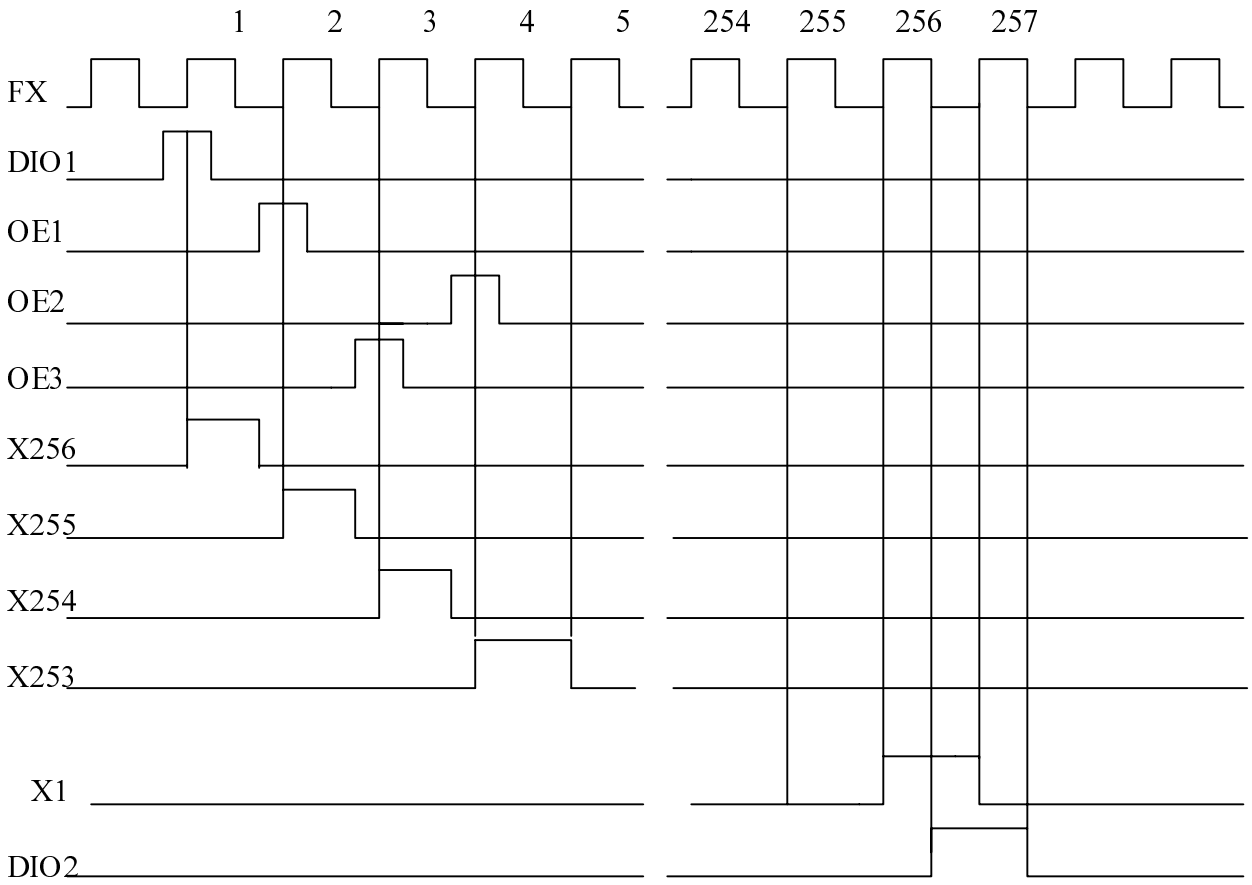

Fig. 5. OEn Functionality RL= "L"

XDON function

When XDON input is "L" then all outputs are driven to the V_{GG} level. This function is overriding all other inputs. With this input all TFT gates are set to high to enable a display off function. This function is not synchronized with FX.

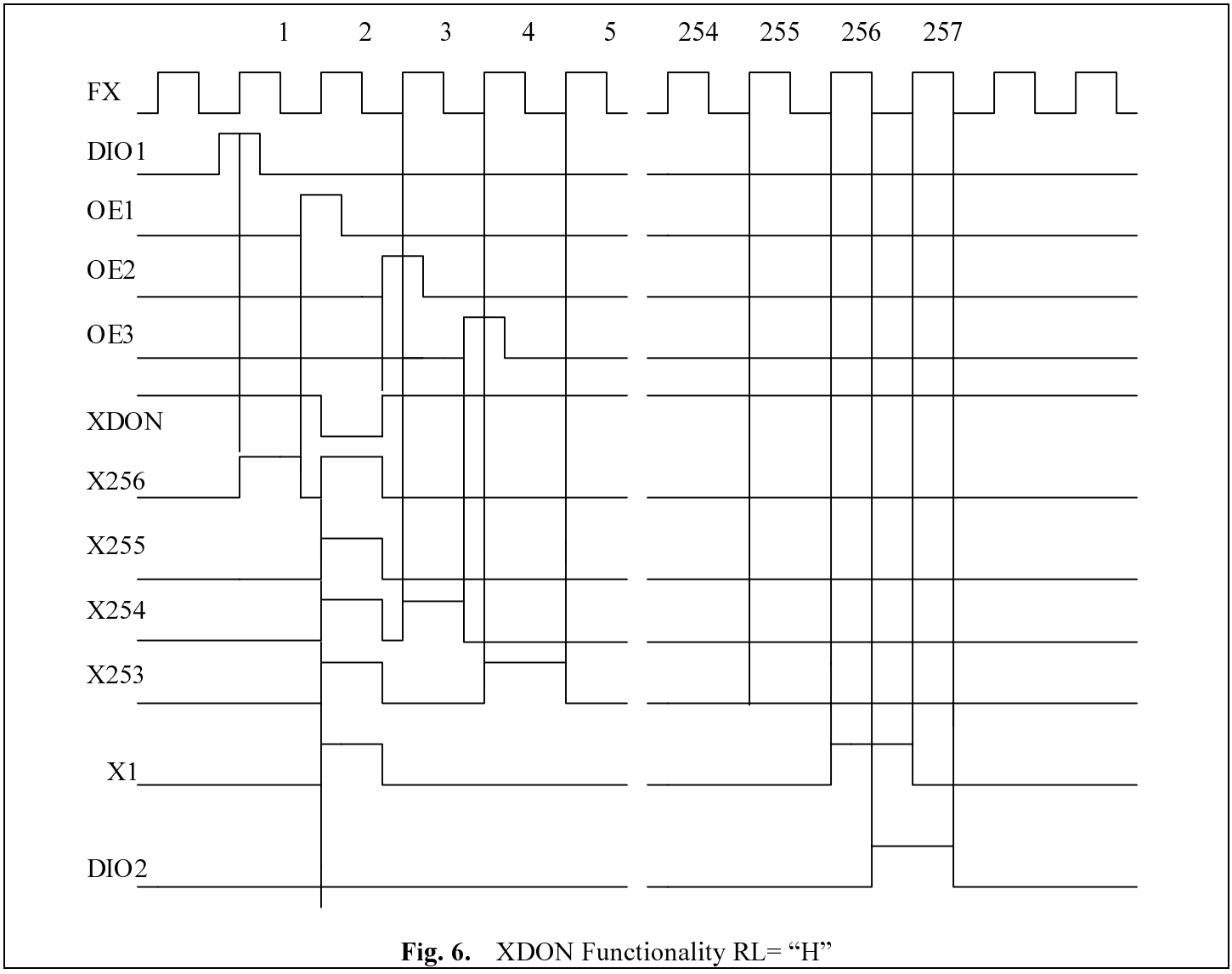

Fig. 6. XDON Functionality RL= "H"

CIRCUIT DIAGRAMS

Input/Output Circuit

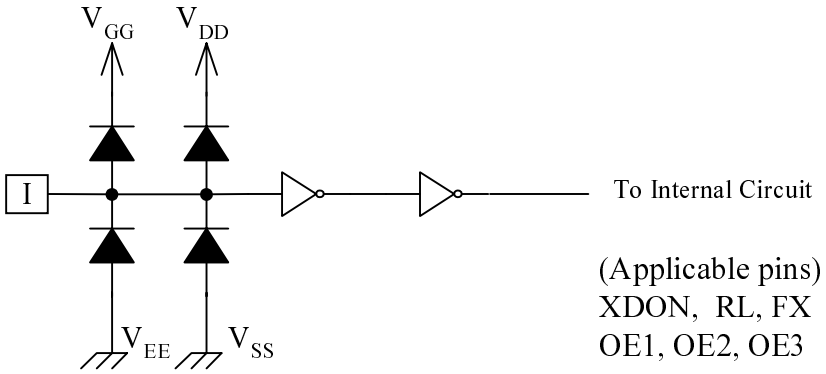

Fig. 7. Input Circuit

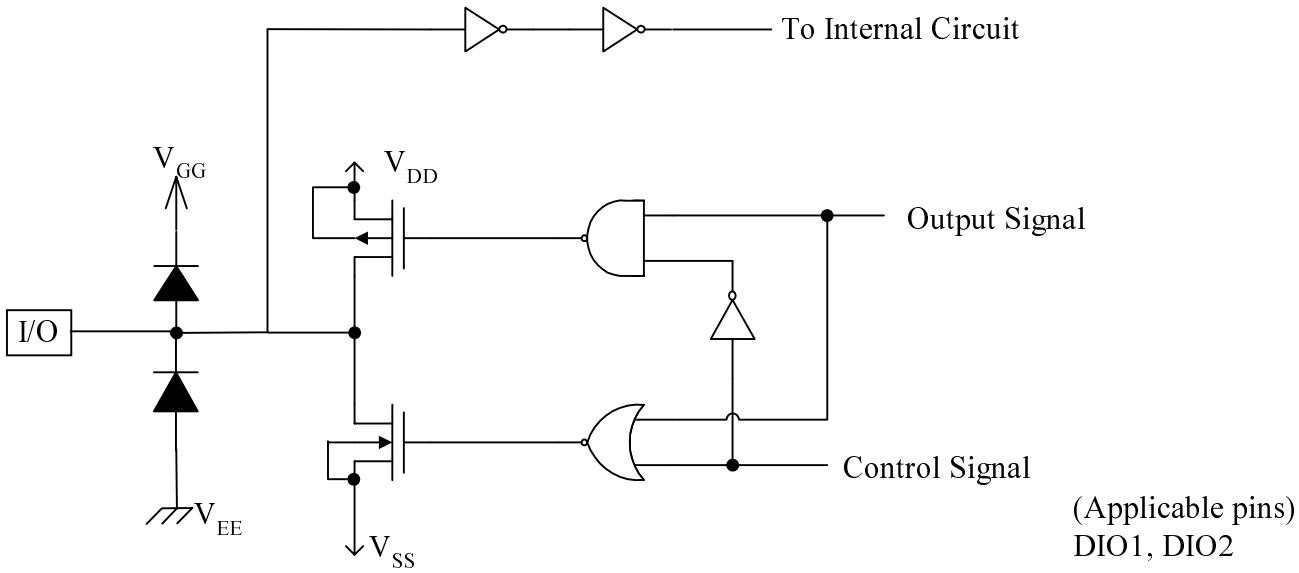

Fig. 8. Input/Output Circuit(1)

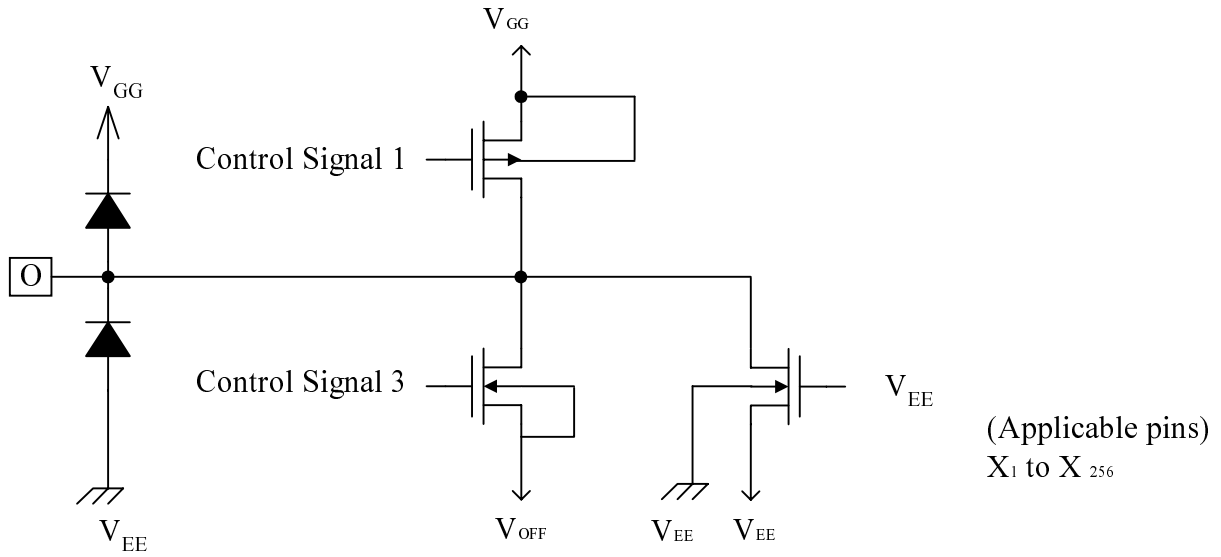

Fig. 9. TFT driver circuit

PRECAUTIONS

Precaution when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD driver power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute maximum Ratings

In accordance with the Absolute Maximum Ratings System (IEC 134); See notes 1 and 2

Parameter	Symbol	Applicable Pins	Ratings	Unit	NOTE
Supply voltage(1)	V_{DD}	V_{DD}	V_{SS} -0.3 to +7.0	V	1, 2
Supply voltage(2)	V_{GG}	V_{GG}	-0.3 to +45.0	V	
	V_{EE}	V_{EE}	V_{GG} -45 to V_{GG}+0.3	V	
	V_{OFF}	V_{OFF}	V_{EE} -0.3 to V_{GG}+0.3	V	
	V_{DD}	V_{DD}	V_{EE} -0.3 to V_{GG}+0.3	V	
	V_{SS}	V_{SS}	V_{EE} -0.3 to V_{GG}+0.3	V	
Input voltage	V_I	EO1, EO2, EO3, DIO1 DIO2, RL, FX, XDON	V_{SS} -0.3 to V_{DD}+0.3 V_{EE} -0.3 to V_{GG}+0.3	V	
Storage temperature	T_{stg}		-45 to +125	℃	

Notes:

1. Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device
2. Parameters are valid over operating temperature range unless otherwise specified.

RECOMMENDED OPERATING CONDITIONS

Table 5. Recommended operating conditions

Parameter	Symbol	Applicable pins	Min.	Typ.	Max.	Unit	NOTE
Supply voltage(1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage(2)	V_{GG}	V_{GG}	+10.0		+42.0	V	
Supply voltage(2)	V_{EE}	V_{EE}	-25		-5	V	
Operating temperature	T_{OPR}		-20		+75	℃	

Notes:

1. All voltages are with respect to V_{SS} unless otherwise noted (0 V).
2. Ensure that voltages are set such that $V_{EE} \le V_{SS} < V_{DD} < V_{GG}$. and $V_{EE} \le V_{OFF} < V_{GG}$

ELECTRICAL CHARACTERISTICS

Table 6. DC Characteristics

(V_{SS}=0 V, V_{DD}=+2.5V to +5.5V, V_{GG}=+15.0 to +42.0 V, T_{OPR}=-20 to +85℃)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit	Note
Operating Supply Current	I_{DD}	f_{FX}=15.7kHz f_{SL}=60Hz V_{DD}=3.3V V_{EE}=-15V V_{GG}=15V Output with no load	V_{DD}			800	μA	
Operating Supply Current	I_{GG}		V_{GG}			300	μA	
Standby quiescent supply current	I_{DS}	Standby V_{DD}=3.3V V_{EE}=-15V V_{GG}=15V	V_{DD}			600	μA	
Standby quiescent Supply Current	I_{GS}		V_{GG}			100	μA	
Input pin								
H input voltage	V_{IH1}		RL,FX, OE1~3, XDON	0.8xV_{DD}		V_{DD}	V	
L input voltage	V_{IL1}			0		0.2xV_{DD}	V	
Input leakage current	V_{LI1}			-10		10	μA	
Output pin								
H input voltage	V_{IH3}		DIO1, DIO2	0.8xV_{DD}		V_{DD}	V	
L input voltage	V_{IL3}					0.2xV_{DD}	V	
H output voltage	V_{OH}	I_O = -100 μA		V_{DD}-0.4			V	
L output voltage	V_{OL}	I_O = 100 μA				0.4	V	
Liquid crystal driving voltage input pin								
Input leakage current	V_{LI2}		V_{OFF}	-100		100	μA	
Liquid crystal driving output pin								
Output leakage current	V_{LO1}		X1~X256	-50		50	μA	
Output ON resistance	RON-V_{GG}	V_{GG}=15V V_{EE}=-15V V_{OM}=V_{GG}-0.5V V_{OM} is X1~X256			600	1000	Ω	
	RON-V_{OFF}	V_{GG}=15V V_{EE}=-15V V_{OFF}=-10v V_{OM}=V_{OFF}+0.5V V_{OM} is X1~X256			600	1000	Ω	

AC Characteristics

(V_{SS}= 0 V, V_{DD}=+2.5V to +5.5V, V_{GG}-V_{EE}=+30.0 to +42.0 V, T_{OPR}=-20 to +85℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock period	t_{FX}		833			ns
Pulse width of clock H level	t_{WH}		350			ns
Pulse width of clock L level	t_{WL}		350			ns
DIO data set up time	t_{su}		50			ns
DIO data hold time	th		350			ns
DIO output delay time	tpd1	CL=50pF			300	ns
Xn output delay time	tpd2	CL=300pF			800	ns

Timing Chart

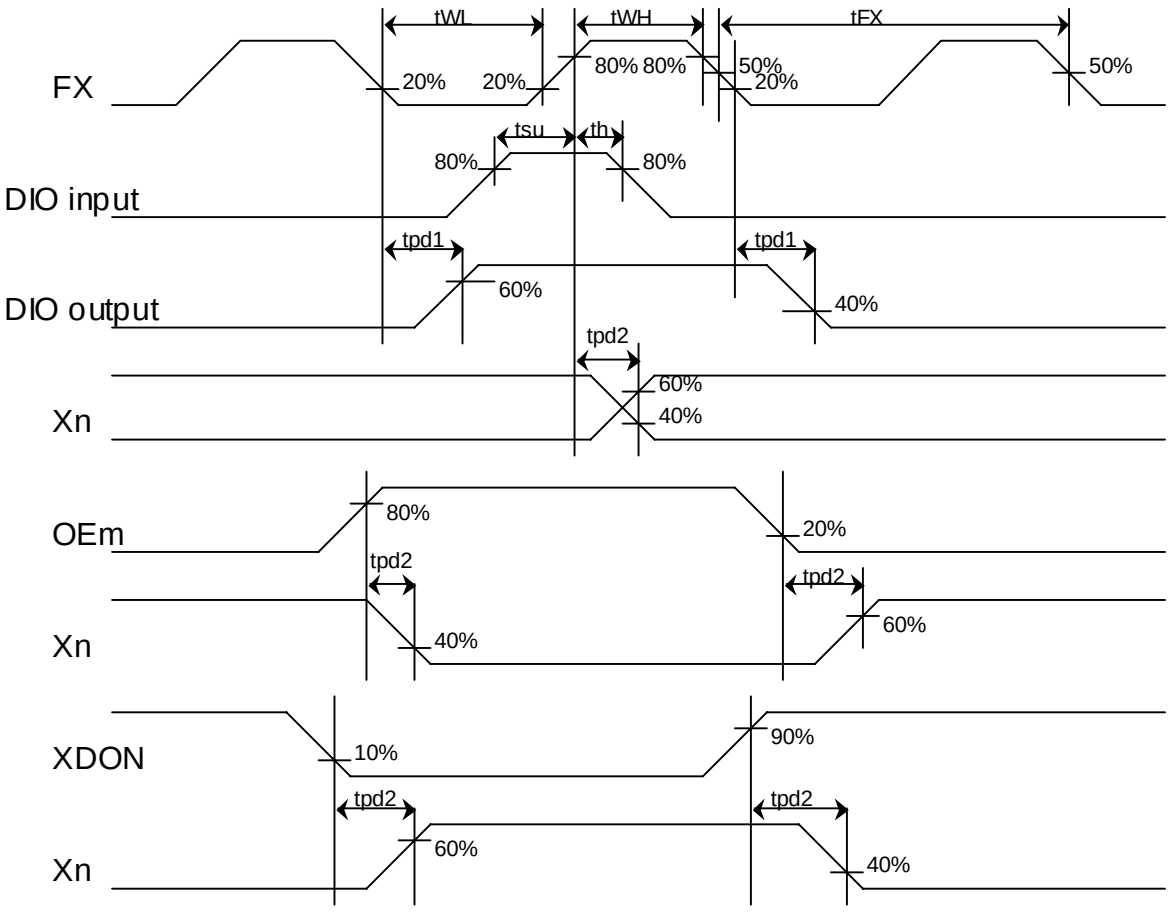

Fig. 10. Timing

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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