Description

The Edge4707 is a precision measurement unit designed for automatic test equipment and instrumentation. Manufactured in a wide voltage CMOS process, it is a monolithic solution for a quad channel per pin PMU.

Each channel of the Edge4707 features a PMU that can force or measure voltage over a 15V I/O range, and supports 4 current ranges: 2 µA, 200 µA, 20 µA, and 2 mA.

Each channel of the Edge4707 features an on-board window comparator that provides two bits of information: DUT too high and DUT too low. There is also a monitor function which provides a real time analog signal proportional to either the measured voltage or current.

The Edge4707 is designed to be a low power, low cost, small footprint solution to allow high pin count testers to support a PMU per pin.

In addition, two independent switches per channel (for a central PMU force and sense) plus two wide voltage analog muxes per channel are included.

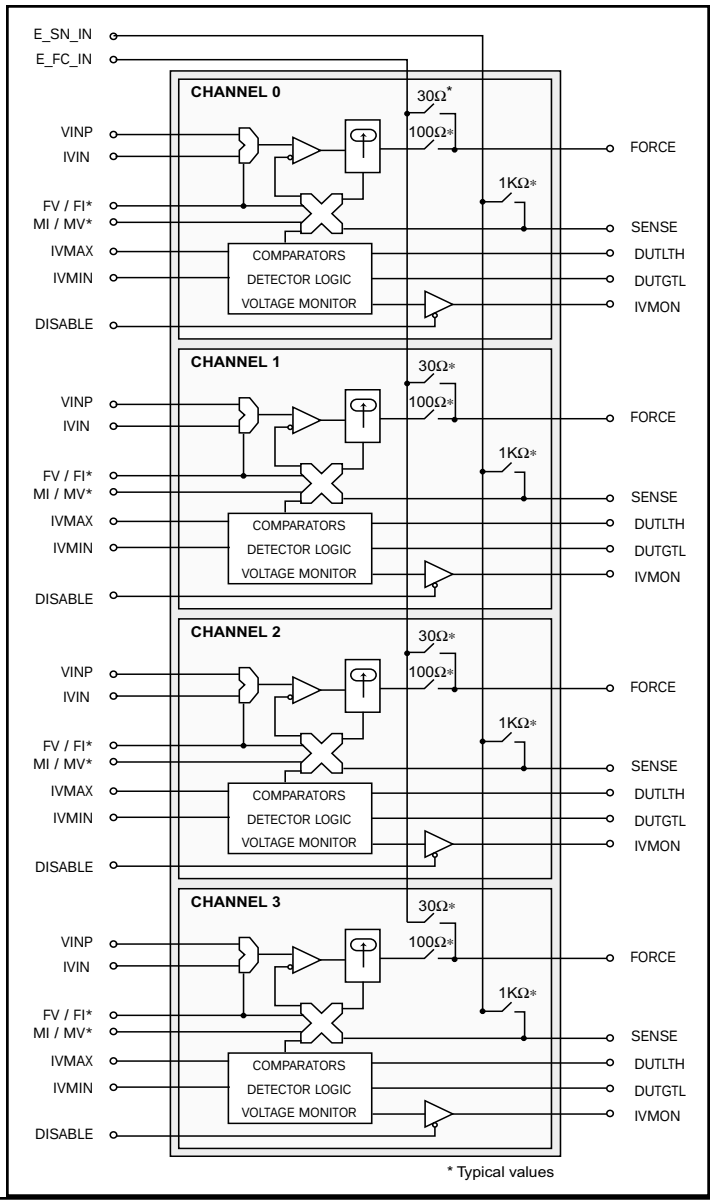
Applications

- Automated Test Equipment
  - Memory Testers
  - VLSI Testers
  - Mixed Signal Tester

Features

- FV / MI Capability
- FI / MV Capability
- FV / MV Capability
- FI / MI Capability
- 4 Current Ranges (2 µA, 20 µA, 200 µA, 2mA)
- –2V to +13V Output Range (Zero Current)
- 0V to 11V Output Range (Full Scale Current)
- FV Linearity to ± .025% FSR
- Central PMU Switches
- Per Pin Super Voltage Switches

Functional Block Diagram



PIN Description

Pin Name	Pin #	Description
VINP[0:3]	C2, F5, H3, L2	Analog voltage input which forces the output voltage (FV/MI mode) (one per channel).
IVIN[0:3]	C1, F2, H4, J5	Analog voltage input which forces the output current (FI/MV mode) (one per channel).
FORCE[0:3]	C14, F12, H13, L12	Analog output pin which forces current or voltage.
SENSE[0:3]	C13, G10, H14, K11	Analog input pin which senses voltage.
FV/FI*[0:3]	D10, B8, A6, E6	TTL compatible input which determines whether the PMU is forcing voltage or forcing current.
MI/MV*[0:3]	B10, A8, C6, D5	TTL compatible input which determines whether the PMU is measuring current or measuring voltage.
RS0[0:3] RS1[0:3]	B11, A9, C7, C5 A12, C10, D8, A5	TTL compatible current range select inputs.
IVMIN[0:3] IVMAX[0:3]	G5, E1, H2, K3 C3, E3, H1, L1	Analog input voltages which establish the lower and upper threshold level for the measurement comparator.
DUTLTH[0:3] DUTGTL[0:3]	P11, N9, N7, N5 N11, P9, P7, P5	Digital comparator output that indicates the DUT measurement is less than the upper threshold and greater than the lower threshold.
DISABLE[0:3]	A11, C9, D7, A4	TTL compatible input which places the IVMON outputs in high impedance.
E_SNSEL[0:3]	D11, E9, B7, B5	TTL switch select for the external SENSE switch for Channels 0–3.
E_SN_IN	L4	Analog output for external SENSE.
E_FC_IN	K5	Analog input for external FORCE signal.
E_FCSEL[0:3]	E10, B9, A7, D6	TTL switch select for the external FORCE switch for Channels 0–3.
I_FCSEL[0:3]	C11, D9, B6, B4	TTL switch select for internal FORCE switch for Channels 0–3.
RA[0:3], RB[0:3] RC[0:3], RD[0:3]	D13, G11, J14, K10 D14, G12, J13, L11 E12, G14, J10, M14 F11, G13, K12, M13	External resistor input corresponding to Ranges A through D.
RES_IN[0:3]	F10, F13, J12, L13	External resistor input. One side of the external resistors connect to RA[0:3], RB[0:3], RC[0:3], RD[0:3]. The other side of all resistors connect to RES_IN.

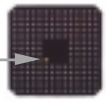
PIN Description *(continued)*

Pin Name	Pin #	Description
IVMON[0:3]	B1, E2, G4, J4	Analog voltage output that provides a real time monitor of either the measured voltage or measured current level.
COMP1[0:3] COMP2[0:3]	D4, F1, J2, K4 E5, F3, J1, M1	Internal compensation pins that require an external capacitor connected between the two pins.
COMP3[0:3]	D2, F4, J3, M2	Internal compensation pin that requires an external capacitor connected between the pin and ground.
COMP4[0:3]	D1, G2, H5, L3	Internal compensation pin that requires an external capacitor connected between the pin and the RES_IN pin.
Analog MUX Switches		
$V_{IH[0:3]}$	K9, M9, M7, M5	Driver High input.
$V_{IHH[0:3]}$	L10, K8, L7, K6	Super voltage input High.
$V_{IL[0:3]}$	L9, M8, M6, M4	Driver Low input.
$V_{ILH[0:3]}$	M10, L8, L6, L5	Super voltage input Low.
SVSEL[0:3]	A10, C8, E7, A3	Select for MUX.
DVH[0:3]	P10, N8, N6, N4	Output High.
DVL[0:3]	N10, P8, P6, P4	Output Low.
Power Pins		
VCC[1:4]	A1, D12, E4, E14, G3, H12, K2, K13	Positive analog power supply.
VDD	P3	Positive digital supply.
VEE[1:4]	D3, E13, G1, H11, K1, K14, M12, N1	Negative analog power supply.
GND[1:4]	E11, F14, J11, L14	Ground.

PIN Description *(continued)*

Bottom View

A1 Ball Pad Indicator



12 mm X 12 mm 180 FLEXBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	P1	P2	P3 VDD	P4 DVL3	P5 DUTGTL3	P6 DVL2	P7 DUTGTL2	P8 DVL1	P9 DUTGTL1	P10 DVH0	P11 DUTLTH0	P12	P13	P14
N	N1 VEE4	N2	N3	N4 DVH3	N5 DUTLTH3	N6 DVH2	N7 DUTLTH2	N8 DVH1	N9 DUTLTH1	N10 DVL0	N11 DUTGTL0	N12	N13	N14
M	M1 COMP2_3	M2 COMP3_3	M3	M4 VIL3	M5 VIH3	M6 VIL2	M7 VIH2	M8 VIL1	M9 VIH1	M10 VILH0	M11	M12 VEE4	M13 RD3	M14 RC3
L	L1 IVMAX3	L2 VINP3	L3 COMP4_3	L4 E_SN_IN	L5 VILH3	L6 VILH2	L7 VIHH2	L8 VILH1	L9 VIL0	L10 VIHH0	L11 RB3	L12 FORCE3	L13 RESIN3	L14 GND4
K	K1 VEE3	K2 VCC4	K3 IVMIN3	K4 COMP1_3	K5 E_FC_IN	K6 VIHH3	K7	K8 VIHH1	K9 VIH0	K10 RA3	K11 SENSE3	K12 RD2	K13 VCC4	K14 VEE3
J	J1 COMP2_2	J2 COMP1_2	J3 COMP3_2	J4 IVMON3	J5 IVIN3	J6	J7	J8	J9	J10 RC2	J11 GND3	J12 RESIN2	J13 RB2	J14 RA2
H	H1 IVMAX2	H2 IVMIN2	H3 VINP2	H4 IVIN2	H5 COMP4_2	H6	H7	H8	H9	H10	H11 VEE2	H12 VCC3	H13 FORCE2	H14 SENSE2
G	G1 VEE2	G2 COMP4_1	G3 VCC3	G4 IVMON2	G5 IVMIN0	G6	G7	G8	G9	G10 SENSE1	G11 RA1	G12 RB1	G13 RD1	G14 RC1
F	F1 COMP1_1	F2 IVIN1	F3 COMP2_1	F4 COMP3_1	F5 VINP1	F6	F7	F8	F9	F10 RESIN0	F11 RD0	F12 FORCE1	F13 RESIN1	F14 GND2
E	E1 IVMIN1	E2 IVMON1	E3 IVMAX1	E4 VCC2	E5 COMP2_0	E6 FV/FI*3	E7 SVSEL2	E8	E9 E_SNSEL1	E10 E_FCSEL0	E11 GND1	E12 RC0	E13 VEE1	E14 VCC2
D	D1 COMP4_0	D2 COMP3_0	D3 VEE1	D4 COMP1_0	D5 MI/MV*3	D6 E_FCSEL3	D7 DISABLE2	D8 RS1_2	D9 I_FCSEL1	D10 FV/FI*0	D11 E_SNSEL0	D12 VCC1	D13 RA0	D14 RB0
C	C1 IVIN0	C2 VINP0	C3 IVMAX0	C4	C5 RS0_3	C6 MI/MV*2	C7 RS0_2	C8 SVSEL1	C9 DISABLE1	C10 RS1_1	C11 I_FCSEL0	C12	C13 SENSE0	C14 FORCE0
B	B1 IVMON0	B2	B3	B4 I_FCSEL3	B5 E_SNSEL3	B6 I_FCSEL2	B7 E_SNSEL2	B8 FV/FI*1	B9 E_FCSEL1	B10 MI/MV*0	B11 RS0_0	B12	B13	B14
A	A1 VCC1	A2	A3 SVSEL3	A4 DISABLE3	A5 RS1_3	A6 FV/FI*2	A7 E_FCSEL2	A8 MI/MV*1	A9 RS0_1	A10 SVSEL0	A11 DISABLE0	A12 RS1_0	A13	A14

A1 Ball Pad Corner Indicator (No Solder Ball)

PIN Description *(continued)*

A1 Ball Pad Indicator

Top View

12 mm X 12 mm 180 FLEXBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	A1 VCC1	A2	A3 SVSEL3	A4 DISABLE3	A5 RS1_3	A6 FV/FI*2	A7 E_FCSEL2	A8 MI/MV*1	A9 RS0_1	A10 SVSEL0	A11 DISABLE0	A12 RS1_0	A13	A14
B	B1 IVMON0	B2	B3	B4 I_FCSEL3	B5 E_SNSEL3	B6 I_FCSEL2	B7 E_SNSEL2	B8 FV/FI*1	B9 E_FCSEL1	B10 MI/MV*0	B11 RS0_0	B12	B13	B14
C	C1 IVIN0	C2 VINP0	C3 IVMAX0	C4	C5 RS0_3	C6 MI/MV*2	C7 RS0_2	C8 SVSEL1	C9 DISABLE1	C10 RS1_1	C11 I_FCSEL0	C12	C13 SENSE0	C14 FORCE0
D	D1 COMP4_0	D2 COMP3_0	D3 VEE1	D4 COMP1_0	D5 MI/MV*3	D6 E_FCSEL3	D7 DISABLE2	D8 RS1_2	D9 I_FCSEL1	D10 FV/FI*0	D11 E_SNSEL0	D12 VCC1	D13 RA0	D14 RB0
E	E1 IVMIN1	E2 IVMON1	E3 IVMAX1	E4 VCC2	E5 COMP2_0	E6 FV/FI*3	E7 SVSEL2	E8	E9 E_SNSEL1	E10 E_FCSEL0	E11 GND1	E12 RC0	E13 VEE1	E14 VCC2
F	F1 COMP1_1	F2 IVIN1	F3 COMP2_1	F4 COMP3_1	F5 VINP1	F6	F7	F8	F9	F10 RESIN0	F11 RD0	F12 FORCE1	F13 RESIN1	F14 GND2
G	G1 VEE2	G2 COMP4_1	G3 VCC3	G4 IVMON2	G5 IVMIN0	G6	G7	G8	G9	G10 SENSE1	G11 RA1	G12 RB1	G13 RD1	G14 RC1
H	H1 IVMAX2	H2 IVMIN2	H3 VINP2	H4 IVIN2	H5 COMP4_2	H6	H7	H8	H9	H10	H11 VEE2	H12 VCC3	H13 FORCE2	H14 SENSE2
J	J1 COMP2_2	J2 COMP1_2	J3 COMP3_2	J4 IVMON3	J5 IVIN3	J6	J7	J8	J9	J10 RC2	J11 GND3	J12 RESIN2	J13 RB2	J14 RA2
K	K1 VEE3	K2 VCC4	K3 IVMIN3	K4 COMP1_3	K5 E_FC_IN	K6 VIHH3	K7	K8 VIHH1	K9 VIH0	K10 RA3	K11 SENSE3	K12 RD2	K13 VCC4	K14 VEE3
L	L1 IVMAX3	L2 VINP3	L3 COMP4_3	L4 E_SN_IN	L5 VILH3	L6 VILH2	L7 VIHH2	L8 VILH1	L9 VIL0	L10 VIHH0	L11 RB3	L12 FORCE3	L13 RESIN3	L14 GND4
M	M1 COMP2_3	M2 COMP3_3	M3	M4 VIL3	M5 VIH3	M6 VIL2	M7 VIH2	M8 VIL1	M9 VIH1	M10 VILH0	M11	M12 VEE4	M13 RD3	M14 RC3
N	N1 VEE4	N2	N3	N4 DVH3	N5 DUTLTH3	N6 DVH2	N7 DUTLTH2	N8 DVH1	N9 DUTLTH1	N10 DVL0	N11 DUTGTL0	N12	N13	N14
P	P1	P2	P3 VDD	P4 DVL3	P5 DUTGTL3	P6 DVL2	P7 DUTGTL2	P8 DVL1	P9 DUTGTL1	P10 DVH0	P11 DUTLTH0	P12	P13	P14

A1 Ball Pad Corner Indicator (No Solder Ball)

Circuit Description

Circuit Overview

The Edge4707 is a quad channel parametric test and measurement unit that can :

- Force Voltage / Measure Current
- Force Current / Measure Voltage
- Force Voltage / Measure Voltage
- Force Current / Measure Current

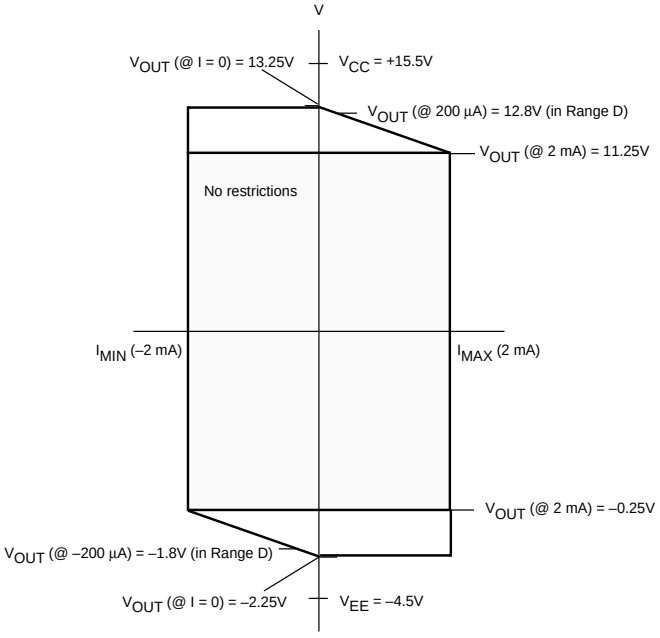
Each PMU channel can force or measure voltage over a 15V range and force or measure current over four distinct ranges:

- ± 2 µA
- ± 20 µA
- ± 200 µA
- ± 2 mA.

An on-board window comparator provides two bit output range classification. Also, a monitor passes a real time analog voltage which tracks either the measured current or voltage.

PPMU Functionality

The trapezoid in Figure 1 describes the current-voltage functionality of the PMU with VCC = 15.5V and VEE = –4.5V, *in Range D.*



NOTE: Negative current implies current is flowing into the 4707 from DUT.

Figure 1. PMU Functionality

Control Inputs

FV/FI* is a TTL compatible input which determines whether the PMU forces voltage or current, and MI/MV* is a TTL compatible input which determines whether the PMU measures current or voltage. FV/FI* and MI/MV* are independent for each PMU. Table 1 describes the modes of operation controlled by these pins.

FV / FI*	MI/MV*	Mode of Operation
0	0	Force Current, Measure Voltage
0	1	Force Current, Measure Current
1	0	Force Voltage, Measure Voltage
1	1	Force Voltage, Measure Current

Table 1.

RS0 and RS1 are TTL compatible inputs to an internal analog mux which selects an external resistor corresponding to a desired current range. The truth table for RS0 to RS1, along with the associated external resistor values and current ranges, is shown in Table 2. RS0 and RS1 are independent for each channel of the 4707.

RS1	RS0	Range	Current Range	"Nominal" Ext. R
0	0	A	± 2 µA	RA = 1MΩ
0	1	B	± 20 µA	RB = 100KΩ
1	0	C	± 200 µA	RC = 10KΩ
1	1	D	± 2 mA	RD = 1KΩ

Table 2.

FORCE/SENSE

FORCE is an analog output which either forces a current or forces a voltage, depending on which operating mode is selected.

SENSE is a high impedance analog input which measures the DUT voltage input in the MV operating mode.

FORCE and SENSE are brought out to separate pins to allow remote sensing.

Circuit Description *(continued)*

IVMON

IVMON is a real time analog voltage output which tracks the sensed parameter.

In the MV mode, the output voltage displayed at IVMON is a 1:1 mapping of the SENSE voltage. In the MI mode, IVMON follows the equation:

$$IVMON = I(measured) * REXT$$

Using nominal values for the external resistors (RA, RB, RC, and RD), a voltage at IVMON of +2V corresponds to Imax and –2V corresponds to Imin of the selected current range.

The IVMON pin can also be placed into a high impedance state by using the DISABLE input (see Table 3).

Disable	MI / MV*	Sensed Parameter
1	X	High Impedance
0	0	Measured Voltage
0	1	Measured Current

Table 3.

Force Voltage Mode

In the FV mode (FV/FI* = 1), VINP is a high impedance analog voltage input that maps directly to the voltage forced at the FORCE pin.

Measure Current Mode

In the MI mode (MI/MV* = 1), a current monitor is connected in series with the PMU forcing amplifier. This monitor generates a voltage that is proportional to the current passing through it, and is brought out to IVMON. This voltage (corresponding to the measured current) is also tested by the on-board window comparator.

Force Current Mode (see page 15)

In the FI mode (FV/FI* = 0), IVIN is a high impedance analog voltage input that is converted into a current at the FORCE pin using the following relationship:

$$Forced\ Current = IVIN / REXT$$

(Positive current is defined as current flowing out of the FORCE pin.) The IVIN input voltage range and forced current (at FORCE) can be seen in Table 4.

IVIN	Corresponding Forced Current
+2V	Imax (full scale)
0V	0
–2V	Imin (full scale)

Table 4.

Measure Voltage Mode

In the MV mode (MI/MV* = 0), DUT voltage is measured via the SENSE input pin. Note that EXT_SENSE_SEL = 0 when the Edge4707 SENSE is used. This measured voltage is also tested with the on-board window comparator.

Comparator

The Edge4707 features an on-board window comparator which provides two-bit measurement range classification. IVMAX and IVMIN are high impedance analog inputs that establish the upper and lower thresholds for the window comparator.

In the MI mode, an I/V MAX input of +2V will set the upper threshold of the window comparator to a voltage corresponding to +FSC (full-scale current), and an I/V MIN input of –2V will set the lower threshold to a voltage corresponding to –FSC (positive current is defined as current flowing out of the PMU).

DUTGTL the DUTLTH are LVTTL compatible outputs which indicate the range of the measured parameter in relation to IVMIN and IVMAX. Comparator functionality is summarized in Table 5 for MI Mode and Table 6 for MV mode.

TEST CONDITION	DUT LTH	DUT GTL
IVMON > IVMAX IVMON < IVMAX	0 1	N/A
IVMON > IVMIN IVMON < IVMIN	N/A	1 0
IVMON < IVMAX and IVMON > IVMIN	1	1

Table 5. MI Comparator Truth Table

TEST CONDITION	DUT LTH	DUT GTL
SENSE > IVMAX SENSE < IVMAX	0 1	N/A
SENSE > IVMIN SENSE < IVMIN	N/A	1 0
SENSE < IVMAX and SENSE >IVMIN	1	1

Table 6. MV Comparator Truth Table

Circuit Description *(continued)*

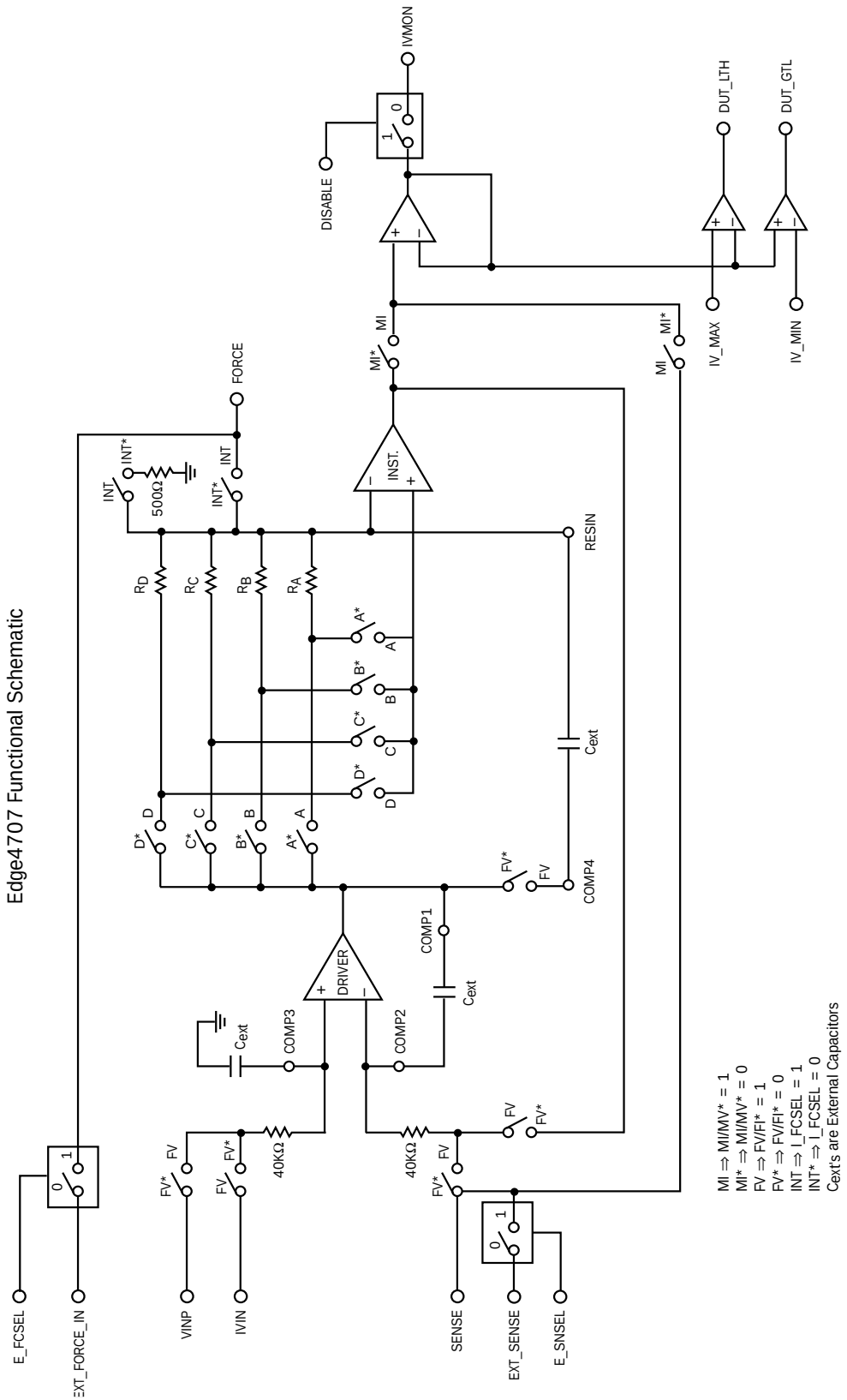


Figure 2. Edge4707 Functional Schematic

Circuit Description *(continued)*

REXT Selection

The Edge 4707 is designed for the voltage drop across RA, RB, RC, and RD to be ≤ 2V with the maximum current passing through them. However, these resistor values can be changed to support different applications.

Increasing the maximum current beyond the nominal range is not recommended. However, decreasing the maximum current is allowed by increasing the external resistor using the equation IMAX = 2V / REXT.

Switch Operation on Force and Sense Lines

Each channel of the Edge4707 features two switches connected to the FORCE output pin (External Force = 30Ω, Internal Force = 100Ω) and one 1KΩ switch connected to the SENSE input pin. These switches are controlled by the TTL compatible inputs I_FCSEL, E_FCSEL, and E_SNSEL. Switch operation is described in Table 7.

Switch	Switch Select Name	Open/Close State on Switch
100Ω, to internal force circuitry	I_FCSEL	0 = Open 1 = Closed
30Ω, to external force circuitry	E_FCSEL	0 = Open 1 = Closed
1KΩ, to external sense circuitry	E_SNSEL	0 = Open 1 = Closed

Table 7.

These switches can be configured to route the Edge4707 for external forcing or sensing operations (see Figure 2). For external forcing operation, the switch controlled by I_FCSEL can be used to internally isolate the PMU from the FORCE output. This enables the user to connect the FORCE pin to an external device connected to the E_FC_IN pin using the switch controlled by the E_FC_SEL input. I_FCSEL and E_FCSEL functionality is described in Table 8.

I_FCSEL	E_FCSEL	FORCE
0	0	HiZ
1	1	Illegal Condition
1	0	VINP
0	1	E_FC_IN

Table 8.

For external sense operation, the switch controlled by E_SNSEL can be used to internally connect the SENSE input pin to the E_SN_IN output pin (see Figure 2). This allows the user to use the E_SN_IN pin for remote sensing.

Analog MUX

The Edge4707 has a separate analog mux section which is intended for 12V flash programming signal muxing with lower, more standard voltages. There are five inputs for this section, all of which are brought out to external pins (see Figure 3). The two outputs, DVH and DVL, connect to driver reference voltages of the Edge720 (or other pin electronics drivers).

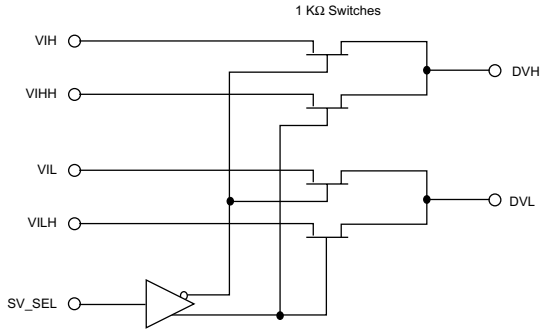


Figure 3. Analog MUX Section
(Typically used to provide flash programming and standard voltages to driver pin electronic references.)

The truth table for SV-SEL is shown in Table 9.

SV_SEL	
0	DVH = VIH DVL = VIL
1	DVH = VIHH DVL = VILH (supervoltage)

Table 9. SV-SEL Truth Table

Circuit Description *(continued)*

Short Circuit Protection

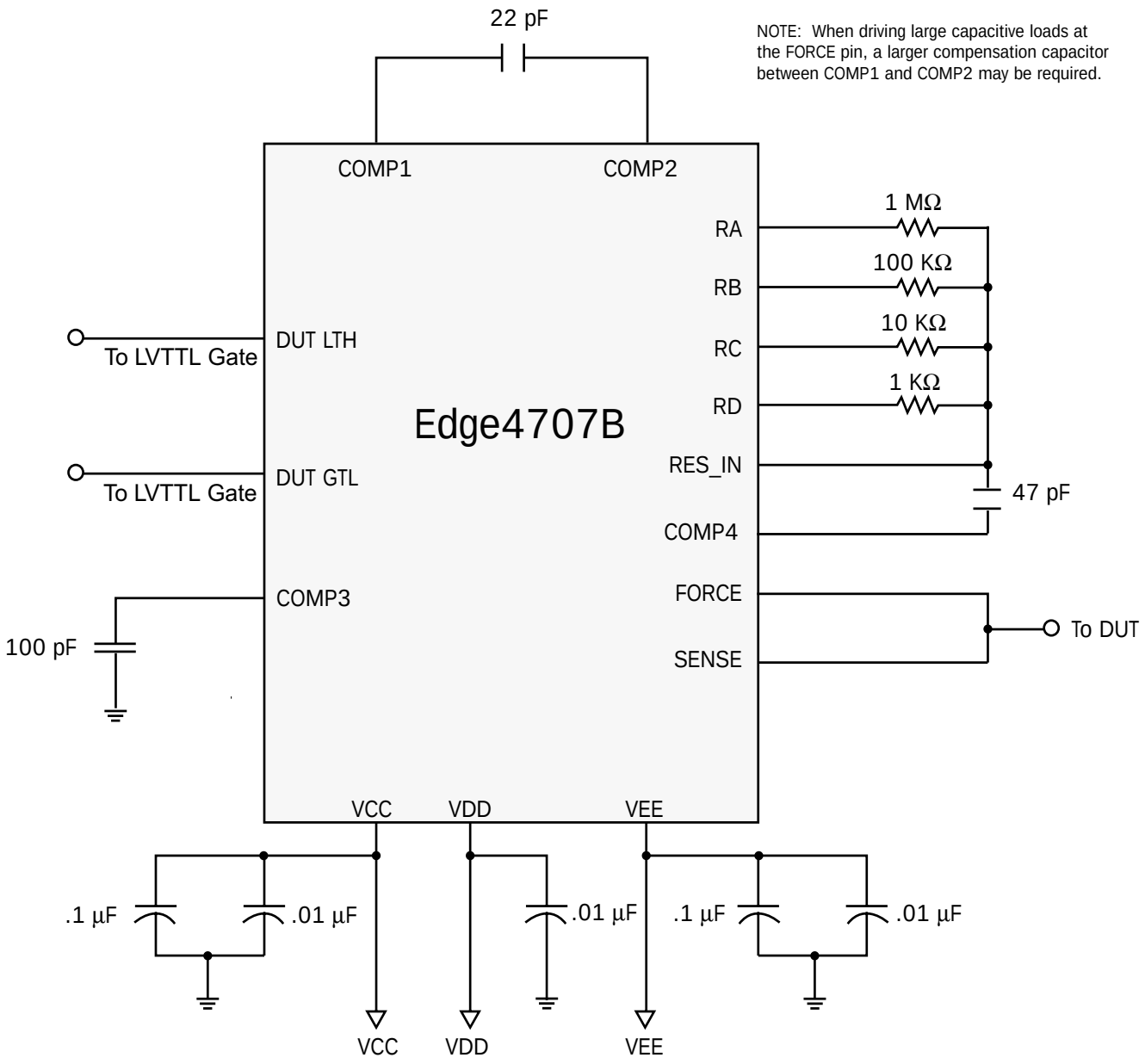
The Edge 4707 is designed to survive a direct short circuit to any legal voltage at the FORCE and SENSE pins, by virtue of a limited current, which results from the presence of an external current sense resistor (normally 1 KΩ to 1MΩ) in the FORCE path.

Transient Clamps

The Edge 4707 has on-board clamps to limit the voltage and current spikes that might result from either changing the current range or changing the operating mode.

Application Information

Required External Components (Per Channel)



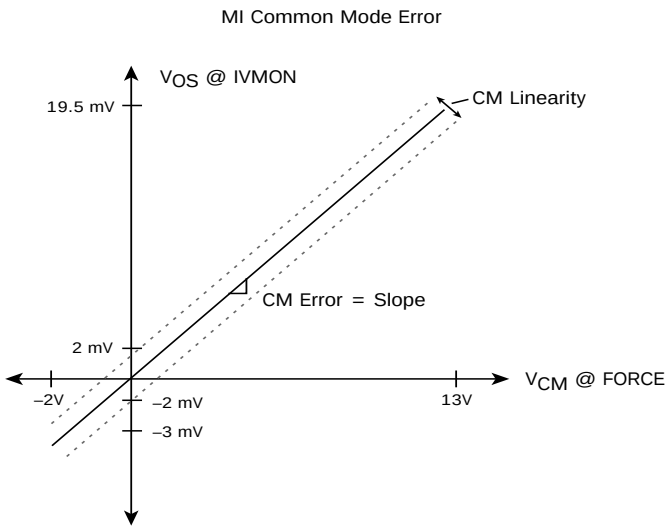
Actual decoupling capacitor values depend on the system environment.

Application Information *(continued)*

Calibration

In order to attain a high degree of accuracy in a typical ATE application, offset and gain errors are accounted for through software calibration. When operating the Edge4707 in the Measure Current (MI) or Force Current (FI) modes, an additional source of error, common mode error, should be accounted for. Common mode error is a measure of how the common mode voltage, V_{CM}, at the input of the current sense amplifier affects the forced or measured current values (see Figure 4). Since this error is created by internal resistors in the current sense amplifier, it is very linear in nature.

Using the common mode error and common mode linearity specifications, one can see that with a small number of calibration steps (see Applications note E4707-A1), the effect of this error can be significantly reduced.



NOTE: In some cases, slope may be negative.

Figure 4. Graphical Representation of Common Mode Error

Maximum Input Voltage Range for FV Mode

In order to ensure that the full-scale output voltage range (FSV) can be achieved by the 4707, errors such as gain, linearity, and offset must be taken into account when determining the input voltage range required at VINP. The equations in Table 10 can be used to determine the input voltage range required at VINP to achieve full scale voltage (FSV) at the FORCE pin.

VINP (Worst Case)	FORCE
$\frac{FSV}{Gain}$ + V_{OS} + LInearity Error	+ FSV
$\frac{-FSV}{Gain}$ + V_{OS} + LInearity Error	– FSV

Table 10.

Example: If it is desired to operate the 4707 with a FV range of –2V to 13V, the VINP input voltages in Table 11 may be required.

VINP	FORCE
13.3V	+13V
–2.13V	–2V

Table 11.

Application Information *(continued)*

Maximum Input Voltage Range for FI Mode

In order to ensure that the full-scale output current range (FSC) can be achieved by the 4707, errors such as gain, linearity, common mode, and offset must be taken into account when determining the input voltage range required at IVIN. The equations in Table 12 can be used to determine the input voltage range required at IVIN to achieve full scale current (FSC) at the FORCE pin.

IVIN (Worst Case)	Corresponding Forced Current
$\frac{2V}{Gain}$ + V_{OS} + Common Mode Error + Linearity Error	+ FSC
$\frac{-2V}{Gain}$ + V_{OS} + Common Mode Error + Linearity Error	– FSC

Table 12.

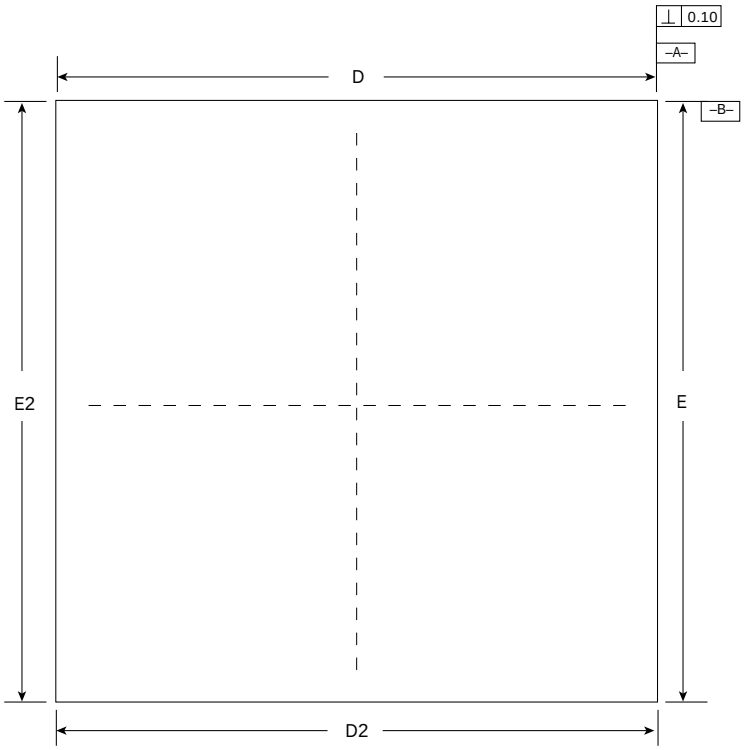
Example: To guarantee that the 4707 is capable of forcing ± 2 mA with REXT = 1KΩ (Range D), the input voltages in Table 13 may be required.

IVIN	Corresponding Forced Current
2.15V	2 mA
–2.15V	– 2 mA

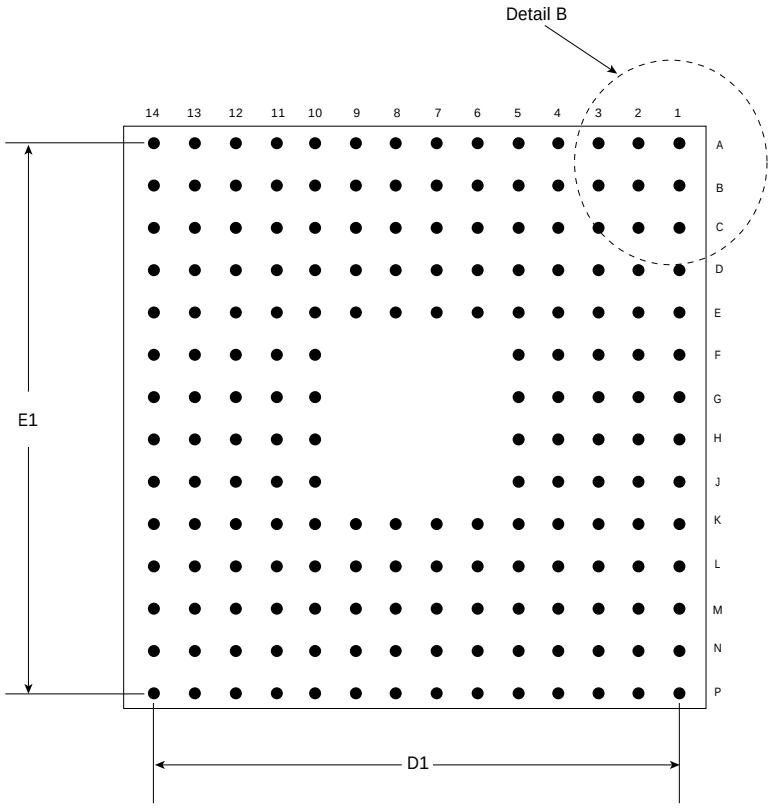
Table 13.

Package Information

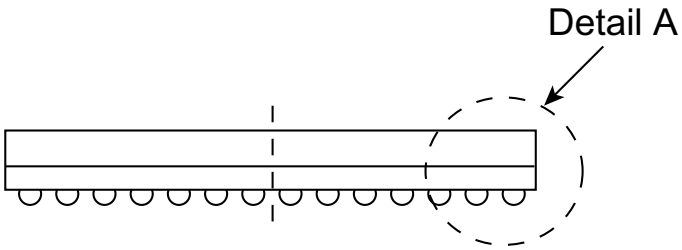
Top View



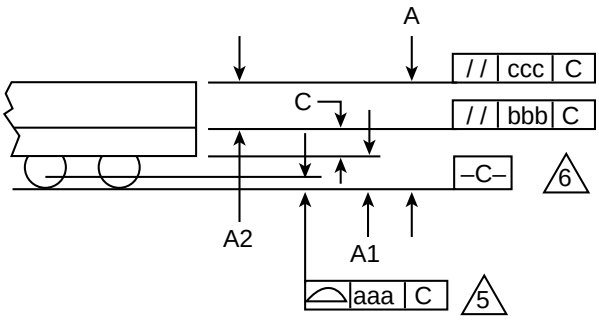
Bottom View



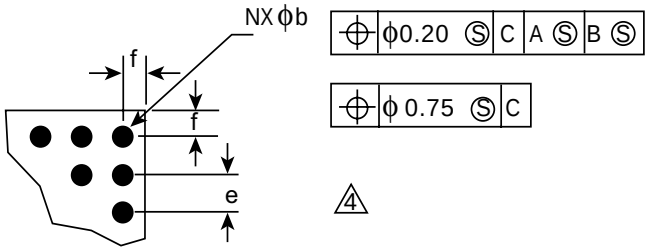
Package Information *(continued)*



Side View



Detail A



Detail B

NOTES:

1. All dimensions are in millimeters.
2. 'e' represents the basic solder ball grid pitch.
3. 'M' represents the basic solder ball matrix size, and symbol 'N' is the maximum allowable number of balls after depopulating.
4. 'b' is measurable at the maximum solder ball diameter parallel to primary datum –C–.
5. Dimension 'ccc' is measured parallel to primary datum –C–.
6. Primary datum –C– and seating plane are defined by the spherical crowns of the solder balls.
7. Package surface shall be matte finish charmilles 24 to 27.
8. Package warp shall be 0.050 mm maximum.
9. Substrate material base is BT resin.
10. The overall package thickness 'A' already considers collapse balls.

Dimensional References			
REF.	**MIN.**	**NOM.**	**MAX.**
A	1.30	1.45	1.55
A1	0.30	0.40	0.45
A2	0.65	0.70	0.75
D	11.80	12.00	12.20
D1		10.40 BSC.	
D2	11.80	12.00	12.20
E	11.80	12.00	12.20
E1		10.40 BSC.	
E2	11.80	12.00	12.20
b	0.50	0.55	0.60
c		0.35	
aaa			0.15
bbb			0.20
ccc			0.25
e	0.725	0.80	0.875
f	0.70	0.80	0.90
M		14	
N		180	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Power Supply (relative to GND)	VCC	15.25	15.5	15.75	V
Negative Analog Power Supply (relative to GND)	VEE	–4.75	–4.5	–4.25	V
Total Analog Power Supply	VCC – VEE	19.5	20	20.5	V
Digital Power Supply (relative to GND)	VDD	3.15	3.3	3.45	V
Case Temperature	TC	25		65	˚C
Thermal Resistance of Package (Junction to Case)	θ_{JC}		4.1		˚C/W

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC			20	V
Negative Power Supply	VEE	–10			V
Total Power Supply	VCC – VEE	0		21	V
Digital Power Supply	VDD	GND – .5		VCC	V
Digital Inputs		–.5		7.0	V
Analog Inputs		VEE – .5		VCC + .5	V
Analog MUX Breakdown Voltage	VI[H, L, HH, LH] – DV[L, H]			VCC – VEE	V
Current Capability of MUX	I_{MUX}	–4.8		4.8	mA
External Force and Sense Switch Breakdown Voltage	E_FC_IN – FORCE E_SN_IN – FORCE			VCC – VEE	V
Storage Temperature		–55		+125	˚C
Junction Temperature		–65		+125	˚C
Soldering Temperature				260	˚C

Stresses above listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Power Supplies

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Consumption (Note 1)					
Positive Supply	ICC			30	mA
Negative Supply	IEE			30	mA
Digital Supply (Quiescent)	IDD			1	mA
Power Supply Rejection Ratio (Notes 2, 3)	PSRR				
1 MHz			8.5		dB
500 kHz			14.5		dB
100 kHz			29		dB

Force Voltage

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range @ VINP	V_{VINP}	VEE + 2		VCC – 1.75	V
Input Bias Current	I_{VINP}	–1	0	1	µA
Output Forcing Voltage (positive full scale current through REXT)	V_{FORCE}	VEE + 2.25		VCC – 4.25	V
Output Forcing Voltage (zero current through REXT)	V_{FORCE}	VEE + 2.25		VCC – 2.25	V
Output Forcing Voltage (negative full scale current through REXT)	V_{FORCE}	VEE + 4.25		VCC – 2.25	V
Voltage Accuracy					
Offset	Vos	–100		100	mV
Gain	FV Gain	.985		1.015	V/V
Linearity	FV INL	–0.025	±.01	+0.025	%FSR
Temperature Dependence (Note 6)					
Temperature Coefficient of Offset	$\Delta Vos/\Delta T$		TBD		TBD
Temperature Coefficient of Gain	$\Delta FVGain/\Delta T$		TBD		TBD
Temperature Coefficient of Linearity	$\Delta FV\ INL/\Delta T$		TBD		TBD

DC Characteristics *(continued)*

Measure Current

Parameter	Symbol	Min	Typ	Max	Units
Current Measurement Range	$I_{MEASURE}$				
Range A		–2		2	µA
Range B		–20		20	µA
Range C		–200		200	µA
Range D		–2		2	mA
Current Measurement Accuracy					
Measure Current Offset	V_{OS}	–150		+150	mV
Gain	MI Gain	.985		1.015	
Linearity (measured at IVMON)	MI INL				
FORCE = VEE + 4.25 to VCC – 5.25V		–.05	±.01	.05	% FSR
FORCE = VCC – 5.25 to VCC – 4.25V		–.08		.08	% FSR
Common Mode Error	CM Error	–1.5		1.5	mV/V
Common Mode Linearity	ΔCM Error	–.05		.05	%FSR
Temperature Dependence (Note 6)					
Temperature Coefficient of Offset	ΔVos/ΔT		TBD		TBD
Temperature Coefficient of Gain	ΔMI Gain/ΔT		TBD		TBD
Temperature Coefficient of Linearity	ΔMI INL/ΔT		TBD		TBD

Force Current

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range @ IVIN	V_{IVIN}	–2.25		2.25	V
Input Bias Current	I_{IVIN}	–1	0	1	µA
Output Forcing Current	I_{FORCE}				
Range A		–2		2	µA
Range B		–20		20	µA
Range C		–200		200	µA
Range D		–2		2	mA
Compliance Voltage Range	V_{FORCE}				
Positive Full-Scale Current through REXT		VEE + 2.25		VCC – 4.25	V
Zero Current through REXT		VEE + 2.25		VCC – 2.25	V
Negative Full-Scale Current through REXT		VEE + 4.25		VCC – 2.25	V
Current Accuracy					
Offset	Ios	–2.5		2.5	% FSR
Gain	FI Gain	.985		1.015	
Linearity (measured at IVMON)	FI INL				
FORCE = VEE + 4.25 to VCC – 5.25V		–.05	±.01	.05	% FSR
FORCE = VCC – 5.25 to VCC – 4.25V		–.08		.08	% FSR
Common Mode Error (Note 4)	CM Error	–3		3	mV/V
Common Mode Linearity	ΔCM Error	–.05		.05	%FSR
Temperature Dependence (Note 6)					
Temperature Coefficient of Offset	ΔVos/ΔT		TBD		TBD
Temperature Coefficient of Gain	ΔFI Gain/ΔT		TBD		TBD
Temperature Coefficient of Linearity	ΔFI INL/ΔT		TBD		TBD

DC Characteristics *(continued)*

Measure Voltage

Parameter	Symbol	Min	Typ	Max	Units
Voltage Measurement Range	V_{SENSE}	VEE + 2.25		VCC – 2.25	V
Voltage Measurement Accuracy					
Measure Voltage Offset	Vos	–100		100	mV
Gain	MV Gain	.985		1.015	
Linearity	MV INL	–.025	±.01	.025	%FSR
Temperature Dependence (Note 6)					
Temperature Coefficient of Offset	ΔVos/ΔT		TBD		TBD
Temperature Coefficient of Gain	ΔMV Gain/ΔT		TBD		TBD
Temperature Coefficient of Linearity	ΔMV INL/ΔT		TBD		TBD

Digital Inputs (FV/FI*, MI/MV*, RS0, RS1, DISABLE, I_FCSEL, E_FCSEL, E_SNSEL, SV_SEL)

Parameter	Symbol	Min	Typ	Max	Units
Input Low Level	VIL			0.8	V
Input High Level	VIH	2.0			V
Input Bias Current @ 0V to VDD	IIN	–1	0	1	µA

External Force & Sense Switches

Parameter	Symbol	Min	Typ	Max	Units
On-resistance – External Force Switches	R_{ON_FRC}		30	45	Ω
On-resistance – External Sense Switches	R_{ON_SNS}		1000	1200	Ω
HiZ (Switch Open) Leakage Current (Note 5) @ FORCE = –3 to +13V, FI Mode	ILEAK	–10		+10	nA
Leakage Current at External Force Switch Input (Switch Open)	ILEAK	–10		+10	nA
Usable Input Voltage Range	Vin	VEE		VCC	V
Capacitance of Force and Sense (Combined) (Notes 2, 5)	C_{FRC_SNS}			14	pF
Maximum Current for E_FC_IN	$I_{F\_FC\_IN}$	–25		25	mA
E_FC_IN Input Capacitance			TBD		pF

DC Characteristics *(continued)*

Analog MUX

Parameter	Symbol	Min	Typ	Max	Units
Usable Input Voltage Range	Vin	VEE		VCC	V
On-resistance (Force) @ 500 µA	R_{ON_MUX}		600	1000	Ω
Leakage Current	I_{LEAK_MUX}			200	nA

IVMON

Parameter	Symbol	Min	Typ	Max	Units
Leakage in DISABLED Mode @ IVMON = –2.2V to +13V	I_{LEAK_IVMON}	–100		+100	nA
IVMON Output Impedance	R_{OUT}		500		Ω

Comparator

Parameter	Symbol	Min	Typ	Max	Units
IVMAX Voltage Range	IVMAX	VEE + 1.75		VCC – 1.75	V
IVMIN Voltage Range	IVMIN	VEE + 1.75		VCC – 1.75	V
Comparator Offset (IVMIN, IVMAX)	Vos	–100		+100	mV
Input Bias Current at IVMIN, IVMAX	Ibias	–1		+1	µA

Digital Outputs (DUTLTH, DUTGTL)

Parameter	Symbol	Min	Typ	Max	Units
Output Low Level @ I_{OL} = –200 µA	VOL			400	mV
Output High Level @ I_{OH} = 200 µA	VOH	2.4		VDD	V

Above DC Characteristic specifications are guaranteed over full Recommended Operating Condition ranges unless otherwise noted.

Note 1: Under no load conditions.
Note 2: Guaranteed by design and characterization. Not production tested.
Note 3: PSRR is tested from VCC/VEE supplies to FORCE and IVMON outputs. Characterized in FV/MI and FI/MV modes.
Note 4: The mV/V units shown are derived as follows: (Δoffset current * range resistance) / Δoutput force voltage.
Note 5: Test Conditions: E_FC_SEL = I_FC_SEL = 0; FV/FI* = 0, FORCE and SENSE tied together over full-scale voltage range.
Note 6: Temperature coefficients are valid over a 25˚C to 65˚C case temperature range unless otherwise noted.

AC Characteristics

Force Voltage/Measure Current

Parameter	Symbol	Min	Typ	Max	Units
FORCE Output Voltage Settling Time (Notes 1, 2)					
To 0.1% of final value ($C_{FORCE/SENSE}$ = 100 pF)	t_{settle}				
Range A				530	µs
Ranges B, C, D				110	µs
Measured Current Settling Time (Notes 1, 4)					
To 0.1% of final value ($C_{FORCE/SENSE}$ = 100 pF)	t_{settle}				
Range A				1.4	ms
Ranges B, C, D				110	µs
To 2% of final value ($C_{FORCE/SENSE}$ = 150 pF)	t_{settle}				
Ranges B, C, D				110	µs
I/V Monitor (Note 3)					
DISABLE True to HiZ Propagation Delay	t_z			60	ns
DISABLE False to Active Propagation Delay	t_{oe}			60	ns
Force Amp Saturation Recovery Time	t_{sat}		35	TBD	µs
Capacitive Loading Range for Stable Operation (FORCE)	C_{LOAD}			4	nF

Force Current/Measure Voltage

Parameter	Symbol	Min	Typ	Max	Units
FORCE Output Current Settling Time (Notes 1, 6)	t_{settle}				
(To 0.1% of final value)					
Range A				2	ms
Ranges B, C, D				250	µs
SENSE (Measure) Voltage Settling Time (Notes 1, 4)	t_{settle}				
(To 0.1% of final value)					
Range A				1.75	ms
Ranges B, C, D				225	µs
I/V Monitor (Note 3)					
DISABLE True to HiZ Propagation Delay	t_z			60	ns
DISABLE False to Active Propagation Delay	t_{oe}			60	ns
Force Amp Saturation Recovery Time	t_{sat}		35	TBD	µs
Capacitive Loading Range for Stable Operation (FORCE)	C_{LOAD}			4	nF

AC Characteristics *(continued)*

Analog MUX

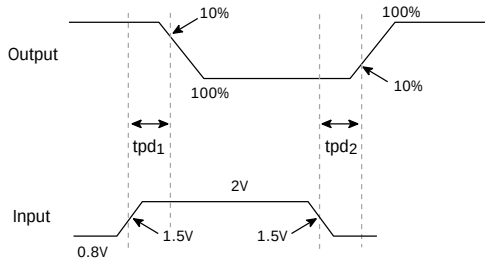
Parameter	Symbol	Min	Typ	Max	Units
Switch Propagation Delay (Note 3)	tpd			60	ns

Comparator

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay	tpd			25	µs

AC Test Conditions (unless otherwise noted): COMP1 to COMP2 = 22 pF, COMP3 = 100 pF to Ground, COMP4 = 47 pF to RES_IN, Capacitive Load at FORCE/SENSE combined output = 150 pF to GND, Capacitive Load at IVMON = 2 nF to GND,

Note 1: Settling times are not production tested. Guaranteed by characterization.
Note 2: Measured from 2V step at VINP to FORCE output.
Note 3: Not production tested. Guaranteed by characterization.
Test Conditions for Characterization:
1. 15 pF load on output
2. input signal has 5 ns rise/fall time
3. tpd is defined as the difference between the time when the output changes 10% (of the total change) from the initial voltage level, and the time when the input crosses 1.5V (see timing diagram below).



Note 4: Measured from 2V step at VINP to IVMON output.
Note 5: Measured from 2V step at IVIN to FORCE output.
Note 6: Measured from 2V step at IVIN to IVMON output.

Ordering Information

Model Number	Package
E4707BBG	180 Lead 12 mm x 12 mm FlexBGA
EVM4707BBG	Edge4707 Evaluation Module

Contact Information

Semtech Corporation
High-Performance Division
10021 Willow Creek Rd., San Diego, CA 92131
Phone: (858)695-1808 FAX (858)695-2633

Revision History

Current Revision Date: April 11, 2002
Previous Revision Date: April 5, 2002

Page#	Section Name	Description of Change
9	Functional Schematic	Update figure.
10	Switch Operation on Force and Sense Lines	Change 1st sentence to read: Each channel fo the Edge4707 features two switches connected to the FORCE output pin (External Force = 30Ω, Internal Force = 100Ω) … Change Table 7: to 30Ω to External
23	AC Characteristic	AC Test Conditions note: Delete "Case Temperature = 25˚C.
23	AC Char Notes	Note 3: Add timing diagram

Revision History

Current Revision Date: April 5, 2002
Previous Revision Date: September 24, 2001

Rev. 2 Die Rev. B 9/24/01 Page#	Rev. 3 Die Rev. C 4/5/02 Page #	Description of Change
all	all	Change status from "Preliminary" to "Target". This datasheets represents the transition from Die Revision B to Die Revision C.
1	1	Changed Switch Resistance In Block Diagram to Reflect Design Change
5	5	Changed "Edge" to "Semtech" on picture of device
8	8	Removed Block Diagram
8	9	Added Functional Schematic
9	10	Removed redundant phrase in "Switch Operation on Force and Sense Lines" (capacitance specification documents measurement conditions)
11	12	Eliminated pull-up resistors and changed compensation capacitor values on the required external components diagram.
16	17	Added Thermal Resistance of Package Spec. to "Recommended Operating Conditions"
16	17	Reduced maximum storage and junction temperatures in "Absolute Maximum Ratings"
17	18	Added temperature dependance specifications to FV section
17	19	Added current measurement range to MI section
17	19	Added temperature dependance specifications to MI section
18	19	Removed reference to P-supplies in IVIN input range. specified as absolute level in FI section
18	19	Added compliance voltage range specification
18	19	Relaxed FI CM Error limit in FI section
18	19	Added Temperature dependance specifications to FI section
18	20	Added voltage meausrement range to MV section
18	20	Added temperature dependence specifications to MV section
19	20	Changed External Force switch RDS(ON) specification to reflect design change in "External Force and Sense Switches" section
19	20	Changed FORCE/SENSE combined capacitance specification to reflect design change in "External Force and Sense Switches" section
19	20	Changed Maximum E_FC_IN range to reflect design change in "External Force and Sense Switches" section
19	20	Added E_FC_IN input capacitance specification in "External Force and Sense Switches" section
19	21	Added IVMON output impedance specification to "IVMON" section
20	21	Changed output high level current drive level capability to reflect design change.
21	22	Seperated ranges for settling times in FV/MI and FI/MV sections
21	22	IVMON disable propogation delay times were decreased to reflect design change in FV/MI and FI/MV sections
21	22	Force amp saturation recovery time specification was added in FV/MI and FI/MV sections
21	22	Capacitive loading range at FORCE was added for FV/MI and FI/MV sections
22	23	Analog MUX switch Tpd was reduced to reflect design change
22	23	AC test conditions were modified to reflect Agilent desired characterization conditions. .2%tsettle added for 150 pF load, 0.1% times for 100 pF load
22	23	Propagation delay definition was refined
23	24	Marketing Revision was incremented on Part Number