Eureka Microelectronics,Inc.

EK7411

OBJECTIVE DATA SHEET

384 Channels 8-bit Source Driver for color TFT LCDs

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384-Channel 8-bit Source Driver for color TFT LCDs

DESCRIPTION

The EK7411 is a 8-bit source driver ICs dedicated for SXGA and UXGA TFT-LCD panels. The digital input is a 8-bit word by 6 dots digital display data, where each word can generate 256-grayscale levels. By using R/G/B filters 3 dots can be combined to generate a 16.77 Millions colors pixel. Each output can drive alternately 256 positive-polarity or 256 negative-polarity grayscale levels with respect to the opposite polarity of adjacent odd and even output pins. These 256 positive and negative grayscale levels are generated with 2x8 external reference voltages (V_0-V_7, V_8-V_{15}) feeding a built-in RDAC that implements a gamma correction for the panel. With positive and negative output voltage, these circuits feature a dot-dot inversion, n-lines-dot inversion and frame-dot inversion schemes.

FEATURES

- CMOS input level (2.5V to 3.6V)
- High-speed data transfer: F_{MAX} = 80 MHz (internal data transfer speed when operating at V_{DD1} = 3.0V)
- 48 data bits (8-bit grayscales code x 3 RGB dot x 2 pixels)
- Logic power supply voltage (V_{DD1}): 2.5V to 3.6V
- Driver power supply voltage (V_{DD2}): 8.5V to 15V
- Output dynamic range: V_{SS2} + 0.1V to V_{DD2} – 0.1V
- 384 outputs
- 256 positive and negative output voltage levels by means of 2x8 external reference voltages and a built in D/A converter (R-DAC)
- Applies for dot-dot inversion, n-line-dot inversion and frame-dot inversion
- Output voltage polarity inversion function (LPOL)
- Bi-directional shift (R/L)
- Chip-enable signal generation circuit
- Display data inversion function (POL1, POL2)

1. INTERNAL BLOCK DIAGRAM

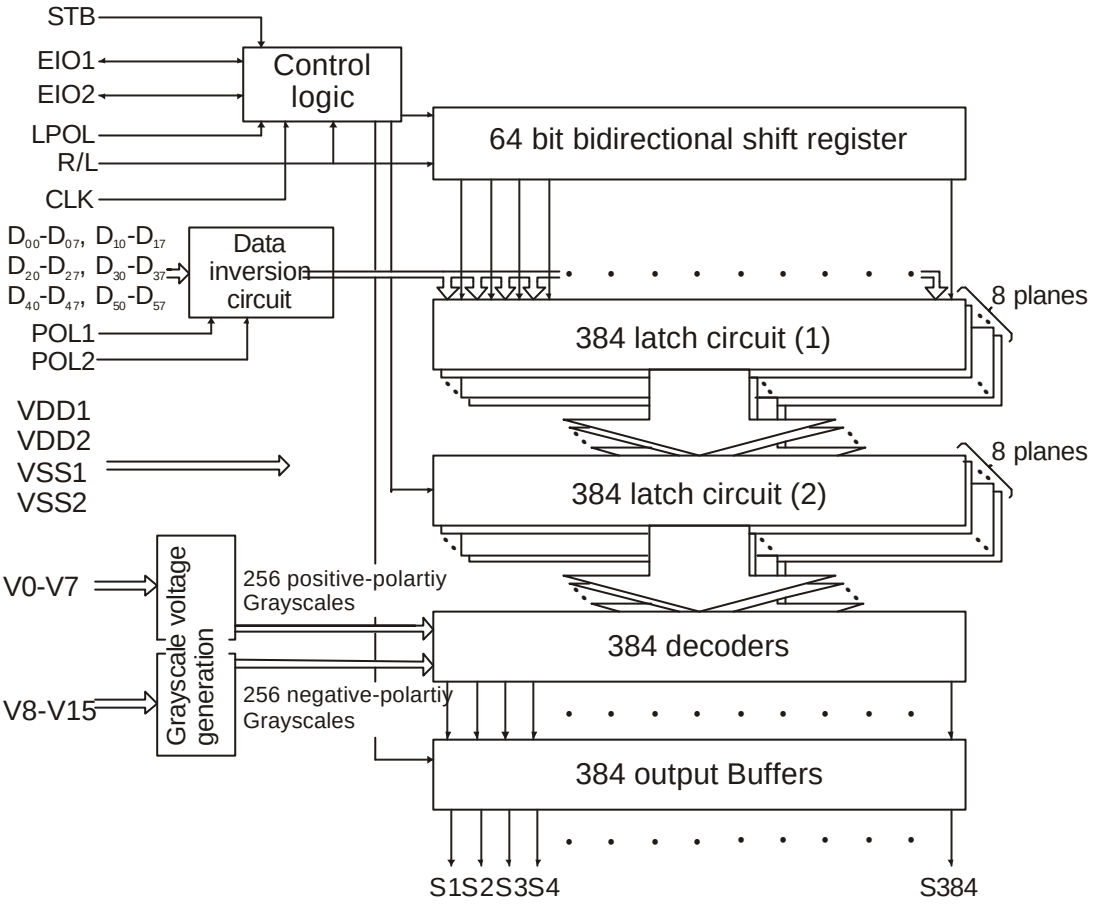


Figure 1: Block diagram

1. **Control logic unit**
   Generates the chip-enable signal EIO1 and EIO2 and the internal control signals.
2. **Data inversion unit**
   Uses the POL1-POL2 signals to invert or not the 6 x 8-bit input data.
3. **64 bits bi-directional shift register**
   Generates the enable signals for sequential latching of 64 groups of 48-bit input data.
4. **Latch circuit (1)**
   384x8-bit latch circuits that latch sequentially 6 outputs x 8-bit (2 pixels) from the data bus.
5. **Latch circuit (2)**
   Stores on the rising edge of STB signal the 384x8-bit line data from the first latch stage to the output buffers.
6. **Decoders**
   Select one of the 256-grayscale levels as a function of the 8-bit code word.
7. **Grayscale voltage generation unit**
   Performs a voltage division of the 16 external input reference voltages, and generates 256 positive-polarity and 256 negative-polarity grayscale levels.
8. **Buffers**
   Drive the selected grayscale voltage level to the panel.

2. PIN CONFIGURATION (TPC PACKAGE)

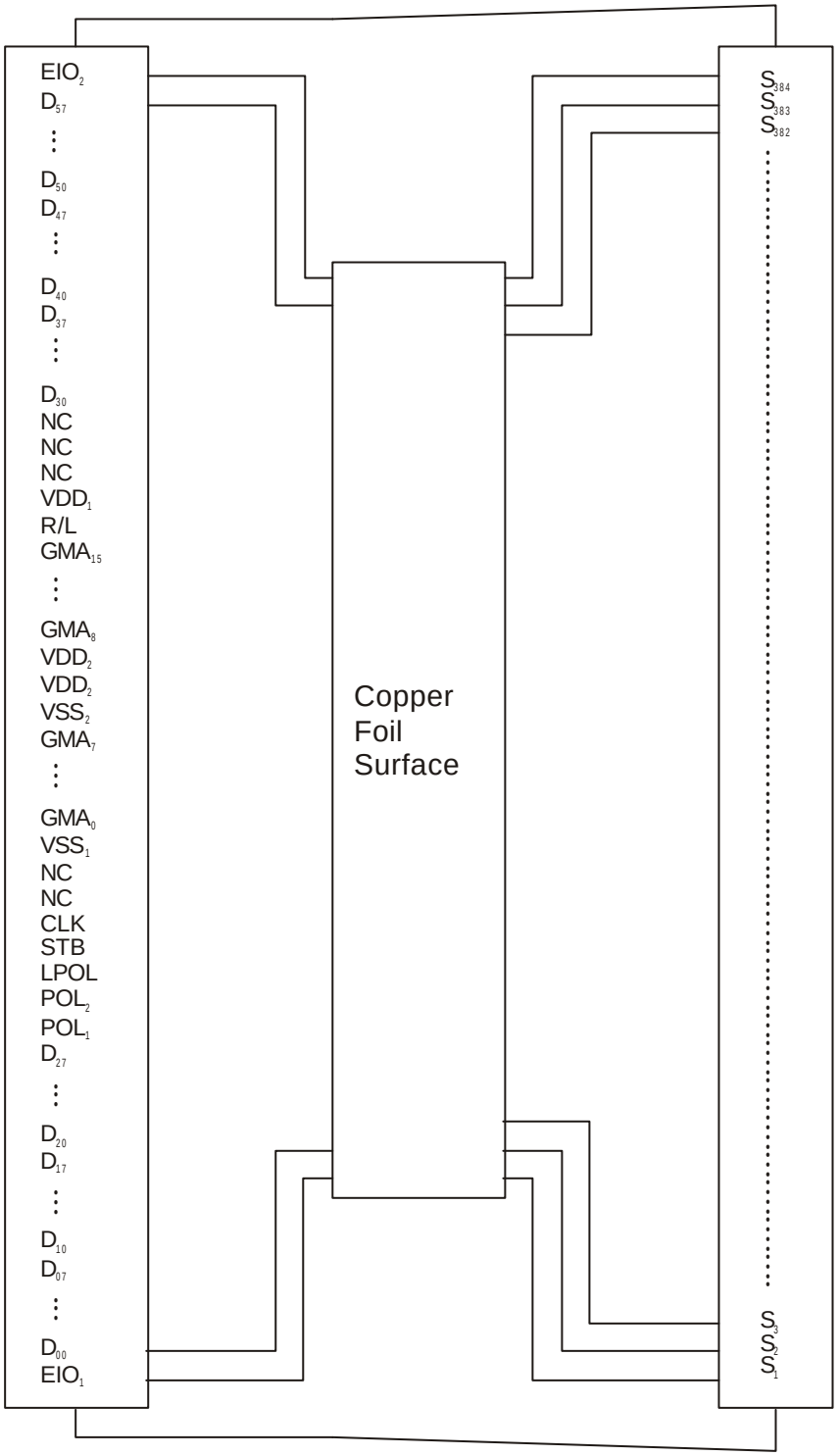


Figure 2: Pin Arrangement

3. PIN FUNCTIONS

Signal Name	Pin Type	Function
S_1 to S_{384}	Output	Signal lines for output of liquid-crystal application voltages
D_{00} to D_{07} D_{10} to D_{17} D_{20} to D_{27} D_{30} to D_{37} D_{40} to D_{47} D_{50} to D_{57}	Input	8-bit Input (grayscale data) x 6-dot display data (2 pixels) *D_{X0}: is the LSB, D_{X7}: is the MSB*
R/L	Input	Controls the display data shift direction *R/L = H : EIO1 input, S_1 ® S_{384}, EIO2 output* *R/L = L : EIO2 input, S_{384} ® S_1, EIO1 output*
EIO_1	Bidir	Right shift start pulse *R/L = H : Becomes the start pulse input pin* *R/L = L : Becomes the start pulse output pin*
EIO_2	Bidir	Left shift start pulse *R/L = H : Becomes the start pulse output pin* *R/L = L : Becomes the start pulse input pin*
CLK	Input	Shift register clock input *Refers to the shift register' s shift clock input. The display data are incorporated into the first stage latch at the rising edge of this clock. At the rising edge of the 64th clock after the input start pulse, the output start pulse goes high, and becomes the input start pulse of the next driver stage.* *After the input start pulse, display data storing is halted automatically when 66 clock pulses are input.*
STB	Input	Load line *The data of one line is transferred from the latch 1 to the latch 2 stage at the rising edge of this clock, and the liquid-crystal application voltage is output at its falling edge. Outputs are in high impedance when STB is active. One pulse must be input in each horizontal period.*
LPOL	Input	Polarity *LPOL = L: The S_{2n-1} outputs drive positive-polarity grayscales levels The S_{2n} outputs drive negative-polarity grayscale levels.* *LPOL = H: The S_{2n-1} outputs drive negative-polarity grayscales levels The S_{2n} outputs drive positive-polarity grayscale levels.* *S_{2n-1} indicates odd outputs and S2n indicates even outputs.*
POL_1, POL_2	Input	Data inversion control of display input data *POL1 controls D_{0j} to D_{2j}, POL2 controls D_{3j} to D_{5j}* *POLx = H : Display data is inverted* *POLx = L : Display data is not inverted* *Default POL1 is shorted to POL2 on the TCP to control D_{0j} to D_{5j} simultaneously.*

V_0 to V_{15}	Power	γ -Correction reference voltage pins *Input the reference voltage levels for the g - correction. The following relationships must be maintained:* $V_{DD2} - 0.1V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{SS2} + 0.1V$
V_{DD1}	Power	Logic power supply
V_{DD2}	Power	Driver power supply
V_{SS1}	Power	Logic ground
V_{SS2}	Power	Driver ground

4. SYSTEM OVERVIEW

TFT LCD panels are composed of source drivers and gate drivers. The gate driver selects one of the lines of the panel and the source driver writes the grayscale levels on each dot. A controller converts the input RGB video signals to 48-bit data display signals (2 pixels). It controls the gate and source driver ICs. A power supply unit is used to generate the 16 gamma corrected reference voltage (see point 9).

For a SXGA panels (1280x 1024) 10 Source drivers of 384 outputs source driver and 4 gate drivers of 256 outputs are used.

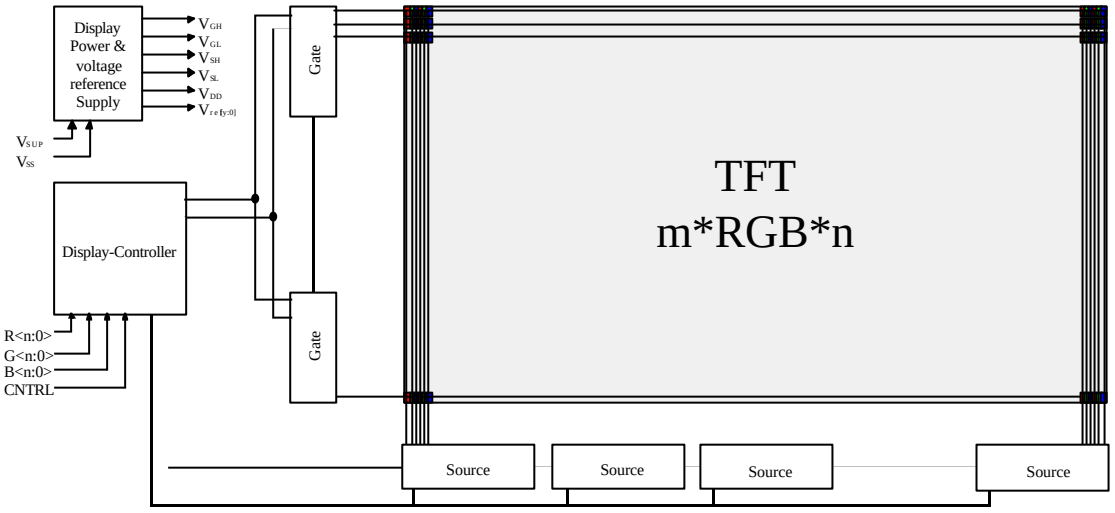


Figure 3: System block diagram

5. OPERATION TIMING

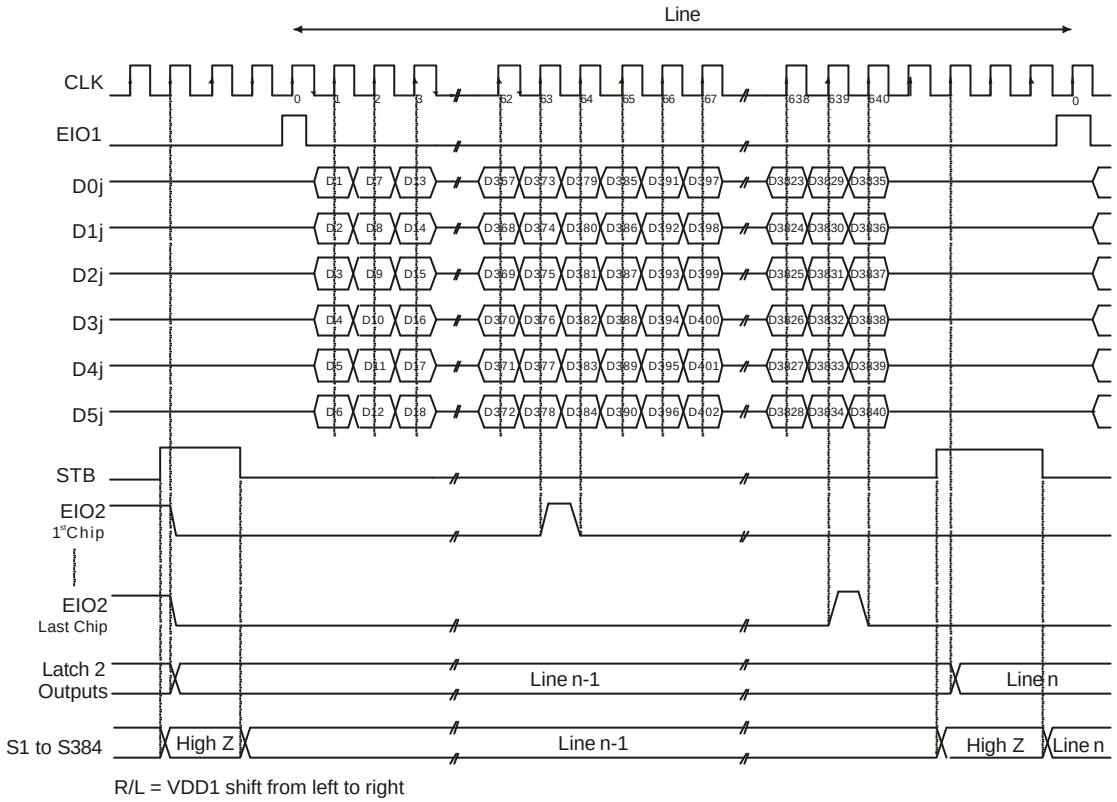


Figure 4: Operation timing diagram

The start condition is initiated by applying a start pulse to the enable input pin (EIO1 when R/L=V_{DD1}) at the beginning of each line of the first chip. During the next 64 CLK rising edges, this source driver chip stores 64 times 48 display data bits (8 grayscale code bits x 3 RGB dot x 2 pixels). While the 63rd data is being stored, it activates (one-clock pulse) the enable output signal (STHL when R/L=V_{DD1}) to enable the following chip.
As soon as the loading of the input data for a complete line is achieved, all enable output signals are activated. Then the controller activates the STB signal to force the 384 output buffers in a high impedance state. At the next CLK rising edge, the data is stored from the first stage latch to the second stage, thus, selecting one of the 256-grayscale levels. Finally, at the falling edge of STB, the 384 output buffers drive the selected grayscale levels to the panel.

6. RELATIONSHIP BETWEEN INPUT AND OUTPUT PIN

Data format: 8 bits x 2 RGB_S (6 dots)
Input width: 48 bits (2-pixel data)

R,/L = H (Right shift)

First → Last

Output	S_1	S_2	S_3	S_4	…	S_{383}	S_{384}
Data	D_{00} to D_{07}	D_{10} to D_{17}	D_{20} to D_{27}	D_{30} to D_{37}	…	D_{40} to D_{47}	D_{50} to D_{57}

R,/L = L (Left shift)

Last ← First

Output	S_1	S_2	S_3	S_4	…	S_{383}	S_{384}
Data	D_{00} to D_{07}	D_{10} to D_{17}	D_{20} to D_{27}	D_{30} to D_{37}	…	D_{40} to D_{47}	D_{50} to D_{57}

7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

Figure 5 explains the relation between the LPOL signal and the output voltage. As shown, the LPOL signal is sampled at the first CLK rising edge after the activation of STB. The resulting internal signal selects which following output (Odd or Even) is positive or negative. As long as STB is active, the 384 output buffers are forced in a high impedance state.

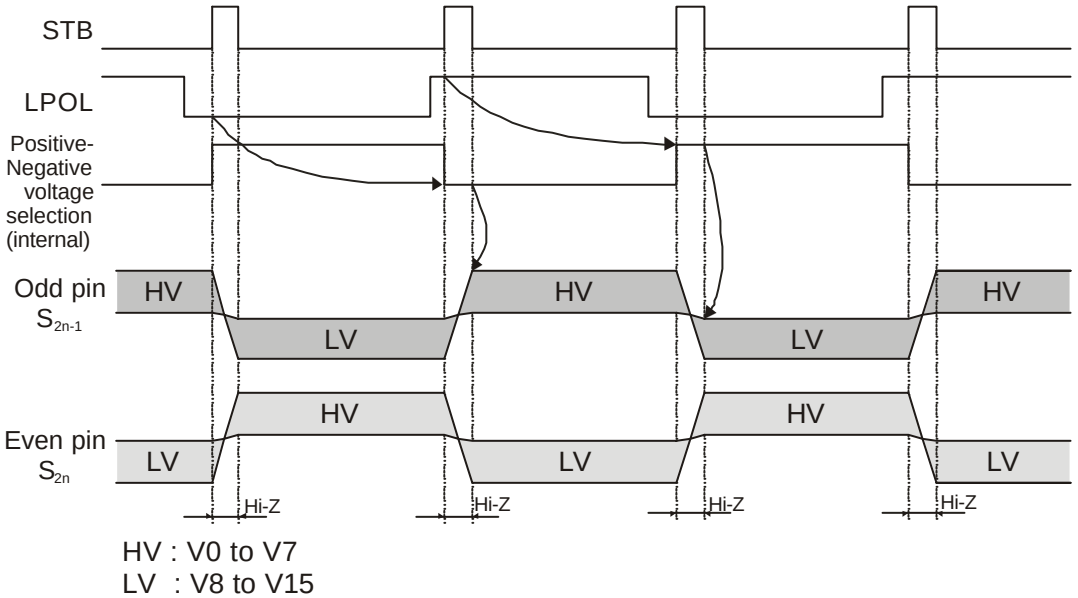


Figure 5: STB and LPOL timing diagram

8. DRIVING SCHEMES

The EK7411 source driver features an alternate positive and negative driving scheme for the odd and even output pins. The polarity selection is achieved by the LPOL signal. Controlling the LPOL signal will enable 3 different driving schemes.

Frame-dot inversion

When LPOL signal is toggled every frame, the polarity inversion is applied on each dot for the same line and on each frame for the same column.

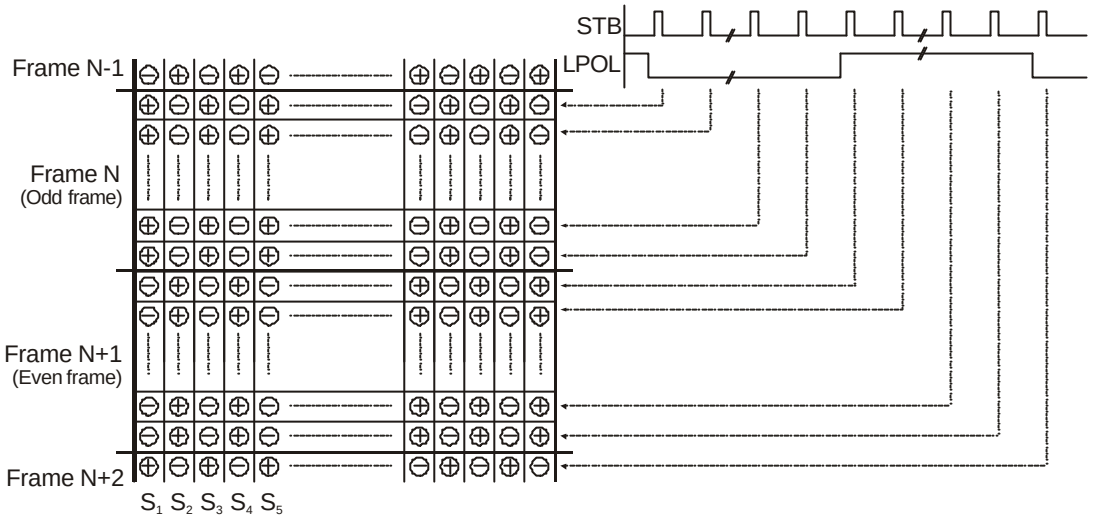


Figure 6: Frame-Dot inversion driving scheme

N-Line-Dot inversion

When LPOL signal is toggled every n-line, the polarity inversion is applied on each dot for the same line and on each n-line for the same column.

2-line inversion is shown in Figure 7 to illustrate such driving scheme.

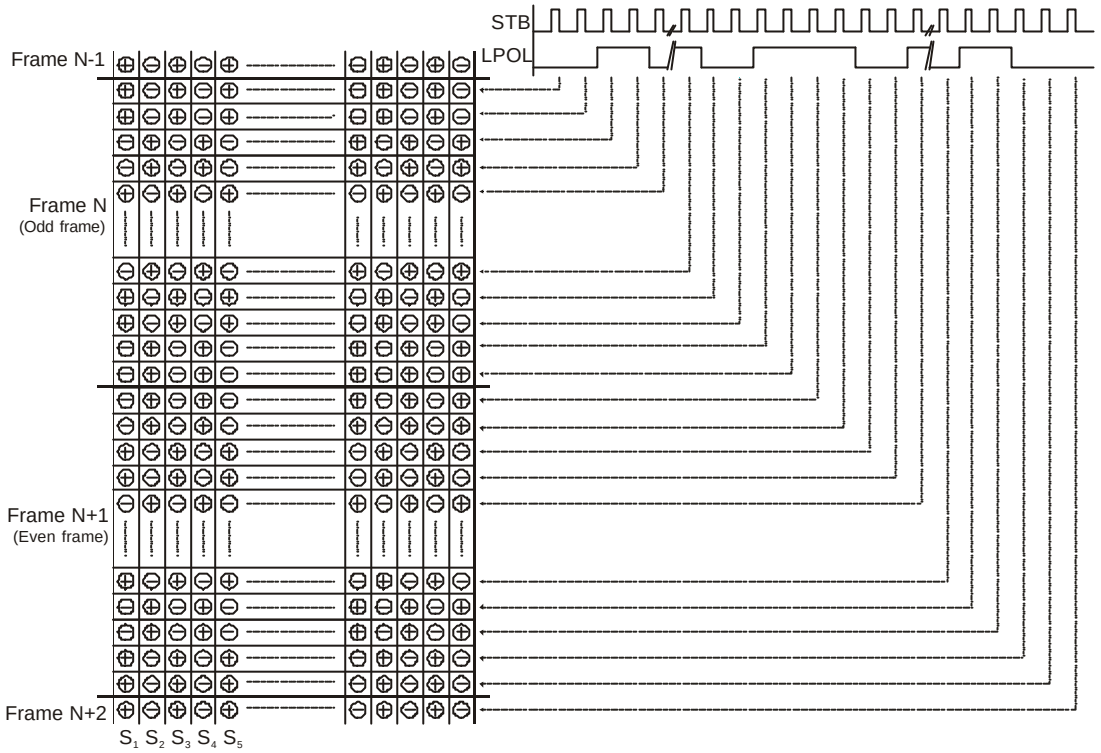


Figure 7: n-Line-Dot driving scheme

Dot-Dot inversion

When LPOL signal is toggled every line, the polarity inversion is applied on each dot for the same line and on each line for the same column.

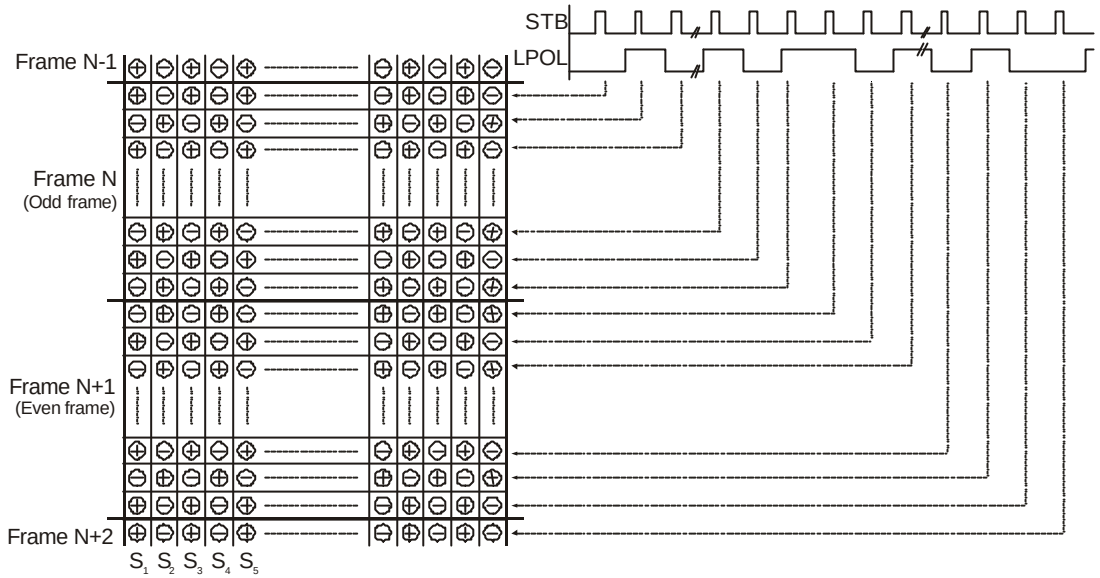


Figure 8 : Dot-Dot driving scheme

For higher quality panels, dot-dot inversion driving scheme can be used. It reduces the cross talk and the sensitivity to flickering. Moreover, odd and even frames should be alternated to avoid the polarization of the liquid.

9. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

A built-in 8-bits D/A converter implements the gamma correction, where two different 256 levels resistor ladders, one for the negative and one for the positive grayscale levels, are used. Eight reference voltages (V_0-V_7 and V_8-V_{15}) connect the 2 resistor ladders. When no fine precision is required on the grayscale levels, V_0, V_7, V_8 and V_{15} can be connected only. With the 12 intermediate reference voltages (V_1 to V_6, V_9 to V_{14}), the gamma correction can be finely adjusted.

Figure 9 represents the relationship between the gamma correction reference voltages, the power supplies V_{DD2} and V_{SS2} and the LCD common voltage. The following voltage relationship $V_{SS2} < V_0 < V_1 < V_2 < V_3 < V_4 < V_5 < V_6 < V_7 < V_8 < V_9 < V_{10} < V_{11} < V_{12} < V_{13} < V_{14} < V_{15} < V_{DD2}$ must be respected.

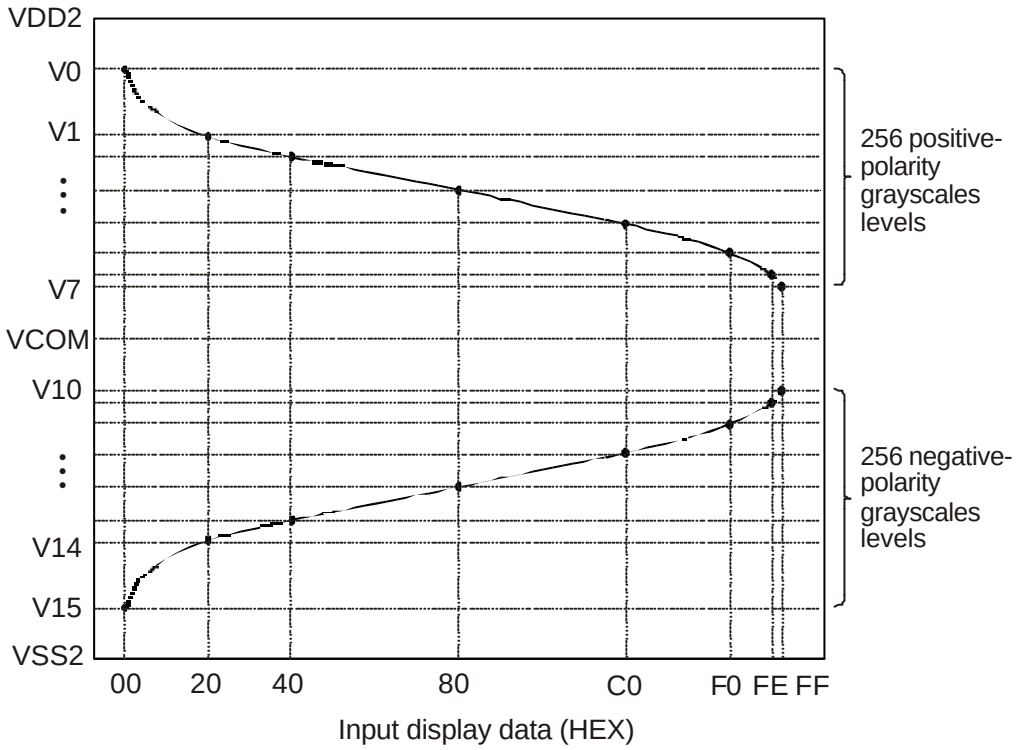


Figure 9: Gamma correction

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Rating (T_A =+25°C, V_{SS1} = V_{SS2} = 0V)

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V_{DD1}	-0.5 to +5.0V	V
Driver Part Supply Voltage	V_{DD2}	-0.5 to +15.0V	V
Logic Part Input Voltage	V_{I1}	-0.5 to V_{DD1} + 0.5	V
Driver Part Supply Voltage	V_{I2}	-0.5 to V_{DD2} + 0.5	V
Logic Part Output Voltage	V_{O1}	-0.5 to V_{DD1} + 0.5	V
Driver Part Output Voltage	V_{O2}	-0.5 to V_{DD2} + 0.5	V
Operating Ambient Temperature	T_A	-30 to +75	°C
Storage Temperature	T_{stg}	-55 to +125	°C

Caution: If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum rating, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum rating.

Recommended Operating Range (T_A =-30 to + 75°C, V_{SS1}=V_{SS2}=0 V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Logic Part Supply Voltage	V_{DD1}		2.5		3.6	V
Driver Part Supply Voltage	V_{DD2}		8.5		15.0	V
High-level Input Voltage	V_{IH}		0.7*V_{DD1}		V_{DD1}	V
Low-level Input Voltage	V_{IL}		0		0.3*V_{DD1}	V
γ-Corrected Voltage	V_0 to V_9		V_{SS2}+ 0.1		V_{DD2}- 0.1	V
Driver Part Output Voltage	V_0		V_{SS2}+ 0.1		V_{DD2}- 0.1	V
Maximum Clock Frequency	F_{MAX}	V_{DD1}=2.5V to 3.0V			60	MHZ
		V_{DD1}=3.0 to 3.6V			80	MHZ

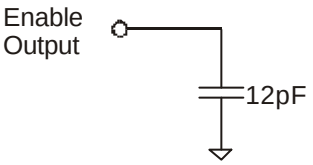
Electrical Characteristics (T_A= -30 to +75°C, V_{DD1}= 2.5V to 3.6V, V_{DD2}= 8.5V to 15V, V_{SS1}=V_{SS2}=0V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input Leakage Current	I_{IL}					±1.0	µA
High-level Output Voltage	V_{OH}	STHR(STHL),I_{OH}=0mA		V_{DD1} - 0.1			V
Low-level Output Voltage	V_{OL}	STHR(STHL),I_{OL}=0mA				0.1	V
γ-Corrected Supply Current	Iγ	V_0 to V_4 = 4.0V V_5 to V_9 = 4.0V	V_0 pin,V_5 pin	TBD	TBD	TBD	
			V_4 pin,V_9 pin	TBD	TBD	TBD	
Output Voltage Deviation	ΔV_0	V_{DD1}=3.3V, V_{DD2}=8.5V,			±10	±20	mV
Output Voltage Range	V_0	All Input data		0.1		V_{DD2} - 0.1	V
Logic Part Dynamic Current Consumption	I_{DD1}	V_{DD1}, with no load			TBD	TBD	
Driver Part Dynamic Current Consumption	I_{DD21}	V_{DD2}= 8.5V±, with no load LPC=H, Bcont= Open			TBD	13.5	mA

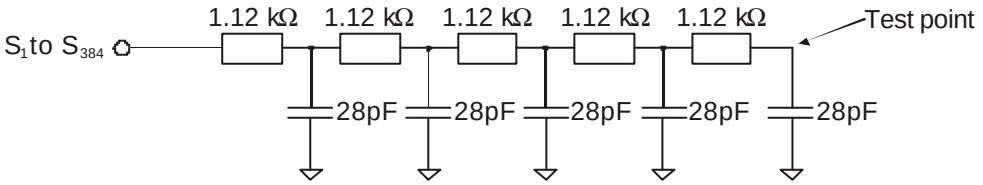
Switching Characteristics (T_A= -30 to +75°C, V_{DD1}= 2.5V to 3.6V, V_{DD2}= 8.5 to 15V, V_{SS1}=V_{SS2}=0V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Delay Time	T_{SD}	C_L =15pF,			10	ns
Driver Output Delay Time	T_{DD1}	C_L =140pF, R_L=5.6kΩ D_{XY}=00H → FFH		2	3	µs
	T_{DD2}			10	12	µs
Input Capacitance	C_{L1}	STHR (STHL) Excluded, T_A=+25°C		5	10	pF
	C_{L2}	STHR (STHL), T_A=+25°C		8	10	pF

Load condition: Start pulse delay Time T_{SD} on Enable output pin



Load condition: Driver Output Delay Time T_{DD1}, T_{DD2} on output buffers

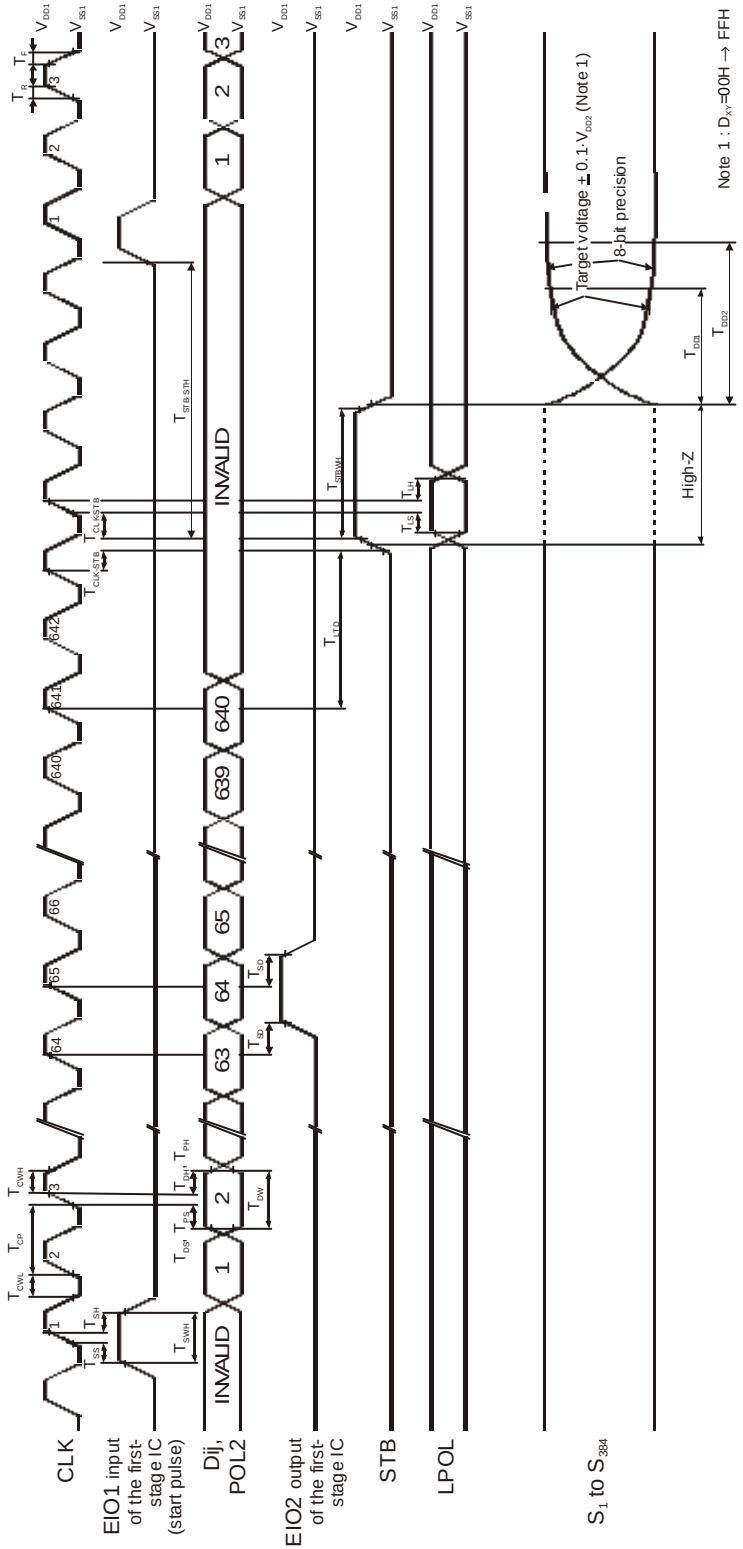


Timing Requirement (T_A= -30 to +75°C, V_{DD1}= 2.5V to 3.6V, V_{SS1}=V_{SS2}=0V, T_r = T_r = 5.0ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Period	T_{CP}	V_{DD1}=2.5V to 3.6V	16.6			ns
		V_{DD1}=3.0V to 3.6V	12.5			ns
Clock high-level width	T_{CWH}		4			ns
Clock low-level width	T_{CWL}		4			ns
Data Setup Time	T_{DS}		0			ns
Data Hold Time	T_{DH}		0			ns
Data width	T_{DW}		4			ns
POL1, POL2 Setup Time	T_{PS}		0			ns
POL1, POL2 Hold Time	T_{PH}		0			ns
Start Pulse Setup Time	T_{SS}		0			ns
Start Pulse Hold Time	T_{SH}		0			ns
Start Pulse high-level width Time	T_{SWH}		4			ns
STB Pulse Width	T_{STBWH}		2			CLK
Last Data Timing	T_{LDT}		1			CLK
CLK-STB Timing	$T_{CLK-STB}$	CLK↑ →STB↑	2			ns
STB-CLK Timing	$T_{STB-CLK}$	STB↑ →CLK↑	2			ns
Time Between STB and Start Pulse	$T_{STB-STH}$	CLK↑ →STB(STHL)↑	3			CLK
LPOL Setup Time	T_{LS}		0			ns
LPOL Hold Time	T_{LH}		4			ns

11. SWITCHING CHARACTERISTICS WAVEFORM

Unless otherwise specified, the input level is defined to V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}



12. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the EK7402.
For more details, refer to the _____
Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

EK7402: TCP(TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C: heating for 2 to 3 Seconds: pressure 100g(per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm^2: time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 Kg/cm^2: time 30 to 40 seconds.

13. LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Eureka customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Eureka for any damages resulting from such improper use or sale.