Eureka Microelectronics,Inc.

EK7302

256 Output Gate Driver

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1. Overview

EK7302 is a gate driver LSI for active matrix LCD panel, which outputs two voltage levels. This chip can be used in the application of XGA, SXGA and SXGA+ mode.

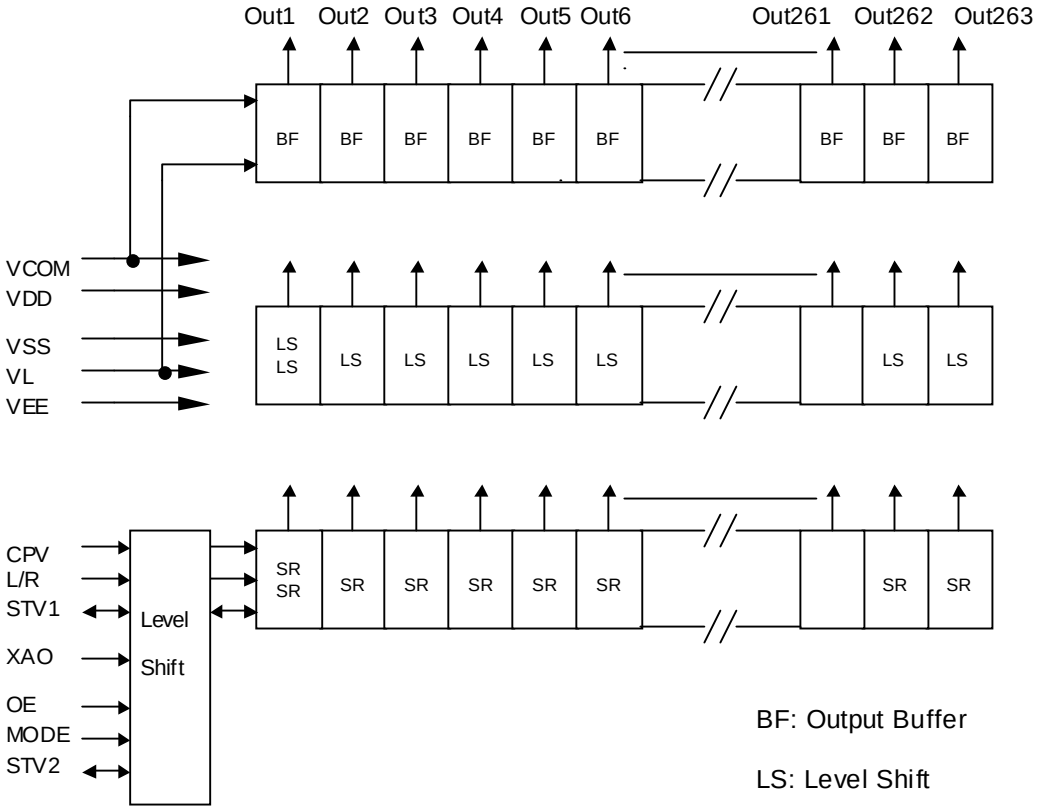
2. Features

- Gate driver LSI for active matrix LCD.
- LCD control output sets either 256 or 263 outputs.
- Required no. of drivers by the definition of panel's resolution.

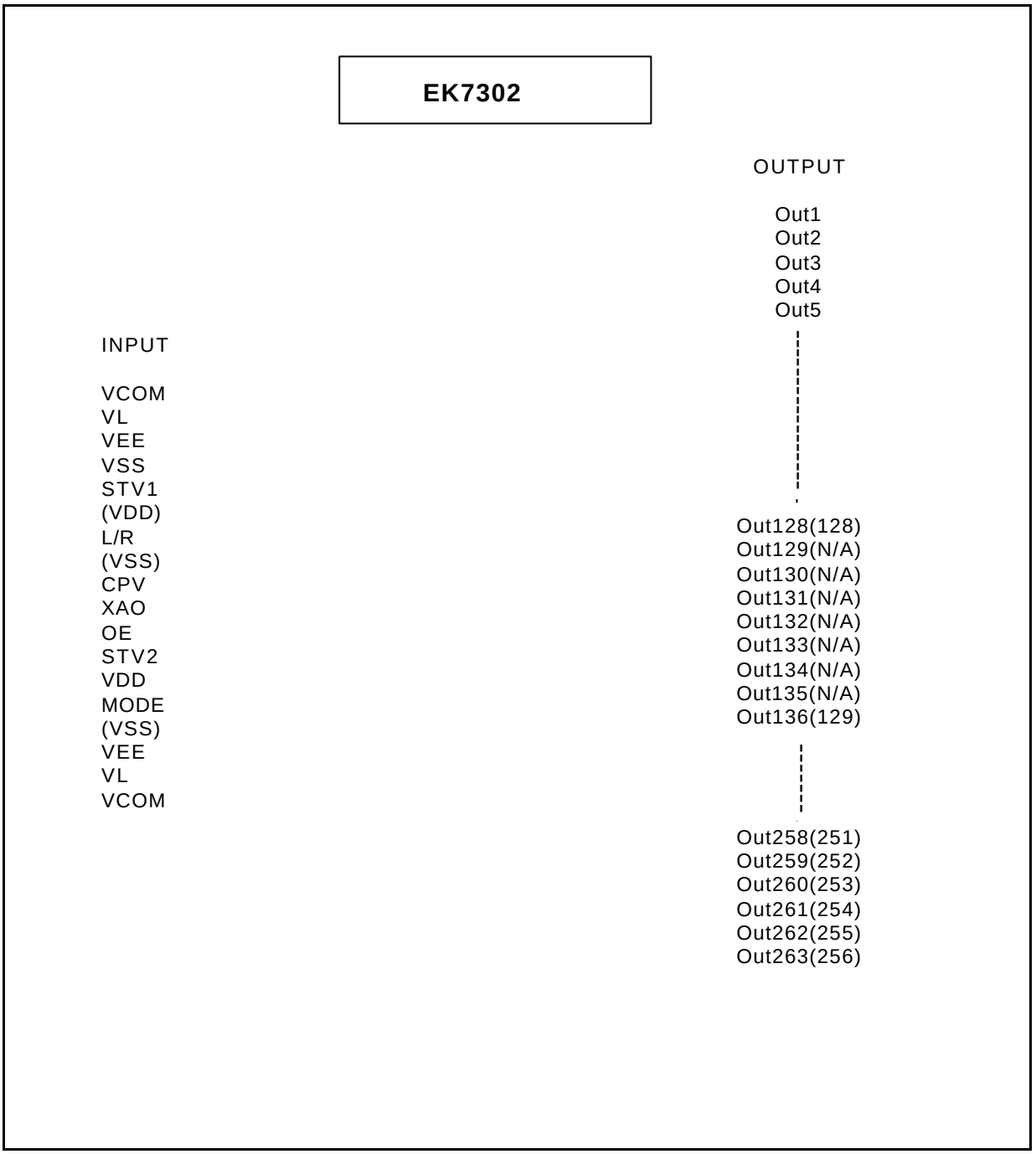
Panel resolution	Mode	Drivers (ea)
XGA (1024 x 768)	256ch	3
SXGA (1280 x 1024)	256ch	4
SXGA+ (1400 x 1050)	263ch	4

- LCD control signal VEE+43V(max)
- Output all-on mode.
- Built-in Bilateral shift register.
- TCP / COF package.

3. Block Diagram



4. I / O pin diagram



Remark: 1.Chip top view from bump surface. This does not specify the TCP package.
2. These are reserved for TCP wiring option, user cannot connect them externally.

5. Pin Description

Pin Name	Input / Output	Description
CPV	Input	Vertical shift clock input The shift register' s shift clock. Data are shifted in sync with the rising edge of this signal.
OE	Input	Output enable input pin. During "H" level of OE, LCD control output is "L". But data included in shift register won' t change. It is asynchronized with CPV.
L / R	Input	Shift direction switching pin. This switches data shift direction as shown below L/R = L: STV1←OUT1← OUT2 OUT262← OUT263 ← STV2 L/R = H: STV1→ OUT1→ OUT2 OUT262→ OUT 263 →STV2
STV1 STV2	Input / Output	Shift data I/O pins These pins are used to input/output data into/from a shift register. During input, data are captured in sync with the leading edge of CPV. During output, data are output in sync with its trailing edge. L/R=L: STV1 is the next-stage data output pin, and STV2 is the shift data input pin. L/R=H: STV1 is the shift data input pin, and STV2 is the next-stage data output pin.
XAO	Input	All output ON input pin. When XAO input level is "L", all outputs are switched "ON" (VCOM), without any relation to the data in the shift register. XAO is asynchronous. XAO function is prior to OE and includes a pull-up resistance.
MODE	Input	Output number select pin. Output pin number can be selected by this input. Mode = H: 263ch mode Mode = L: 256ch mode (OUT129 to OUT135 are not available)
OUT1~OUT263	Output	Output pin for LCD control. Shift register's data are output after level conversion.
VCOM	Power	Supply high voltage.
VDD	Power	Supply logic input.
VSS	Power	Supply logic input.
VL	Power	Supply LCD control OFF voltage.
VEE	Power	GND

6. Function Description

6-1 Functional Description

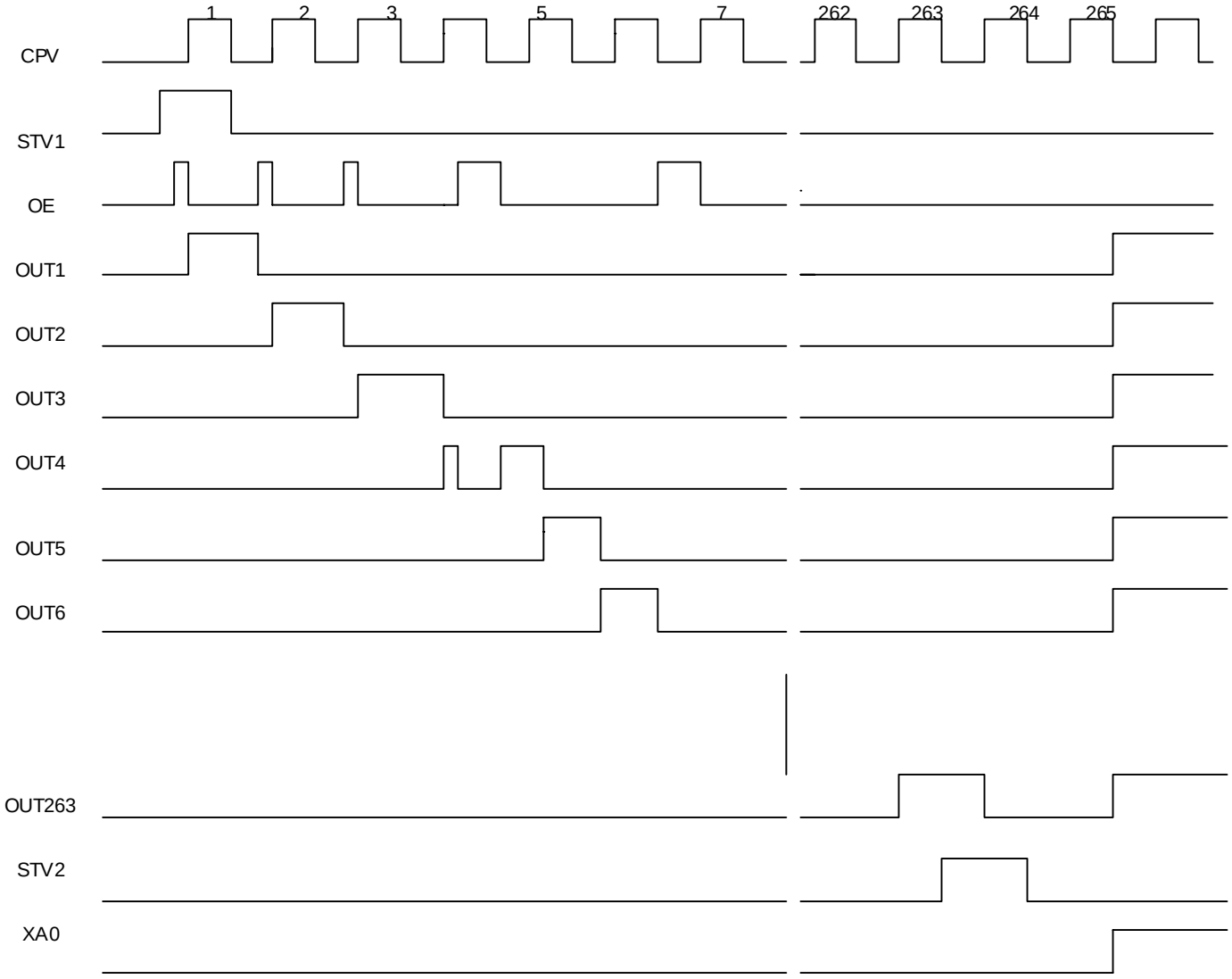
LCD outputs (OUT1 to OUT263) will be set either VCOM or VL, which are controlled by the following input signals, STV1, STV2, CPV, OE and XAO.

By the selection of the shift direction switch L / R, data will be shifted from OUT1 to OUT263 or from OUT263 to OUT1.

In the case of input L / R = “H”, shift data (STV1) will be captured in sync. with the rising edge of the shift clock (CPV) and output to OUT1. At the rising edge of next CPV pulse, the data output of OUT1 will be shifted to OUT2. Each data will shift in sync. with CPV rising edge sequentially. OUT263 data will be output to STV2 in sync. with the falling edge of CPV.

In case of L / R = “L”, shift data (STV2) will be captured in sync. with the rising edge of the shift clock (CPV) and output to OUT263. At the rising edge of next CPV pulse, the data output of OUT263 will be shifted to OUT262. Each data will shift in sync. with CPV rising edge sequentially. OUT1 data will be output into STV1 in sync. with falling edge of CPV.

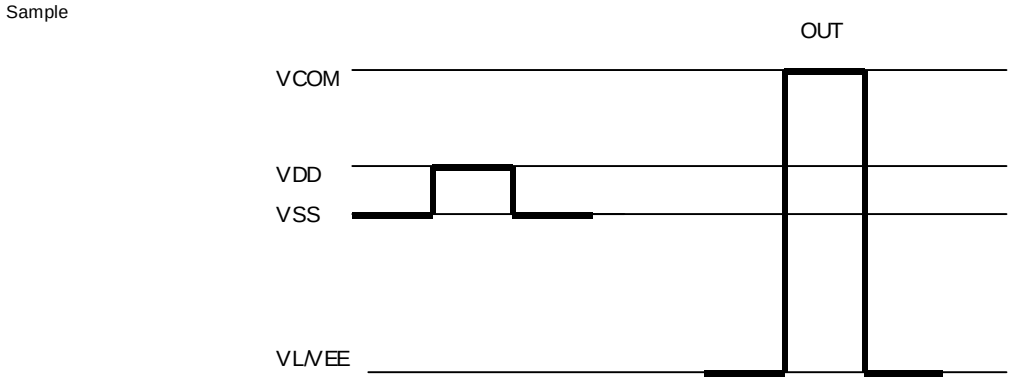
When OE = ”H”, LCD control output is VL level but the data in the registers remain the same.
When OE = “L” again, output level will return to the original voltage.



6-2 All output ON mode

If the input pin is low, all output are switching to the VCOM level asynchronously with CPV. This function should be used carefully because there is a probability of power supply instability by peak current.

6-3 LCD control output voltage



Logic input (CPV, OE, L / R, XAO, MODE, STV1, STV2) should be either at VDD or VSS.

LCD control output pins (OUT1 to OUT263) output should be either at VCOM or VL.

6-4 Caution for "Power ON"

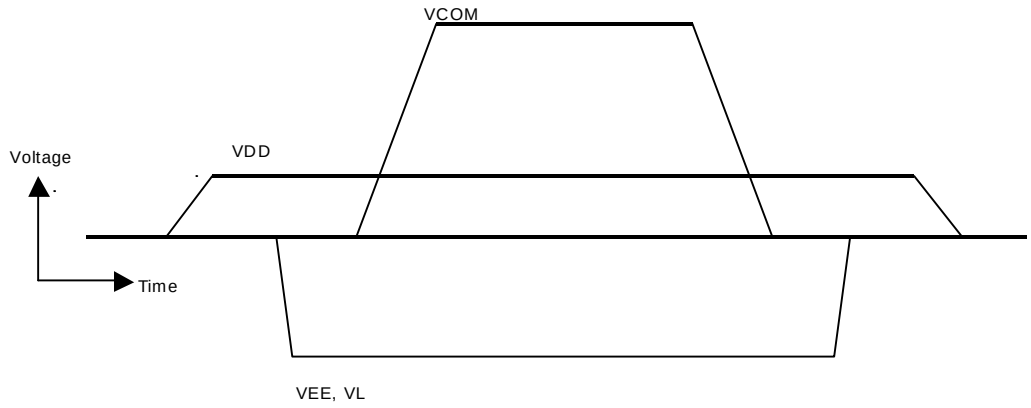
During power on, the data in the latch are undefined. Therefore, we recommend the output enable signal should remain high for one cycle after input data shift operation.

7. Electrical Characteristics (Referenced to the ground terminal)

7-1 Absolute Maximum Ratings (VSS=0)

Item	Signal	Rating	Unit
Supply Voltage (1)	VDD	-0.3 ~ +7.0	V
Supply Voltage (2)	VCOM	-0.3 ~ 32.0	V
Supply Voltage (3)	VEE	-22.0 ~ + 0.3	V
Supply Voltage (4)	VL	VEE-0.3 ~ VEE+7.0	V
Supply Voltage (5)	VCOM-VEE	-0.3 ~ 48.0V	V
Input Voltage	VIN	-0.3 ~ VDD +0.3	V
Temperature	TSTR	-55 ~ +125	°C

Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. Any other conditions beyond these indicated under “recommended operating conditions” is not implied. Exposure to absolute- maximum-rated conditions for extended periods may affect device reliability.
Power up in the following order: VDD→VEE, VL→ input signal →VCOM.
Power down by reversing the sequence.



7-2 Recommendation Operating Conditions

Item	Signal	MIN.	TYP	MAX.	Unit
Supply Voltage (1)	VDD	2.3	3.3	3.6	V
Supply Voltage (2)	VCOM	10.0		30.0	V
Supply Voltage (3)	VEE	-20.0		-3.0	V
Supply Voltage (4)	VL ~ VEE	0.0		6.0	V
Supply Voltage (5)	VCOM-VEE	15.0		43.0	V
Clock Frequency	F_{cpv}			150	K H z
Operating free-air temperature range	Ta	-20		75	°C

7-3 Electrical Characteristics over full range of Recommendation Operating Conditions

Item	Signal	Condition	Min	Typ	Max	Unit	Applicable Pins
"0" input voltage	VIL		VSS		0.3 x VDD	V	
"1" input voltage	VIH		0.7 x VDD		VDD	V	
"0" output voltage	VOL	IOL=40μa	VSS		0.25	V	STV1,2
"1" output voltage	VOH	IOH=40μa	VDD-0.25		VDD	V	STV1,2
"0" output resistance	ROL	VOUT=VEE+0.5V		TBD	1000	Ω	OUT1~OUT263
"1" output resistance	ROH	VOUT=Vcom-0.5V		TBD	1000	Ω	OUT1~OUT263
Input current	Iin		-5.0		+5.0	μA	All inputs except XAO
Pull-up resistance	Rpu	VIN=VSS	10		100	kΩ	XAO
Current Consumption	IDD	(Note 1)		TBD		μA	
Current Consumption	Icom	(Note 2)		TBD		μA	

Remark: 1. Current consumption is based on 1/768 duty cycle.

The outputs are taken without loading. The inputs are VIH=VDD, VIL=VSS, fcpv=50kHz, fstv=104.2Hz, OE=VIL, XAO=VIH.

2. IDD, Icom will be determined after E.S characterization.

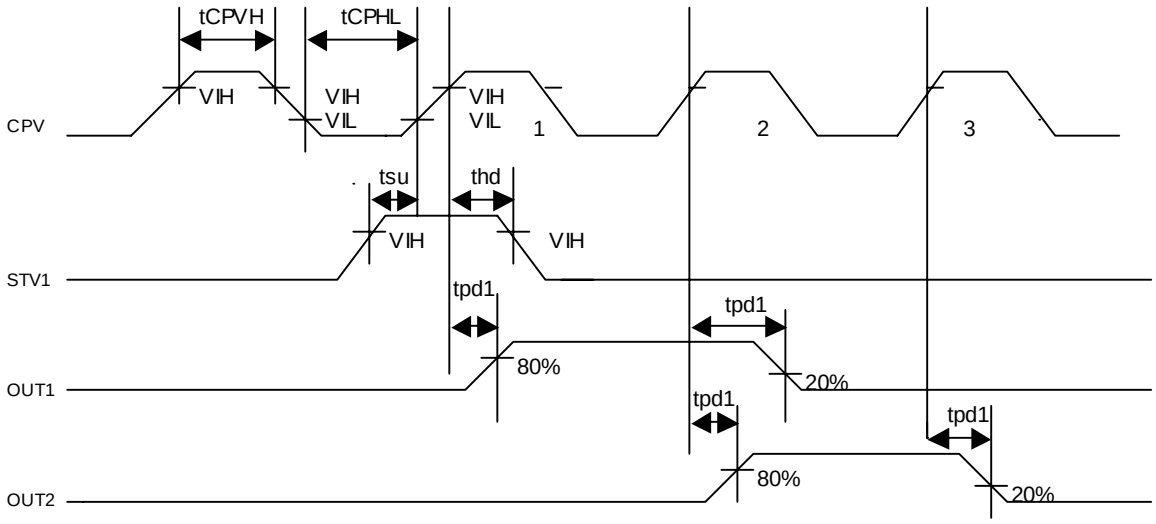
7-4 AC Characteristics

Item	Signal	Condition	MIN	MAX	Unit
Shift Clock Frequency	fCP			150	kHz
Clock Pulse Width	tCPVL, tCPVL		3		μs
Clear Enable	twcl		1.5		μs
Data Set Up	tsu		700		ns
Data Hold	thd		700		ns
Output delay 1	tpd1	CL=300pF		1.5	μs
Output delay 2	tpd2	CL=30pF		1.5	μs
Output delay 3	tpd3	CL=300pf		1.5	μs
Output delay 4	tpd4	CL=300pF		3.0	μs

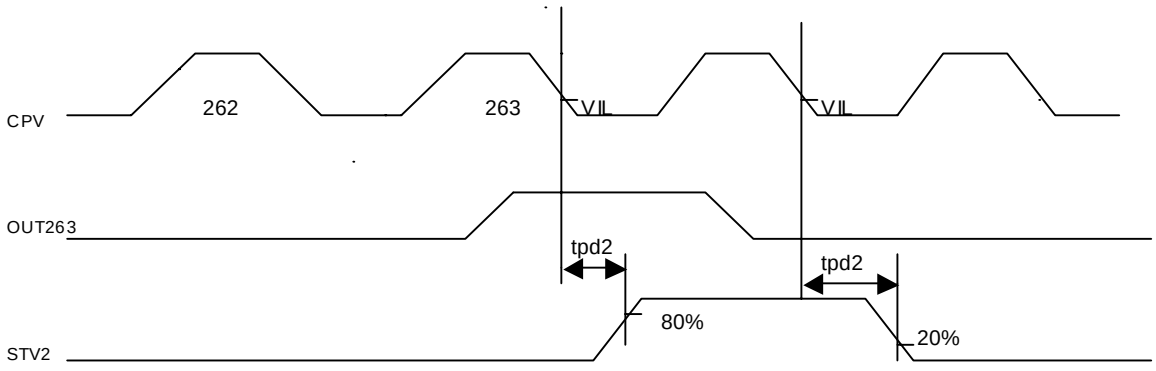
7-5 Timing chart AC characteristics definition

- Input / Output Timing Chart
- STV Output Timing Chart
- OE / XAO Timing Chart

(1) Input / Output Timing Chart



(2) STV Output Timing Chart



(3) *OE / XAO Timing Chart*