

 **Eureka** Microelectronics, Inc.

# EK7102TCA-1901

120 Output Common LCD Driver



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## 120- Output LCD Common Driver IC

### DESCRIPTION

The EK7102 is a 120-output common driver IC suitable for driving dot matrix LCD panels, and it used in personal digital assistant, IA and handheld products. TCP and COG package is available for difference demand, that COG package could be use for customer's system, and the TCP package which is ideal for substantially decreasing the size of the frame section of LCD module. When combined with the Eureka's serials products driver, it can create a low power consuming, high resolution LCD Panel.

### FEATURES

- Number of LCD drive outputs : 120
- Supply voltage for LCD drive : +15.0 to 40V
- Supply voltage for the logic system : +2.5 to +5.5V
- Shift clock frequency 4MHz max. at  $V_{DD}=5V$

- Low power consumption
- Low output impedance
- Built-in 120-bit bi-directional shift register (divisible into 60 bits x 2)
- Available in a single mode (120- bit shift register or in a dual mode (60-bit shift register x 2)
  1.  $Y_1 \rightarrow Y_{120}$  Single mode
  2.  $Y_{120} \rightarrow Y_1$  Single mode
  3.  $Y_1 \rightarrow Y_{60}, Y_{61} \rightarrow Y_{120}$  Dual mode
  4.  $Y_{120} \rightarrow Y_{61}, Y_{60} \rightarrow Y_1$  Dual mode

The above 4 shift directions are pin-selectable
- Shift register circuits are reset when  $\overline{DISPOFF}$  active
- Package : TCP, COG available

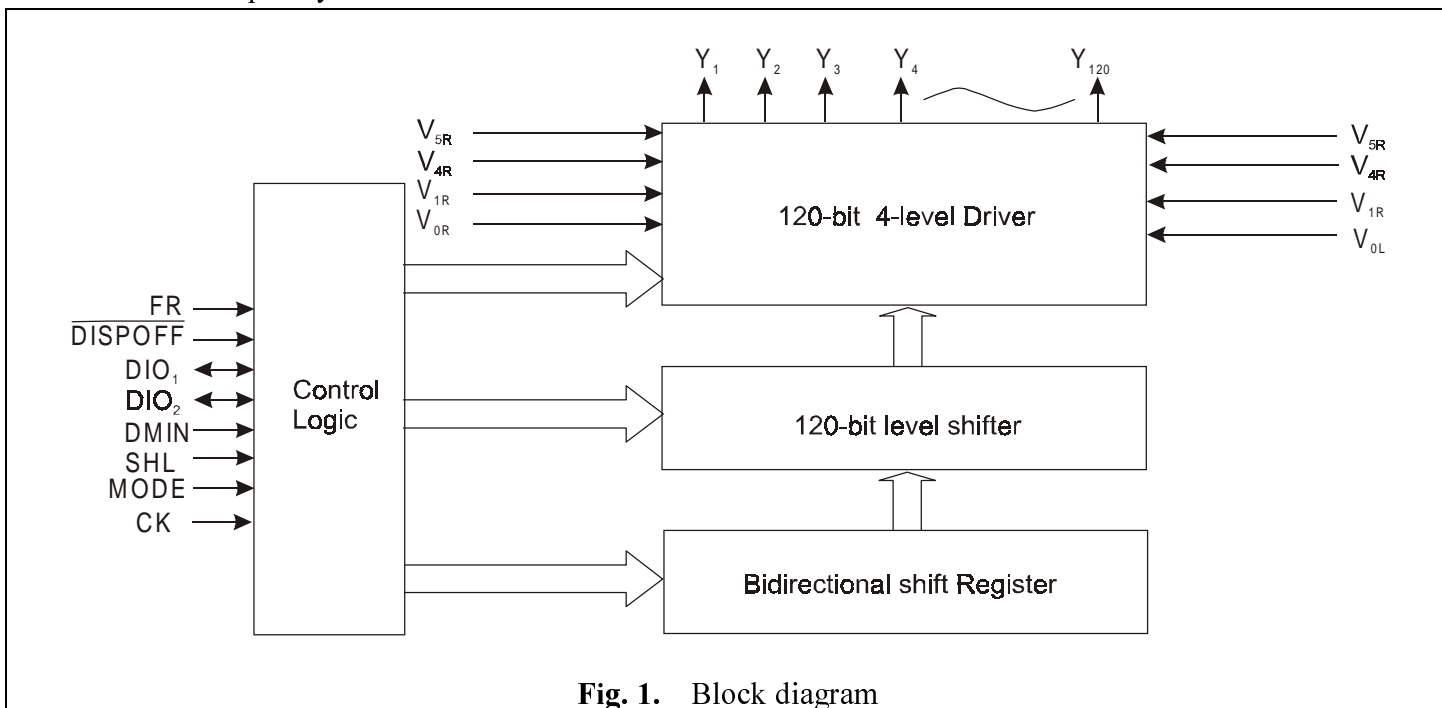
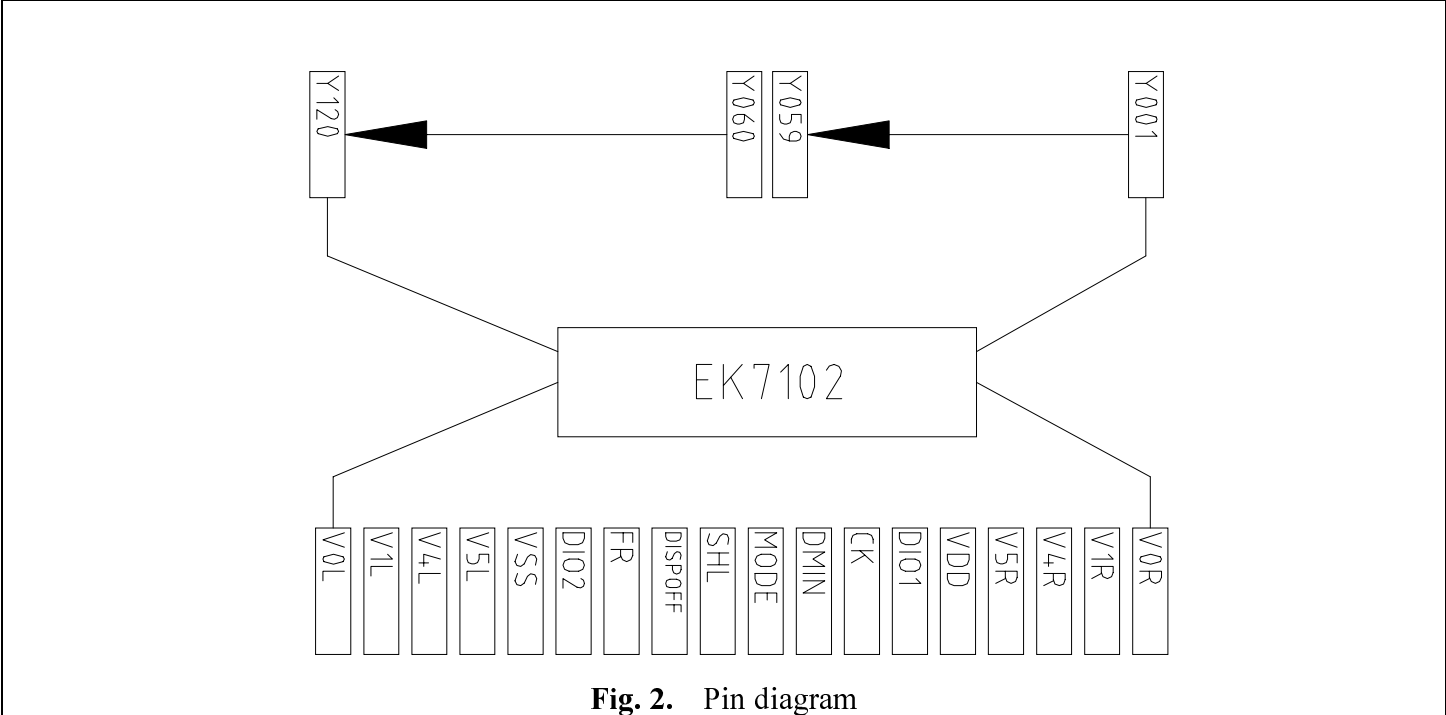


Fig. 1. Block diagram

**PIN CONNECTIONS**



**Fig. 2.** Pin diagram

## PINNING INFORMATION

**Table 1. Pin description**

PIN NO	SYMBOL	I/O	DESCRIPTION
1 to 120	$Y_1$ - $Y_{120}$	O	LCD drive output
121	$V_{0L}$	—	Power supply for LCD drive
138	$V_{0R}$	—	Power supply for LCD drive
122,137	$V_{1L}$ , $V_{1R}$	—	Power supply for LCD drive
123,136	$V_{4L}$ , $V_{4R}$	—	Power supply for LCD drive
124,135	$V_{5L}$ , $V_{5R}$	—	Power supply for LCD drive
125	$V_{SS}$	—	Ground (0V)
126,133	$DIO_2$ , $DIO_1$	I/O	Shift data input /output for shift register
127	FR	I	AC – converting signal input for LCD drive waveform
128	$\overline{DISPOFF}$	I	Control input to disable the display
129	SHL	I	Input for selecting the shift direction of shift register
130	MODE	I	Mode selection input
131	DMIN	I	Dual mode data input
132	CK	I	Shift clock input for shift register
134	$V_{DD}$	—	Power supply for logic system (+2.5 to 5.5 V)

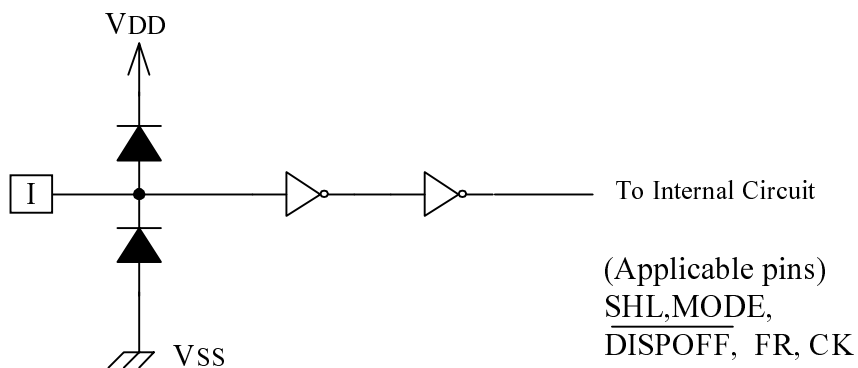
## FUNCTIONAL DESCRIPTION

**Table 2. Functional description**

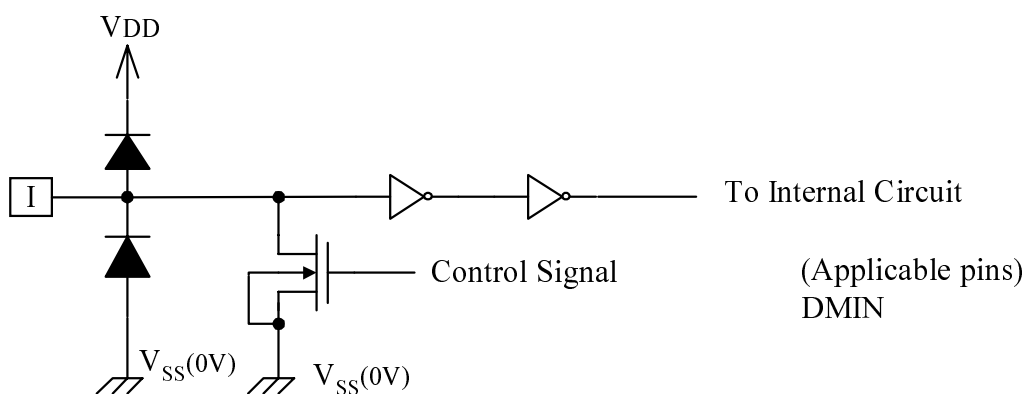
BLOCK	FUNCTION
Shift Register	At the falling edge of the CK signal the Shift Register shifts data from the data input pin, to the data output pin under control of the shift direction and mode setting received from the Control Logic block.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the shift register data, and selects one of 4 levels ( $V_0$ , $V_1$ , $V_4$ or $V_5$ ) based on the FR and $\overline{DISPOFF}$ signals
Control Logic	Controls the shift register's direction of data shift and mode setting in response to SHL and MODE signal inputs

## CIRCUIT DIAGRAMS

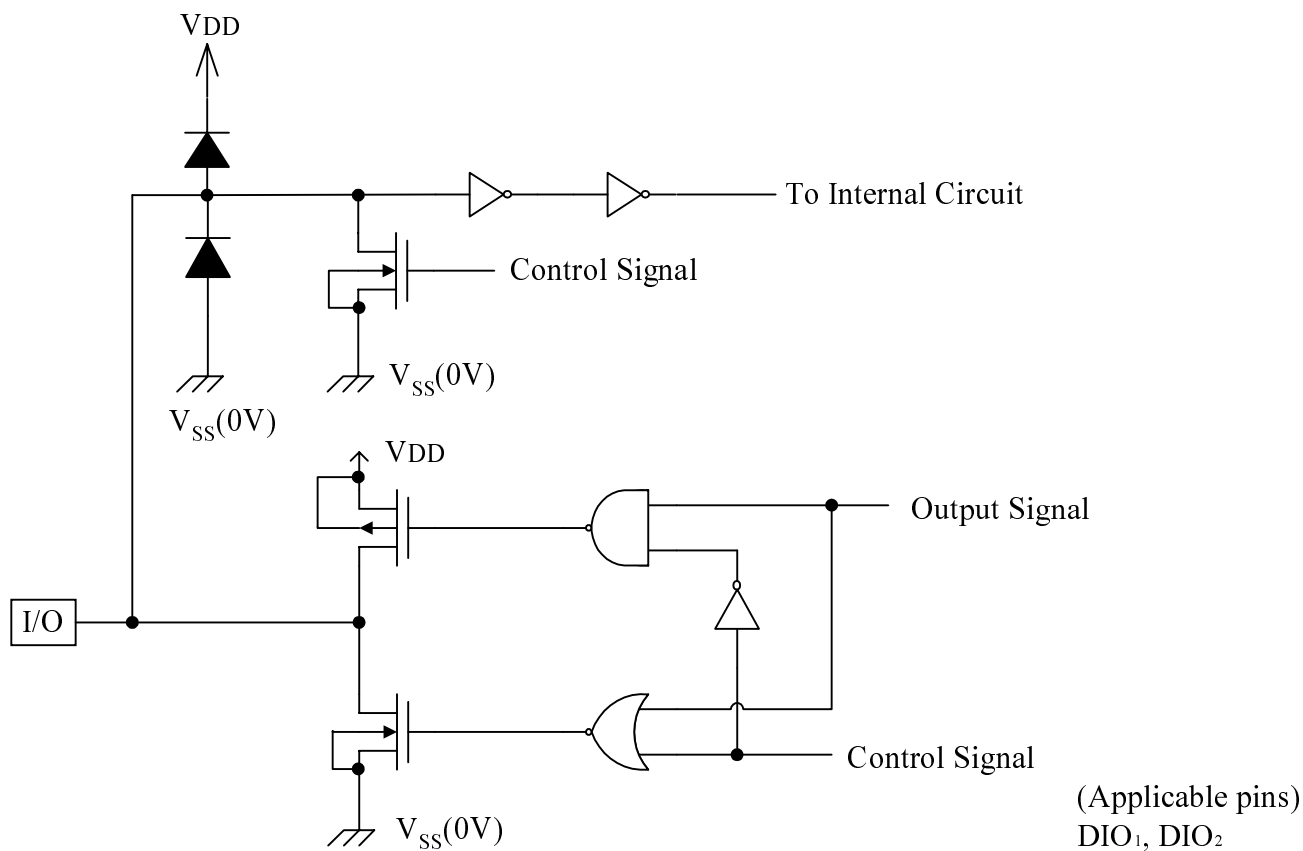
### Input/Output Circuit



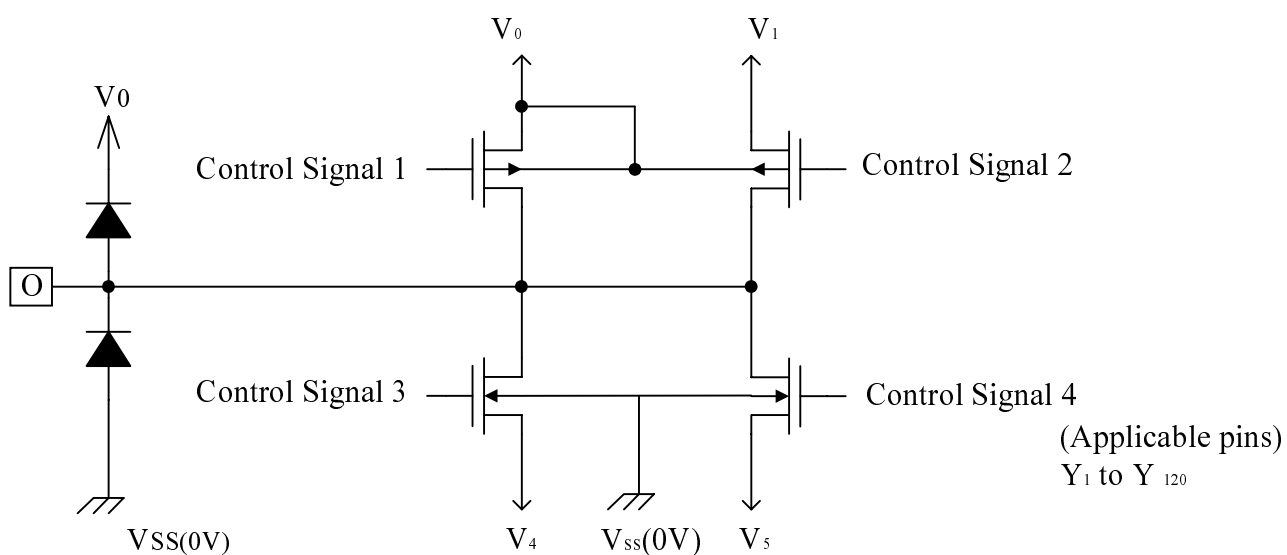
**Fig. 3.** Input Circuit(1)



**Fig. 4.** Input Circuit(2)



**Fig. 5.** Input/Output Circuit



**Fig. 6.** LCD Driver Output Circuit

## PIN DESCRIPTION

**Table 3. Pin Description**

Symbol	Function
$V_{DD}$	Logic system power supply pin, connected to +2.5 to +5.5 V
$V_{SS}$	Ground pin, connected to 0V.
$V_{0L}, V_{0R}$ $V_{1L}, V_{1R}$ $V_{4L}, V_{4R}$ $V_{5L}, V_{5R}$	Power supply pins for LCD drive bias voltage <ul style="list-style-type: none"> <li>Normally use a resistor divider to set the bias voltage.</li> <li>Set the voltages such that <math>V_{SS} \leq V_5 &lt; V_4 &lt; V_1 &lt; V_0</math>.</li> <li><math>V_{iL}</math> and <math>V_{iR}</math> (<math>i=0, 1, 4, 5</math>) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.</li> </ul>
$DIO_1$	Shift data input/output pin for bi-directional shift register <ul style="list-style-type: none"> <li>Input pin when <math>SHL=L</math>, output pin when <math>SHL=H</math>. When <math>SHL=L</math>, <math>DIO_1</math> is used as input pin, it will be pulled down and the data of <math>DIO_1</math> will be latch at the falling edge of CK. When <math>SHL=H</math>, <math>DIO_1</math> is used as output pin, it won't be pulled down and output data will after the falling edge of CK.</li> <li>See also Table 5. .</li> </ul>
$DIO_2$	Shift data input/output pin for bi-directional shift register <ul style="list-style-type: none"> <li>Input pin when <math>SHL=H</math>, output pin when <math>SHL=L</math>.</li> <li>When <math>SHL=H</math>, <math>DIO_2</math> is used as input pin, it will be pulled down and the data of <math>DIO_2</math> will be latched at the falling edge of CK. When <math>SHL=L</math>, <math>DIO_2</math> is used as output pin, it won't be pulled down and output data will change after the falling edge of CK.</li> <li>See also Table 5. .</li> </ul>
CK	Input clock pulse pin to shift the contents of the bi-directional shift register <ul style="list-style-type: none"> <li><math>DIO_1</math> or <math>DIO_2</math> data is shifted at the falling edge of the clock pulse.</li> </ul>
SHL	Direction selection for reading display data <ul style="list-style-type: none"> <li>When SHL is "L". Data is shifted from <math>DIO_1</math> to <math>Y_1</math>, <math>Y_1</math> to <math>Y_2</math>.....<math>Y_{119}</math> to <math>Y_{120}</math> and <math>DIO_2</math>.</li> <li>When SHL is "H". Data is shifted from <math>DIO_2</math> to <math>Y_{120}</math>, <math>Y_{120}</math> to <math>Y_{119}</math>.....<math>Y_2</math> to <math>Y_1</math> and <math>DIO_1</math>.</li> <li>See also Table 5. .</li> </ul>
$\overline{DISPOFF}$	Input pin to set all the outputs to non-select level, active low <ul style="list-style-type: none"> <li>The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.</li> <li>When set to <math>V_{SS}</math> level "L", no matter what values in the shift registers , the LCD drive output pins (<math>Y_1 \sim Y_{120}</math>) are set to level <math>V_5</math> .</li> <li>When set to "L", the contents of the shift register are reset to not reading data. When the <math>\overline{DISPOFF}</math> function is canceled, the driver outputs non-select level (<math>V_1</math> or <math>V_4</math>),and the shift data is read at the next falling edge of the CK. At that time, if <math>\overline{DISPOFF}</math> removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly.</li> <li>See also Table 4. .</li> </ul>

## Pin Description (Continued)

Symbol	Function
FR	AC signal input pin for LCD drive waveform. See also Table 4. <ul style="list-style-type: none"> <li>The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.</li> <li>Normally it inputs a frame inversion signal.</li> <li>The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal.</li> </ul>
MODE	Mode selection input pin. See also Table 5. . <ul style="list-style-type: none"> <li>When set to <math>V_{SS}</math> level "L", single mode is selected; when set to <math>V_{DD}</math> level "H", dual mode is selected.</li> </ul>
DMIN	Dual mode data input pin. See also Table 5. . <ul style="list-style-type: none"> <li>According to the data shift direction of the data shift register, data can be input starting from the 61th bit.</li> <li>When the chip is used in dual mode, DMIN will be pulled down.</li> <li>When the chip is used in single mode, DMIN won't be pulled down.</li> </ul>
$Y_1$ - $Y_{120}$	LCD driver output pins. See also Table 4. <ul style="list-style-type: none"> <li>According to each bit of the shift register, one level(<math>V_0</math>, <math>V_1</math>, <math>V_4</math>, or <math>V_5</math>) is selected and output to LCD panel.</li> </ul>

**Table 4. Logic data to output TRUTH TABLE**

FR	Latch Data	$\overline{\text{DISPOFF}}$	Driver Output Voltage Level( $Y_1$ - $Y_{120}$ )
L	L	H	$V_4$
L	H	H	$V_0$
H	L	H	$V_1$
H	H	H	$V_5$
X	X	L	$V_5$

### Notes:

- $V_{SS} \leq V_5 < V_4 < V_1 < V_0$ , H:  $V_{DD}$  (+2.5 to +5.5V), X : Don't care
  - "Don't care" means that the inputs should be connected to "H" or "L" Do not leave them open.
- There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage which is assigned by specification for each power pin.

**Table 5. Relationship between the DATA I/O PINS and DATA TRANSFER DIRECTION**

MODE	SHL	DATA TRANSFER DIRECTION	DIO <sub>1</sub>	DIO <sub>2</sub>	DMIN
L (Single)	L	$Y_1 \rightarrow Y_{120}$	Input	Output	X
	H	$Y_{120} \rightarrow Y_1$	Output	Input	X
H (Dual)	L	$Y_1 \rightarrow Y_{60}$	Input	Output	Input
		$Y_{61} \rightarrow Y_{120}$			
	H	$Y_{120} \rightarrow Y_{61}$	Output	Input	Input
		$Y_{60} \rightarrow Y_1$			

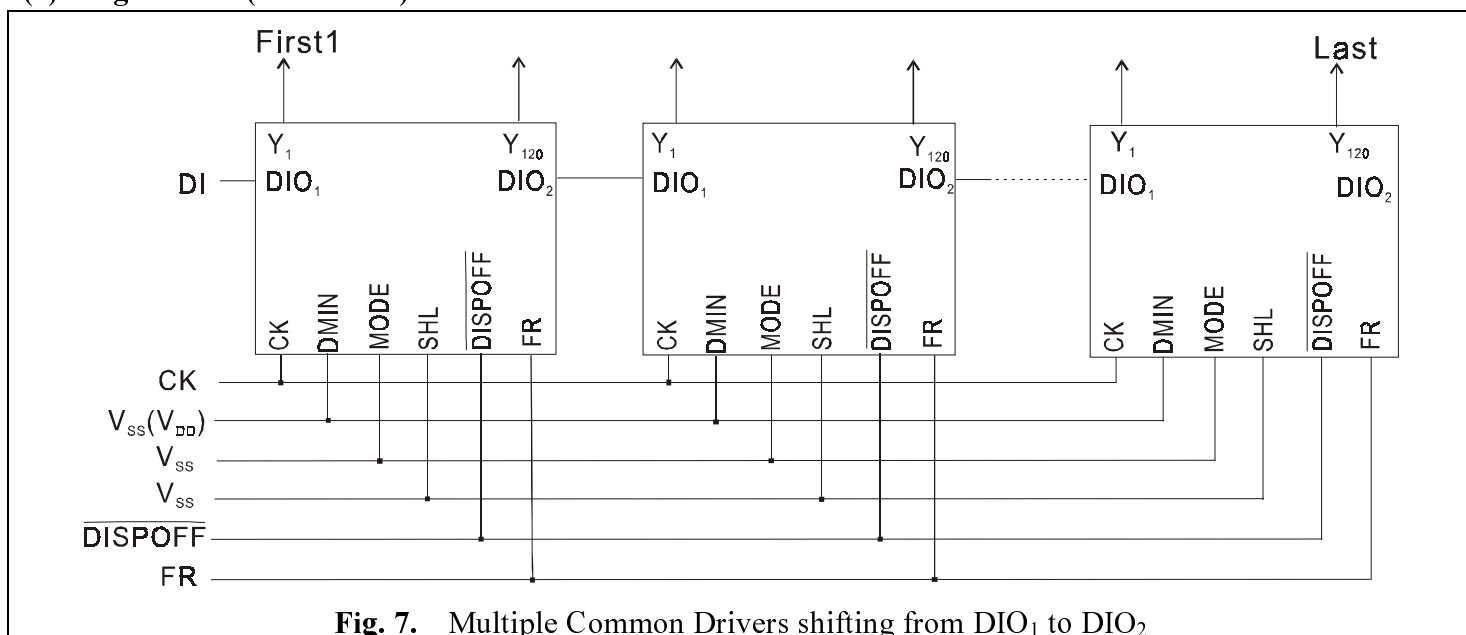
### Notes:

- L :  $V_{SS}$  (0V), H :  $V_{DD}$  (+2.5 to +5.5V), X : Don't care.
- "Don't care" means that the inputs should be connected to "H" or "L" Do not leave them open.



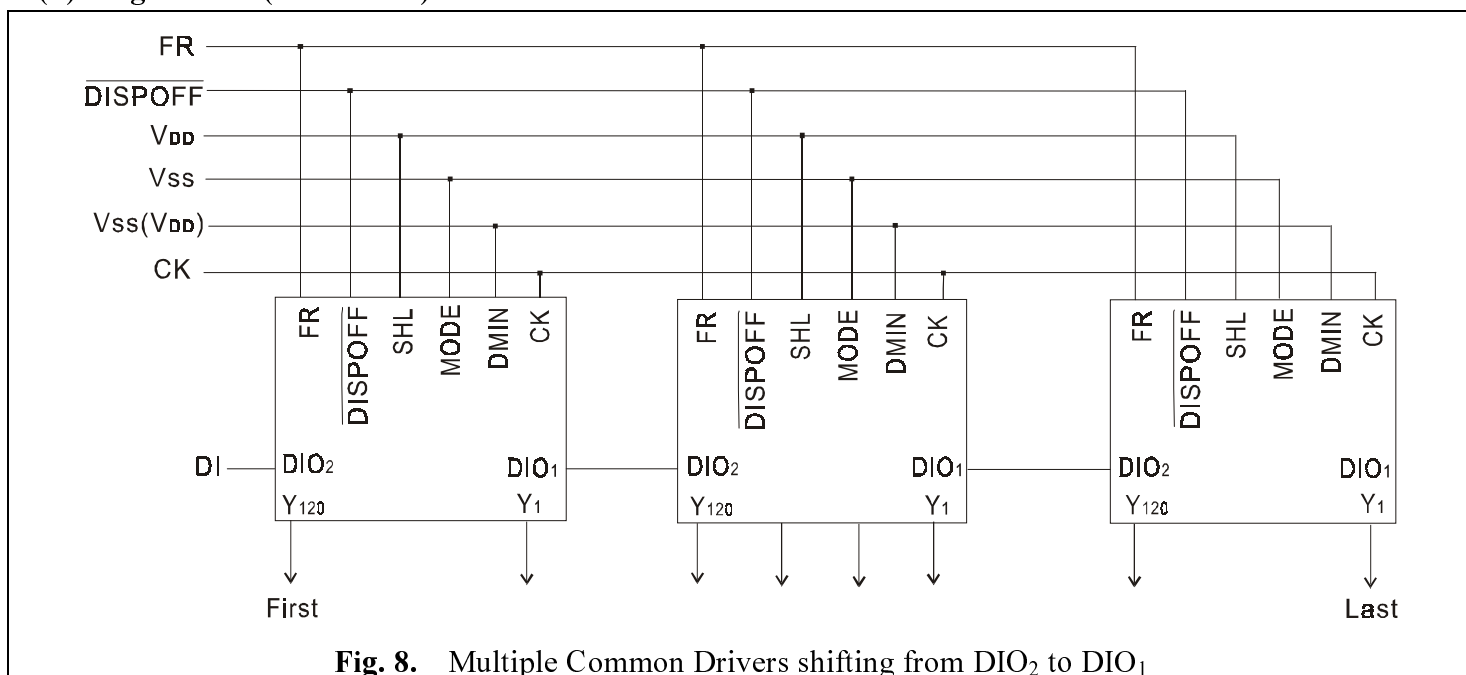
## Application Examples of Multiple Common Drives

### (a) Single Mode (SHL= "L")



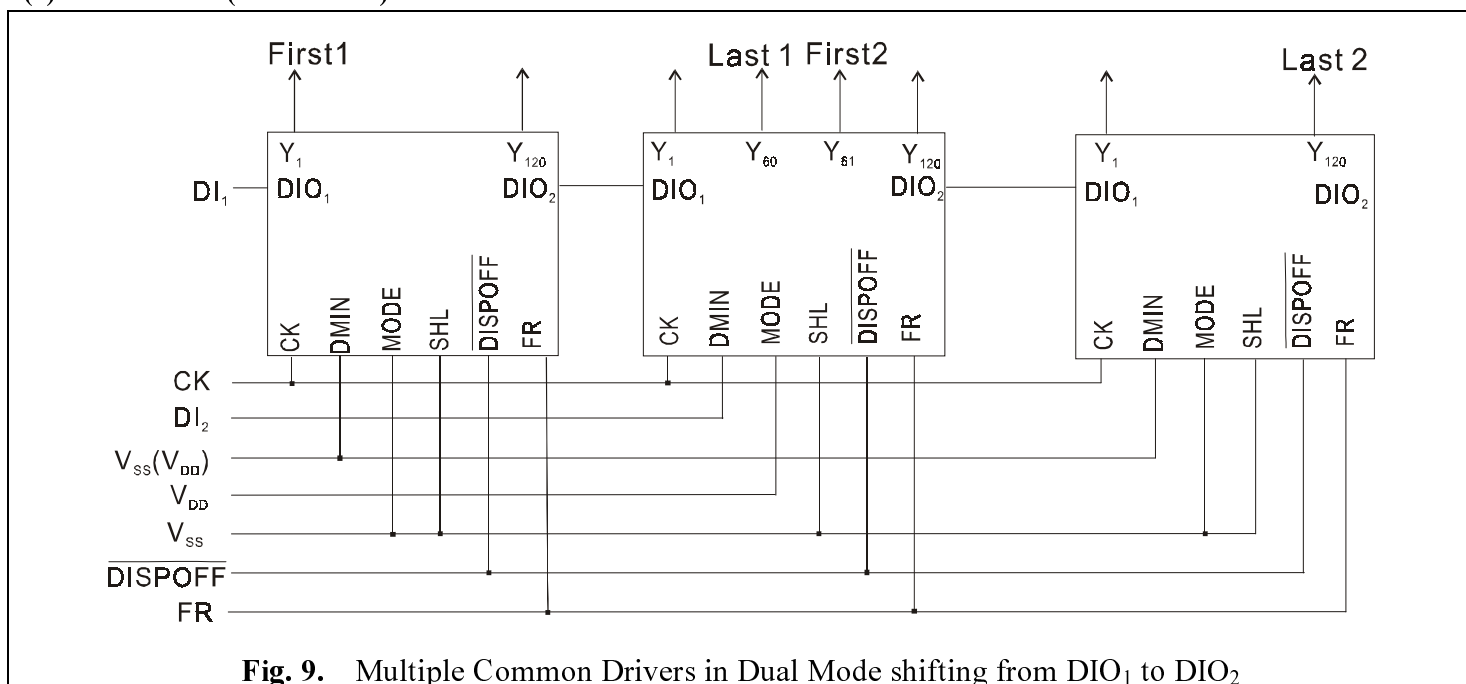
**Fig. 7.** Multiple Common Drivers shifting from DIO<sub>1</sub> to DIO<sub>2</sub>

### (b) Single Mode (SHL= "H")



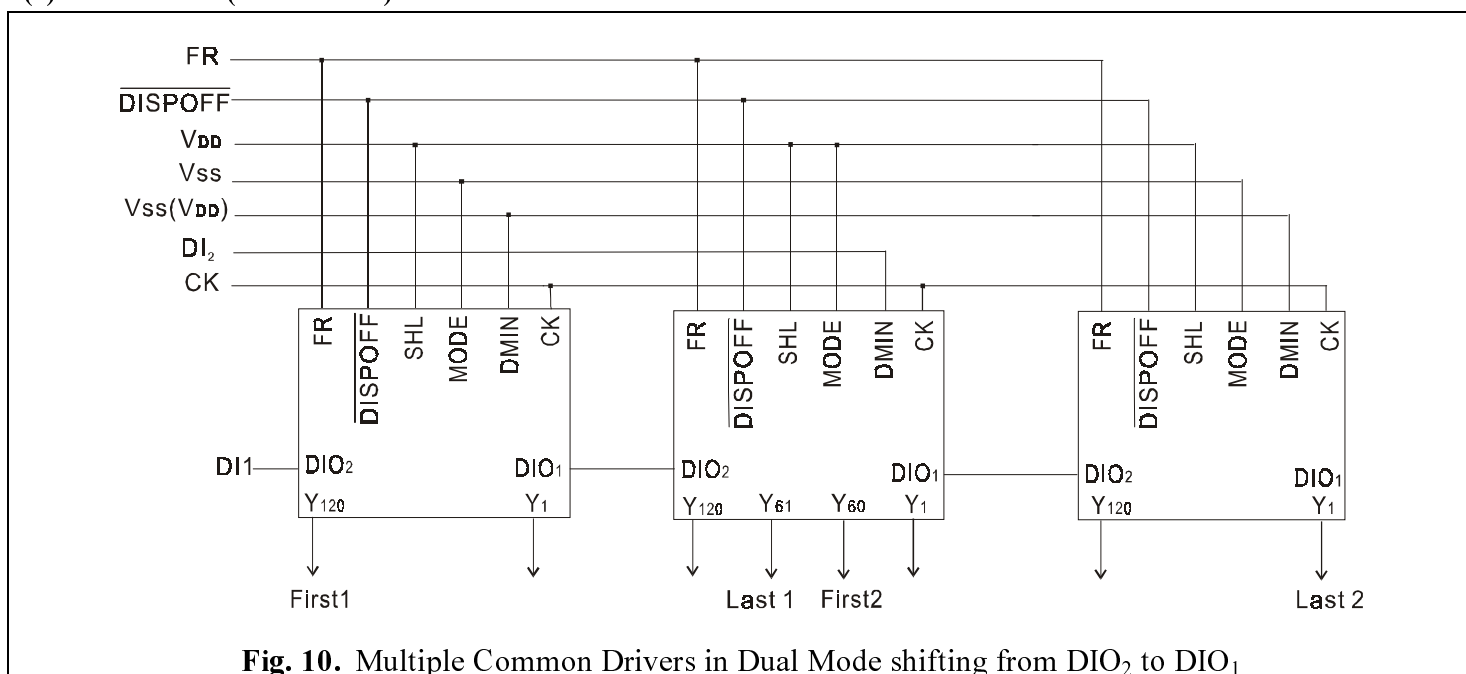
**Fig. 8.** Multiple Common Drivers shifting from DIO<sub>2</sub> to DIO<sub>1</sub>

## (c) Dual Mode (SHL= "L")



**Fig. 9.** Multiple Common Drivers in Dual Mode shifting from DIO<sub>1</sub> to DIO<sub>2</sub>

## (c) Dual Mode (SHL= "H")



**Fig. 10.** Multiple Common Drivers in Dual Mode shifting from DIO<sub>2</sub> to DIO<sub>1</sub>

## PRECAUTIONS

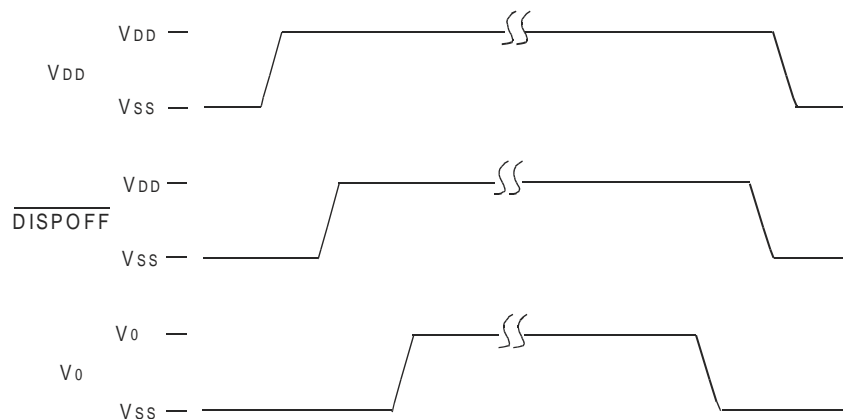
### Precaution when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD driver power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to 100  $\Omega$ ) or fuse to the LCD drive power  $V_0$  of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on  $\overline{\text{DISPOFF}}$  function. After that, cancel the  $\overline{\text{DISPOFF}}$  function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level  $V_5$  on  $\overline{\text{DISPOFF}}$  function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



**Fig. 11.** Power Supply connecting sequence

## ABSOLUTE MAXIMUM RATINGS

**Table 6. Absolute maximum Ratings**

In accordance with the Absolute Maximum Ratings System (IEC 134); See notes 1 and 2

Parameter	Symbol	Applicable Pins	Ratings	Unit	NOTE
Supply voltage(1)	$V_{DD}$	$V_{DD}$	-0.3 to +7.0	V	1, 2
Supply voltage(2)	$V_0$	$V_{0L}, V_{0R}$	-0.3 to +45.0	V	
	$V_1$	$V_{1L}, V_{1R}$	-0.3 to $V_0+0.3$	V	
	$V_4$	$V_{4L}, V_{4R}$	-0.3 to $V_0+0.3$	V	
	$V_5$	$V_{5L}, V_{5R}$	-0.3 to $V_0+0.3$	V	
Input voltage	$V_1$	DIO <sub>1</sub> , DIO <sub>2</sub> , CK, DMIN, SHL, MODE, FR, $\overline{\text{DISPOFF}}$	-0.3 to $V_{DD}+0.3$	V	
Storage temperature	$T_{stg}$		-45 to +125	°C	

### Notes:

1. Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{SS}$  unless otherwise noted.

## RECOMMENDED OPERATING CONDITIONS

**Table 7. Recommended operating conditions**

Parameter	Symbol	Applicable pins	Min.	Typ.	Max.	Unit	NOTE
Supply voltage(1)	$V_{DD}$	$V_{DD}$	+2.5		+5.5	V	1, 2
Supply voltage(2)	$V_0$	$V_{0L}, V_{0R}$	+15.0		+42.0	V	
Operating temperature	$T_{OPR}$		-20		+85	°C	

### Notes:

1. All voltages are with respect to  $V_{SS}$  unless otherwise noted (0 V).
2. Ensure that voltages are set such that  $V_{SS} \leq V_5 < V_4 < V_1 < V_0$ .

## ELECTRICAL CHARACTERISTICS

**Table 8. DC Characteristics**

( $V_{SS}=V_5=0$  V,  $V_{DD}=+2.5$ V to  $+5.5$ V,  $V_0=+15.0$  to  $+40.0$  V,  $T_{OPR}=-20$  to  $+85^{\circ}\text{C}$ )

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit	NOTE
Input “Low” voltage	$V_{IL}$		DIO <sub>1</sub> ,DIO <sub>2</sub> ,CK,DMIN, SHL,MODE,FR, $\overline{\text{DISPOFF}}$			$0.2V_{DD}$	V	
Input “High” voltage	$V_{IH}$			$0.8V_{DD}$			V	
Output “Low” voltage	$V_{OL}$	$I_{OI}=+0.4\text{mA}$	DIO <sub>1</sub> ,DIO <sub>2</sub>			$+0.4$	V	
Output “High” voltage	$V_{OH}$	$I_{OH}=-0.4\text{mA}$		$V_{DD}-0.4$			V	
Input leakage current	$I_{LIL}$	$V_I=V_{SS}$	DIO <sub>1</sub> ,DIO <sub>2</sub> ,CK,DMIN, SHL,MODE,FR, $\overline{\text{DISPOFF}}$			$-10.0$	$\mu\text{A}$	
	$I_{LIH}$	$V_I=V_{DD}$	CK,SHL,MODE,FR, $\overline{\text{DISPOFF}}$			$+10.0$	$\mu\text{A}$	
Input pull-down current	$I_{PD}$	$V_I=V_{DD}$	DIO <sub>1</sub> ,DIO <sub>2</sub> ,DMIN			$100.0$	$\mu\text{A}$	
Output resistance	$R_{ON}$	$ \Delta V_{ON} $ $= 0.5\text{V}$	Y <sub>1</sub> -Y <sub>120</sub>		$0.7$	$1.0$	$\text{K}\Omega$	
					$1.0$	$1.5$		
					$1.5$	$2.0$		
Standby current	$I_{STB}$		$V_{SS}$			$50.0$	$\mu\text{A}$	1
Supply current(1)	$I_{DD}$		$V_{DD}$			$60.0$	$\mu\text{A}$	2
Supply current(2)	$I_0$		$V_{0L}, V_{0R}$			$120.0$	$\mu\text{A}$	2

### Notes:

1.  $V_{DD}=+5.0\text{V}$ ,  $V_0=+40.0\text{V}$ ,  $V_I=V_{SS}$
2.  $V_{DD}=+5.0\text{V}$ ,  $V_0=+40.0\text{V}$ ,  $f_{CK}=41.6\text{kHz}$ ,  $f_{FR}=80\text{Hz}$ , 1/480 duty operation, no-load.

**Table 9. AC Characteristics**

( $V_{SS}=V_5=0$  V,  $V_{DD}=+2.5$  V to  $+5.5$  V,  $V_0=+15.0$  to  $+40.0$  V,  $T_{OPR}=-20$  to  $+85^{\circ}\text{C}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Shift clock period	$t_{CK}$		250			ns
		$V_{DD}=+2.5$ to $\pm 4.5$ V	330			ns
Shift clock "H" pulse width	$t_{WCKH}$	$V_{DD}=+5.0\pm 0.5$ V	15			ns
		$V_{DD}=+2.5$ to $+4.5$ V	30			ns
Data setup time	$t_{SU}$		30			ns
Data Hold time	$t_H$		50			ns
Input signal rise time	$t_R$				50	ns
Input signal fall time	$t_F$				50	ns
$\overline{\text{DISPOFF}}$ removal time	$t_{SD}$		100			ns
$\overline{\text{DISPOFF}}$ "L" pulse width	$t_{WDL}$		1.2			$\mu\text{s}$
Output delay time(1)	$t_D$	$C_L=15\text{pF}$ $V_{DD}=+5.0\pm 0.5$ V			170	ns
		$C_L=15\text{pF}$ $V_{DD}=+2.5$ to $\pm 4.5$ V			250	ns
Output delay time(2)	$t_{PD1}, t_{PD2}$	$C_L=15\text{pF}$			1.2	$\mu\text{s}$
Output delay time(3)	$t_{PD3}$	$C_L=15\text{pF}$			1.2	$\mu\text{s}$

Timing Chart

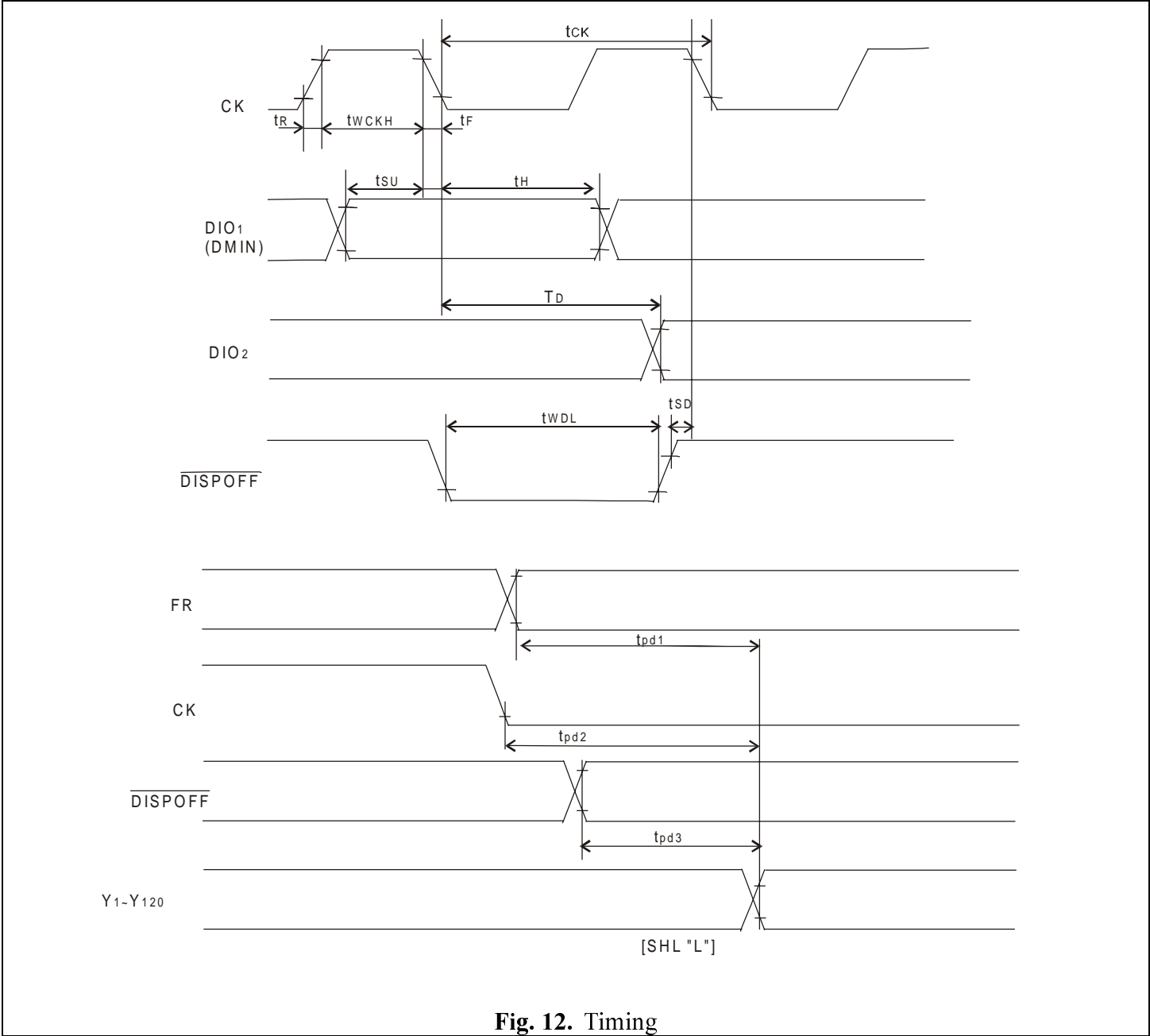


Fig. 12. Timing

## **DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

## **LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Eureka customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Eureka for any damages resulting from such improper use or sale.



## SYSTEM CONFIGURATION EXAMPLE

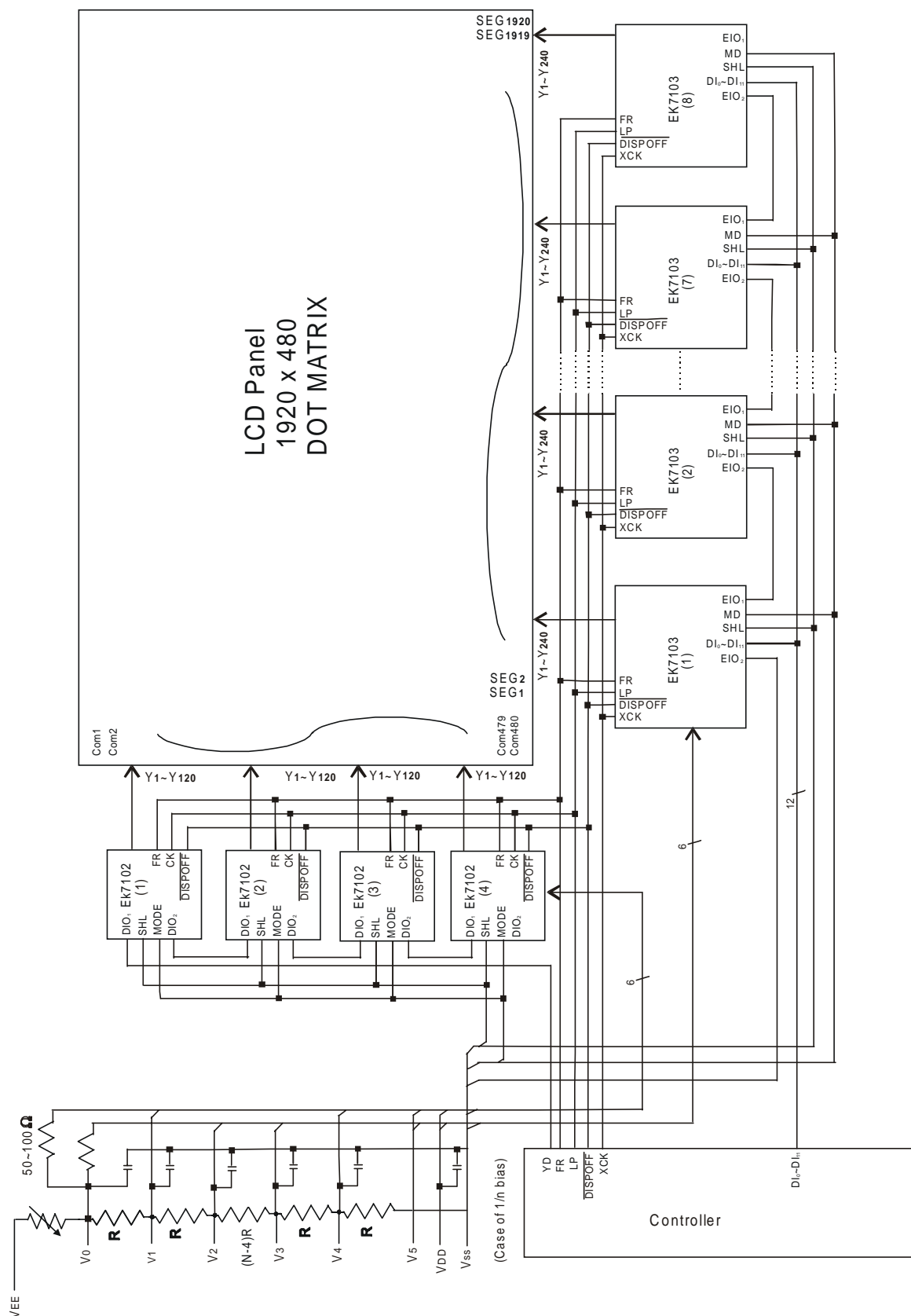


Fig. 13.