Eureka Microelectronics,Inc.

# EK7102CG

## 120 Output Common LCD Driver

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# 120- Output LCD Common Driver IC

## DESCRIPTION

The EK7102 is a 120-output common driver IC suitable for driving dot matrix LCD panels, and it used in personal digital asistant, IA and handheld products. TCP and COG package is available for difference demand, that COG package could be use for customer's system, and the TCP package which is ideal for substantially decreasing the size of the frame section of LCD module. When combined with Eureka's segment drivers, it can create a low power consuming, high resolution LCD Panel.

## FEATURES

- Number of LCD drive outputs：120
- Supply voltage for LCD drive：+15.0 to 40V
- Supply voltage for the logic system ：+2.5 to +5.5V
- Shift clock frequency 4MHz max. at $V_{DD}$=5V
- Low power consumption
- Low output impedance
- Built-in 120-bit bi-directional shift register (divisible into 60 bits x 2 )
- Available in a single mode (120- bit shift register or in a dual mode (60-bit shift register x 2)
  1. $Y_1$ → $Y_{120}$ Single mode
  2. $Y_{120}$ → $Y_1$ Single mode
  3. $Y_1$ → $Y_{60}$, $Y_{61}$ → $Y_{120}$ Dual mode
  4. $Y_{120}$ → $Y_{61}$, $Y_{60}$ → $Y_1$ Dual mode

  The above 4 shift directions are pin-selectable
- Shift register circuits are reset when $\overline{\text{DISPOFF}}$ active
- Package：TCP, COG available

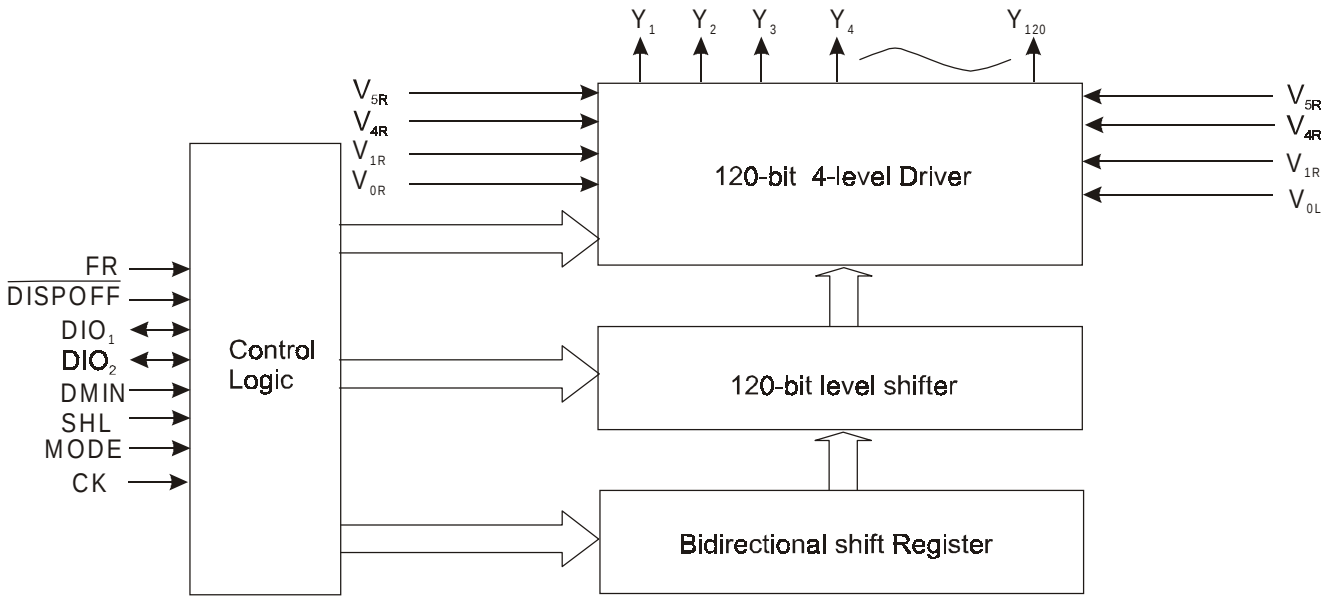


**Fig. 1.** Block diagram

## PINNING INFORMATION

**Table 1. Pin description**

| SYMBOL | I/O | DESCRIPTION |
|---|---|---|
| $Y_1$-$Y_{120}$ | O | LCD drive output |
| $V_{0L}$ | — | Power supply for LCD drive |
| $V_{0R}$ | — | Power supply for LCD drive |
| $V_{1L}$ , $V_{1R}$ | — | Power supply for LCD drive |
| $V_{4L}$ , $V_{4R}$ | — | Power supply for LCD drive |
| $V_{5L}$ , $V_{5R}$ | — | Power supply for LCD drive |
| $V_{SS}$ | — | Ground (0V) |
| $DIO_2$ , $DIO_1$ , | I/O | Shift data input /output for shift register |
| FR | I | AC – converting signal input for LCD drive waveform |
| $\overline{DISPOFF}$ | I | Control input to disable the display |
| SHL | I | Input for selecting the shift direction of shift register |
| MODE | I | Mode selection input |
| DMIN | I | Dual mode data input |
| CK | I | Shift clock input for shift register |
| $V_{DD}$ | — | Power supply for logic system (+2.5 to 5.5 V) |

## FUNCTIONAL DESCRIPTION

**Table 2. Functional description**

| BLOCK | FUNCTION |
|---|---|
| Shift Register | At the falling edge of the CK signal the Shift Register shifts data from the data input pin, to the data output pin under control of the shift direction and mode setting received from the Control Logic block. |
| Level Shifter | The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block. |
| 4-Level Driver | Drives the LCD drive output pins from the shift register data, and selects one of 4 levels ($V_0$,$V_1$,$V_4$ or $V_5$) based on the FR and $\overline{DISPOFF}$ signals |
| Control Logic | Controls the shift register's direction of data shift and mode setting in response to SHL and MODE signal inputs |

## CIRCUIT DIAGRAMS

### Input/Output Circuit

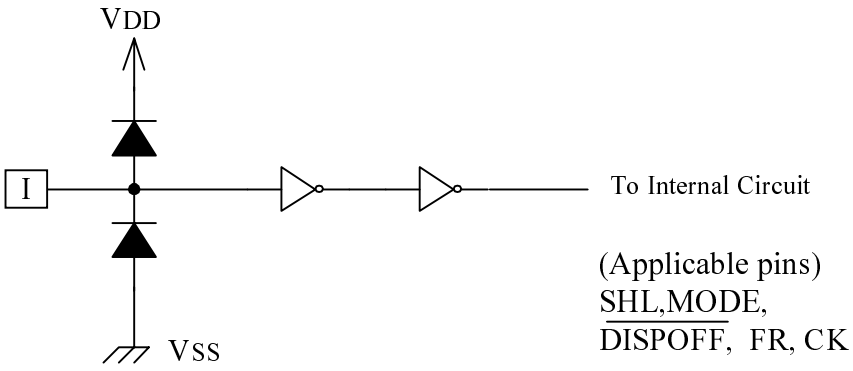


**Fig. 2.** Input Circuit(1)

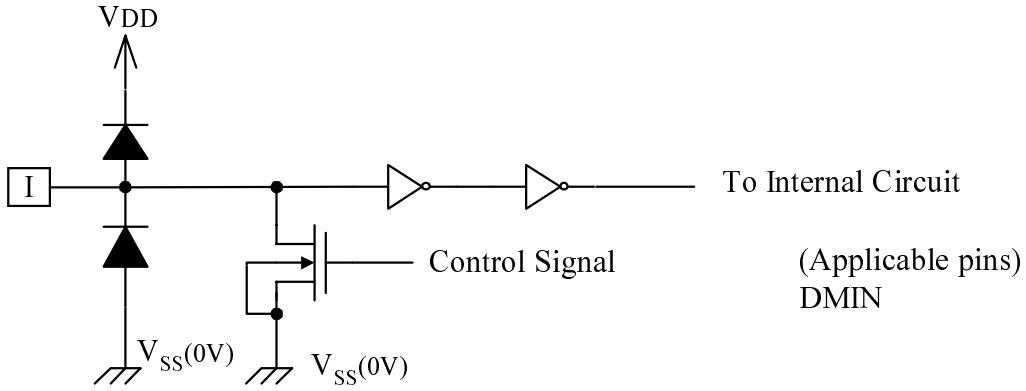


**Fig. 3.** Input Circuit(2)

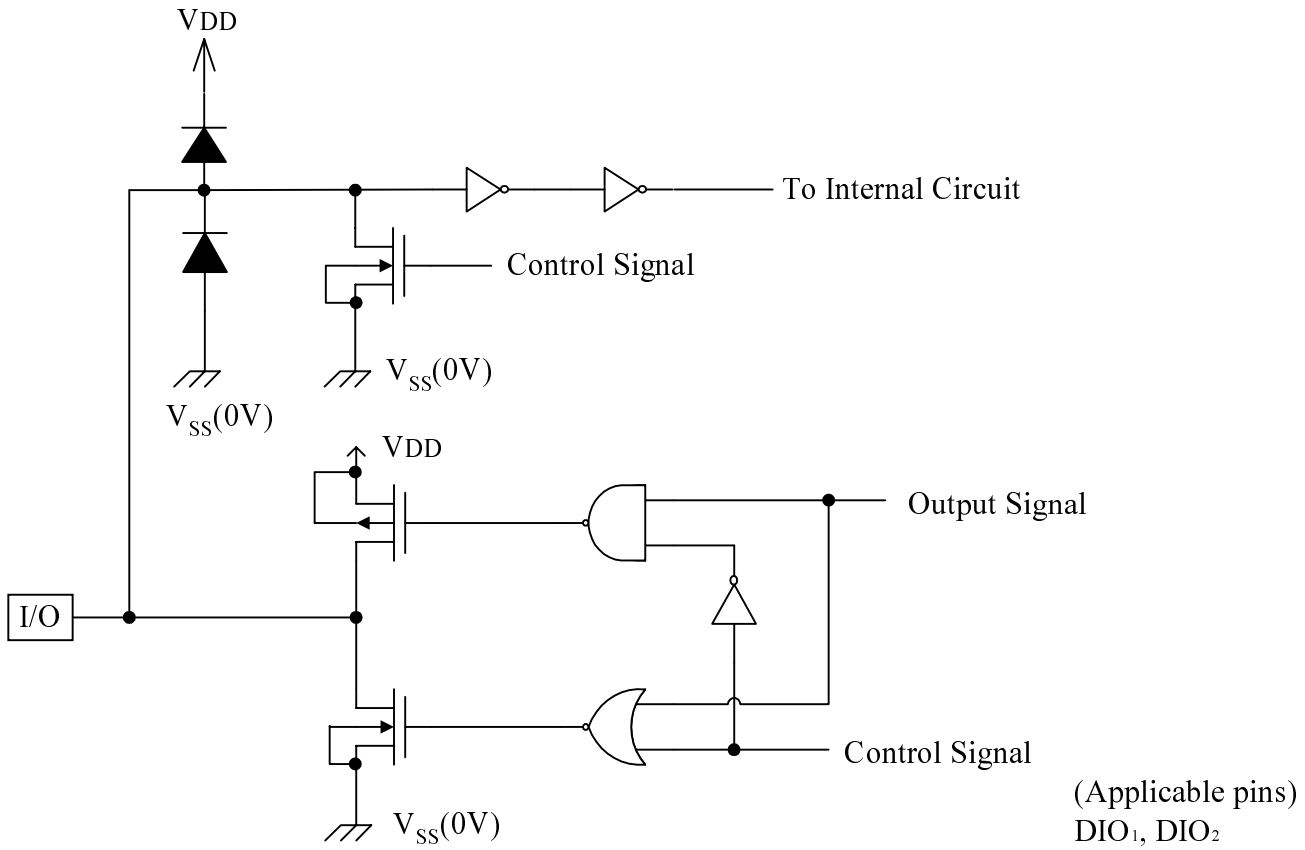


**Fig. 4.** Input/Output Circuit

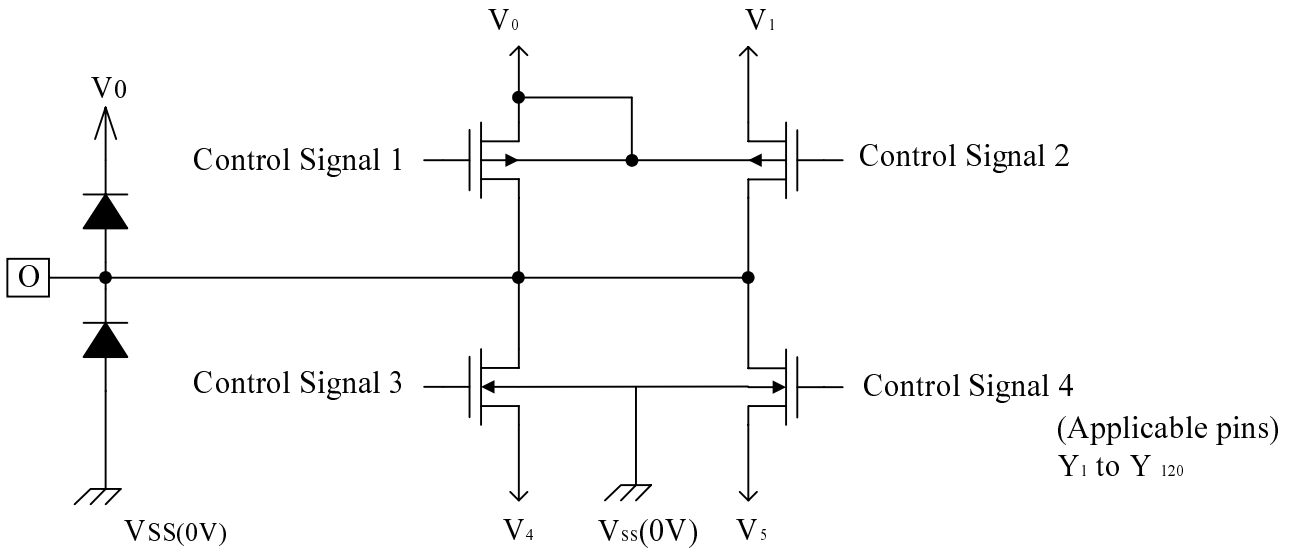


**Fig. 5.** LCD Driver Output Circuit

## PIN DESCRIPTION

**Table 3. Pin Description**

| Symbol | Function |
|---|---|
| $V_{DD}$ | Logic system power supply pin, connected to +2.5 to +5.5 V |
| $V_{SS}$ | Ground pin, connected to 0V. |
| $V_{0L}$,$V_{0R}$<br>$V_{1L}$,$V_{1R}$<br>$V_{4L}$, $V_{4R}$<br>$V_{5L}$, $V_{5R}$ | Power supply pins for LCD drive bias voltage<br>• Normally use a resistor divider to set the bias voltage.<br>• Set the voltages such that Vss ≤ $V_5$<$V_4$<$V_1$<$V_0$.<br>• $Vi_L$ and $Vi_R$ (i=0, 1, 4,5) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin. |
| $DIO_1$ | Shift data input/output pin for bi-directional shift register<br>• Input pin when SHL=L, output pin when SHL=H. When SHL=L, $DIO_1$ is used as input pin, it will be pulled down and the data of $DIO_1$ will be latch at the falling edge of CK. When SHL=H, $DIO_1$ is used as output pin, it won't be pulled down and output data will after the falling edge of CK.<br>• See also Table 5. . |
| $DIO_2$ | Shift data input/output pin for bi-directional shift register<br>• Input pin when SHL=H, output pin when SHL=L.<br>• When SHL=H, $DIO_2$ is used as input pin, it will be pulled down and the data of $DIO_2$ will be latched at the falling edge of CK.<br>When SHL=L, $DIO_2$ is used as output pin, it won't be pulled down and output data will change after the falling edge of CK.<br>• See also Table 5. . |
| CK | Input clock pulse pin to shift the contents of the bi-directional shift register<br>• $DIO_1$ or $DIO_2$ data is shifted at the falling edge of the clock pulse. |
| SHL | Direction selection for reading display data<br>• When SHL is "L".<br>Data is shifted from $DIO_1$ to $Y_1$, $Y_1$ to $Y_2$……$Y_{119}$ to $Y_{120}$ and $DIO_2$.<br>• When SHL is "H".<br>Data is shifted from $DIO_2$ to $Y_{120}$, $Y_{120}$ to $Y_{119}$……$Y_2$ to $Y_1$ and $DIO_1$.<br>• See also Table 5. . |
| $\overline{DISPOFF}$ | Input pin to set all the outputs to non-select level, active low<br>• The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.<br>• When set to Vss level "L", no matter what values in the shift registers , the LCD drive output pins ($Y_1$~$Y_{120}$) are set to level $V_5$ .<br>• When set to "L", the contents of the shift register are reset to not reading data. When the $\overline{DISPOFF}$ function is canceled, the driver outputs non-select level ($V_1$ or $V_4$),and the shift data is read at the next falling edge of the CK. At that time, if $\overline{DISPOFF}$ removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly.<br>• See also Table 4. . |

**Pin Description (Continued)**

| Symbol | Function |
|---|---|
| FR | AC signal input pin for LCD drive waveform. See also Table 4.<br>• The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.<br>• Normally it inputs a frame inversion signal.<br>• The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. |
| MODE | Mode selection input pin. See also Table 5. .<br>• When set to $V_{SS}$ level "L", single mode is selected; when set to $V_{DD}$ level "H", dual mode is selected. |
| DMIN | Dual mode data input pin. See also Table 5. .<br>• According to the data shift direction of the data shift register, data can be input starting from the 61th bit.<br>When the chip is used in dual mode, DMIN will be pulled down.<br>When the chip is used in single mode, DMIN won't be pulled down. |
| $Y_1$-$Y_{120}$ | LCD driver output pins. See also Table 4.<br>• According to each bit of the shift register, one level($V_0$, $V_1$, $V_4$, or $V_5$) is selected and output to LCD panel. |

**Table 4. Logic data to output TRUTH TABLE**

| FR | Latch Data | $\overline{DISPOFF}$ | Driver Output Voltage Level($Y_1$-$Y_{120}$) |
|---|---|---|---|
| L | L | H | $V_4$ |
| L | H | H | $V_0$ |
| H | L | H | $V_1$ |
| H | H | H | $V_5$ |
| X | X | L | $V_5$ |

**Notes**:

- $V_{SS} \leq V_5 < V_4 < V_1 < V_0$, H:$V_{DD}$ (+2.5 to +5.5V), X : Don't care
- "Don't care" means that the inputs should be connected to "H" or "L" Do not leave them open.
  There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage which is assigned by specification for each power pin.

**Table 5. Relationship between the DATA I/O PINS and DATA TRANSFER DIRECTION**

| MODE | SHL | DATA TRANSFER DIRECTION | $DIO_1$ | $DIO_2$ | DMIN |
|---|---|---|---|---|---|
| L (Single) | L | $Y_1$ → $Y_{120}$ | Input | Output | X |
| | H | $Y_{120}$ → $Y_1$ | Output | Input | X |
| H (Dual) | L | $Y_1$ → $Y_{60}$ | Input | Output | Input |
| | | $Y_{61}$ → $Y_{120}$ | | | |
| | H | $Y_{120}$ → $Y_{61}$ | Output | Input | Input |
| | | $Y_{60}$ → $Y_1$ | | | |

**Notes:**

- L : $V_{SS}$ (0V), H : $V_{DD}$ (+2.5 to +5.5V), X : Don't care.
- "Don't care" means that the inputs should be connected to "H" or "L" Do not leave them open.

**Application Examples of Multiple Common Drives**

**(a) Single Mode (SHL= "L")**

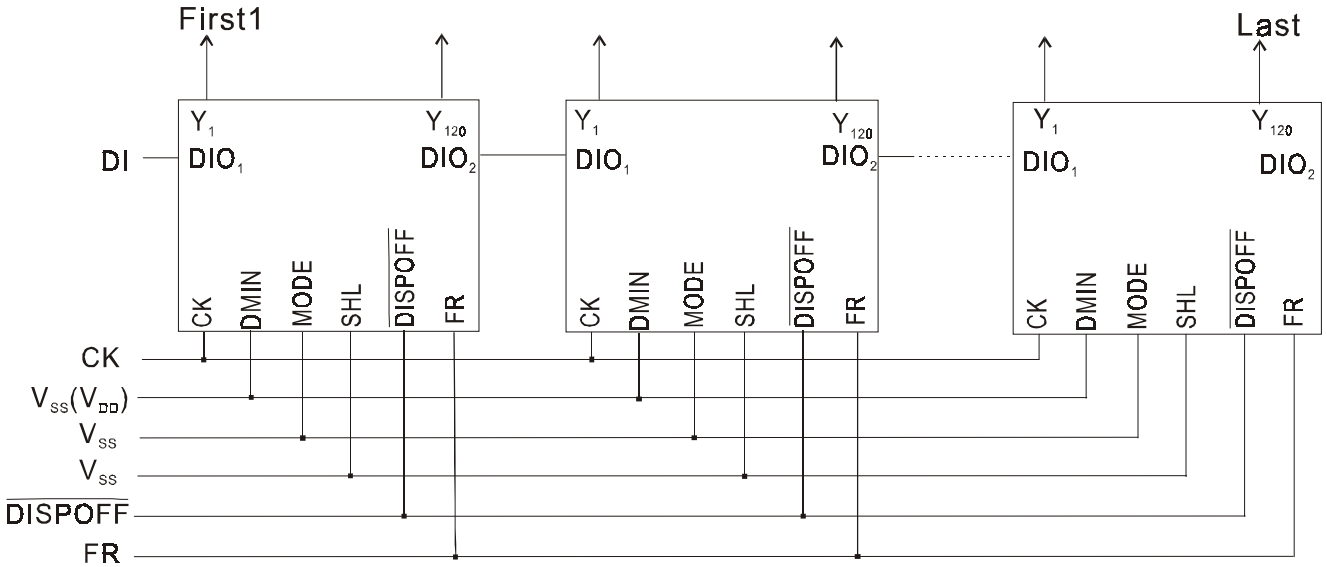


**Fig. 6.** Multiple Common Drivers shifting from $DIO_1$ to $DIO_2$

**(b) Single Mode (SHL= "H")**

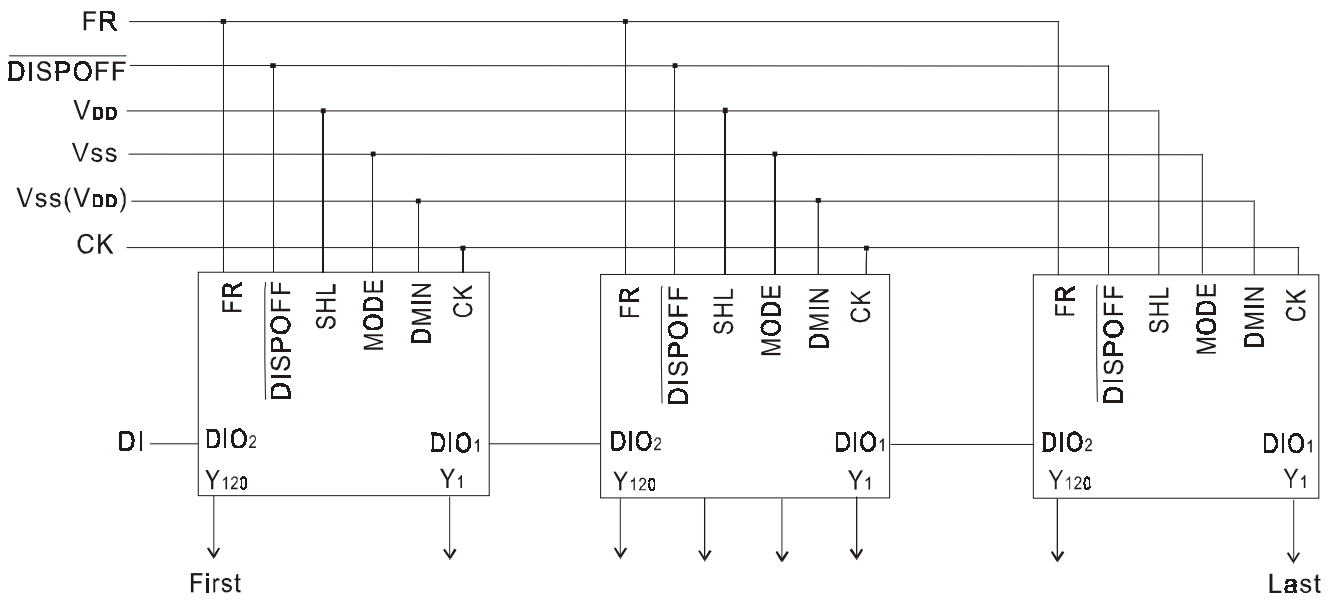


**Fig. 7.** Multiple Common Drivers shifting from $DIO_2$ to $DIO_1$

**(c) Dual Mode (SHL= "L")**

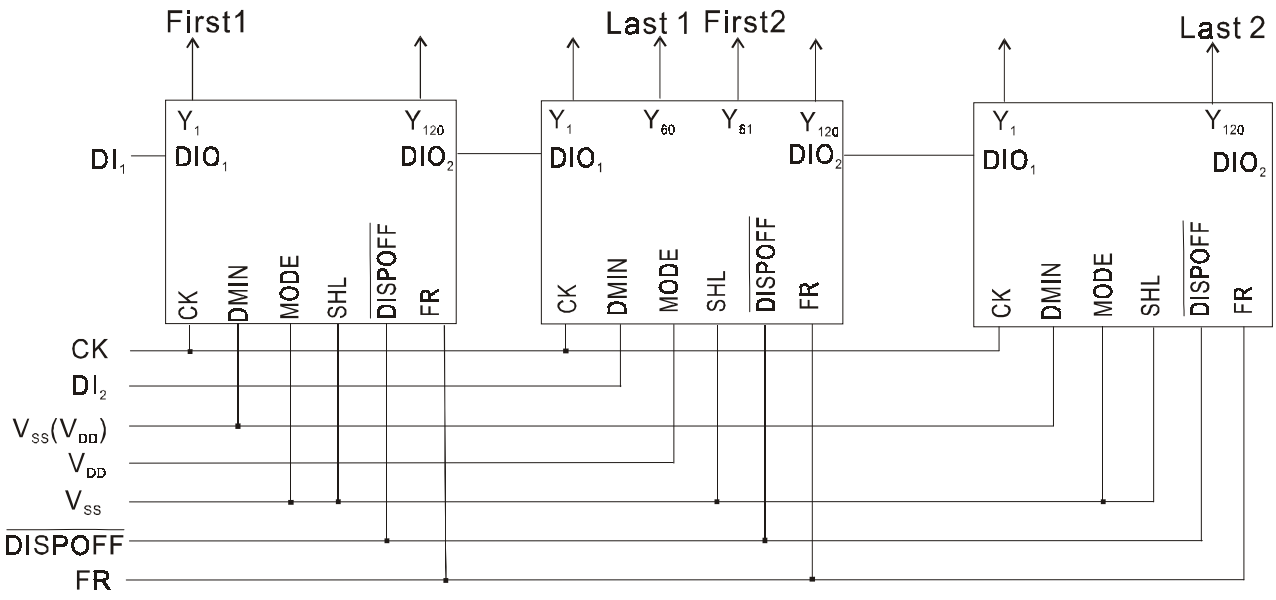


**Fig. 8.** Multiple Common Drivers in Dual Mode shifting from $DIO_1$ to $DIO_2$

**(c) Dual Mode (SHL= "H")**

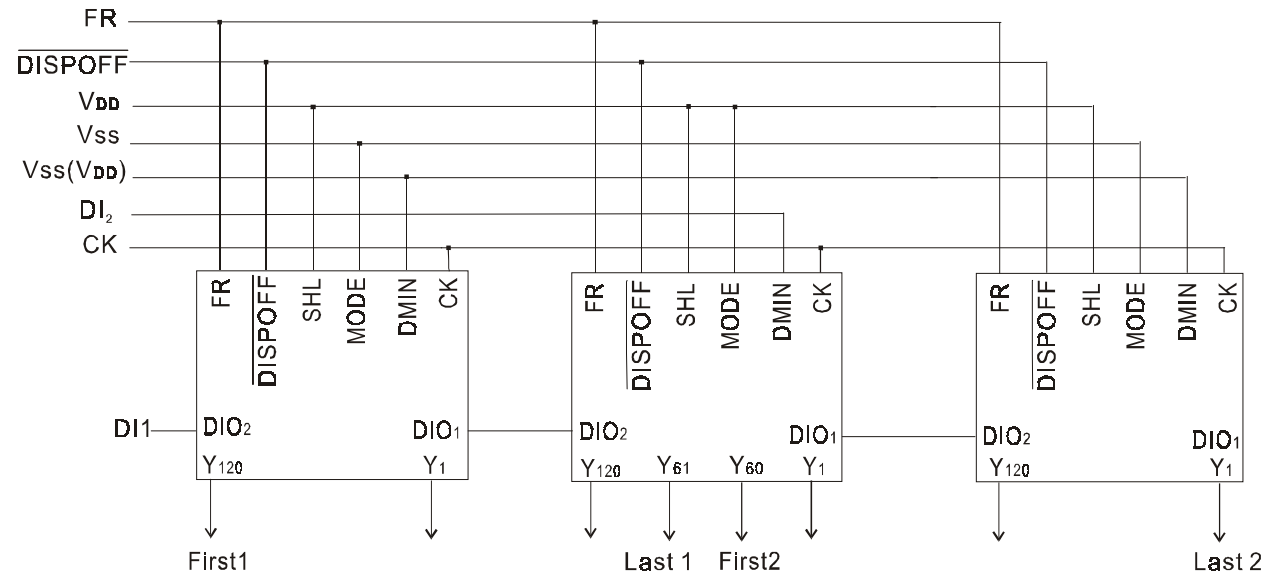


**Fig. 9.** Multiple Common Drivers in Dual Mode shifting from $DIO_2$ to $DIO_1$

**PRECAUTIONS**

**Precaution when connecting or disconnecting the power supply**

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD driver power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to100Ω) or fuse to the LCD drive power $V_0$ of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on $\overline{\text{DISPOFF}}$ function. After that, cancel the $\overline{\text{DISPOFF}}$ function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level $V_5$ on $\overline{\text{DISPOFF}}$ function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.

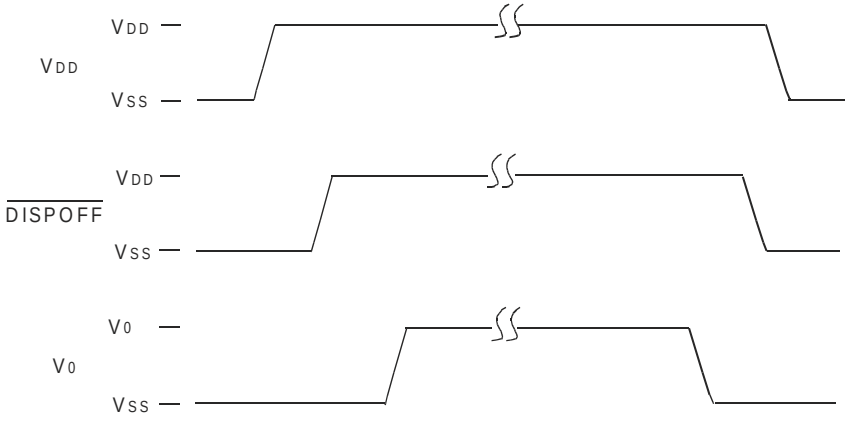


**Fig. 10.** Power Supply connecting sequence

## ABSOLUTE MAXIMUM RATINGS

**Table 6. Absolute maximum Ratings**

In accordance with the Absolute Maximum Ratings System (IEC 134); See notes 1 and 2

| Parameter | Symbol | Applicable Pins | Ratings | Unit | NOTE |
|---|---|---|---|---|---|
| Supply voltage(1) | $V_{DD}$ | $V_{DD}$ | -0.3 to +7.0 | V | 1, 2 |
| Supply voltage(2) | $V_0$ | $V_{0L}$,$V_{0R}$ | -0.3 to +45.0 | V | |
| | $V_1$ | $V_{1L}$,$V_{1R}$ | -0.3 to $V_0$+0.3 | V | |
| | $V_4$ | $V_{4L}$,$V_{4R}$ | -0.3 to $V_0$+0.3 | V | |
| | $V_5$ | $V_{5L}$,$V_{5R}$ | -0.3 to $V_0$+0.3 | V | |
| Input voltage | $V_I$ | $DIO_1$, $DIO_2$, CK, DMIN, SHL, MODE, FR, $\overline{DISPOFF}$ | -0.3 to $V_{DD}$+0.3 | V | |
| Storage temperature | $T_{stg}$ | | -45 to +125 | ℃ | |

**Notes:**

1. Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

## RECOMMENDED OPERATING CONDITIONS

**Table 7. Recommended operating conditions**

| Parameter | Symbol | Applicable pins | Min. | Typ. | Max. | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| Supply voltage(1) | $V_{DD}$ | $V_{DD}$ | +2.5 | | +5.5 | V | 1, 2 |
| Supply voltage(2) | $V_0$ | $V_{0L}$, $V_{0R}$ | +15.0 | | +42.0 | V | |
| Operating temperature | $T_{OPR}$ | | -20 | | +85 | ℃ | |

**Notes:**

1. All voltages are with respect to $V_{SS}$ unless otherwise noted (0 V).
2. Ensure that voltages are set such that $V_{SS} \le V_5 < V_4 < V_1 < V_0$.

## ELECTRICAL CHARACTERISTICS

### Table 8. DC Characteristics

($V_{SS}$=$V_5$=0 V, $V_{DD}$=+2.5V to +5.5V, $V_0$=+15.0 to +40.0 V, $T_{OPR}$=-20 to +85℃)

| Parameter | Symbol | Conditions | Applicable pins | Min. | Typ. | Max. | Unit | NOTE |
|---|---|---|---|---|---|---|---|---|
| Input "Low" voltage | $V_{IL}$ | | $DIO_1$,$DIO_2$,,CK,DMIN, SHL,MODE,FR, $\overline{DISPOFF}$ | | | $0.2V_{DD}$ | V | |
| Input "High" voltage | $V_{IH}$ | | | $0.8V_{DD}$ | | | V | |
| Output "Low" voltage | $V_{OL}$ | $I_{OI}$=+0.4mA | $DIO_1$,$DIO_2$ | | | +0.4 | V | |
| Output "High" voltage | $V_{OH}$ | $I_{OH}$=-0.4mA | | $V_{DD}$-0.4 | | | V | |
| Input leakage current | $I_{LIL}$ | $V_I$=$V_{SS}$ | $DIO_1$,$DIO_2$,,CK,DMIN, SHL,MODE,FR, $\overline{DISPOFF}$ | | | -10.0 | μA | |
| | $I_{LIH}$ | $V_I$=$V_{DD}$ | CK,SHL,MODE,FR, $\overline{DISPOFF}$ | | | +10.0 | μA | |
| Input pull-down current | $I_{PD}$ | $V_I$=$V_{DD}$ | $DIO_1$,$DIO_2$,,DMIN | | | 100.0 | μA | |
| Output resistance | $R_{ON}$ | $\lvert \Delta V_{ON} \rvert$ = 0.5V, $V_0$=+40.0V | $Y_1$-$Y_{120}$ | | 0.7 | 1.0 | KΩ | |
| | | $\lvert \Delta V_{ON} \rvert$ = 0.5V, $V_0$=+30.0V | | | 1.0 | 1.5 | | |
| | | $\lvert \Delta V_{ON} \rvert$ = 0.5V, $V_0$=+20.0V | | | 1.5 | 2.0 | | |
| Standby current | $I_{STB}$ | | $V_{SS}$ | | | 50.0 | μA | 1 |
| Supply current(1) | $I_{DD}$ | | $V_{DD}$ | | | 60.0 | μA | 2 |
| Supply current(2) | $I_0$ | | $V_{0L}$,, $V_{0R}$ | | | 120.0 | μA | 2 |

**Notes:**

1. $V_{DD}$=+5.0V, $V_0$=+40.0V, $V_I$=$V_{SS}$
2. $V_{DD}$=+5.0V, $V_0$=+40.0V, $f_{CK}$=41.6kHz, $f_{FR}$=80Hz, 1/480 duty operation, no-load.

**Table 9. AC Characteristics**

($V_{SS}$=$V_5$=0 V, $V_{DD}$=+2.5V to +5.5V, $V_0$=+15.0 to +40.0 V, $T_{OPR}$=-20 to +85℃)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Shift clock period | $t_{CK}$ | | 250 | | | ns |
| | | $V_{DD}$=+2.5 to±4.5V | 330 | | | ns |
| Shift clock "H" pulse width | $t_{WCKH}$ | $V_{DD}$=+5.0±0.5V | 15 | | | ns |
| | | $V_{DD}$=+2.5 to +4.5V | 30 | | | ns |
| Data setup time | $t_{SU}$ | | 30 | | | ns |
| Data Hold time | $t_H$ | | 50 | | | ns |
| Input signal rise time | $t_R$ | | | | 50 | ns |
| Input signal fall time | $t_F$ | | | | 50 | ns |
| $\overline{DISPOFF}$ removal time | $t_{SD}$ | | 100 | | | ns |
| $\overline{DISPOFF}$ "L"pulse width | $t_{WDL}$ | | 1.2 | | | μs |
| Output delay time(1) | $t_D$ | $C_L$=15pF<br>$V_{DD}$=+5.0±0.5V | | | 170 | ns |
| | | $C_L$=15pF<br>$V_{DD}$=+2.5 to±4.5V | | | 250 | ns |
| Output delay time(2) | $t_{PD1}$, $t_{PD2}$ | $C_L$=15pF | | | 1.2 | μs |
| Output delay time(3) | $t_{PD3}$ | $C_L$=15pF | | | 1.2 | μs |

**Timing Chart**

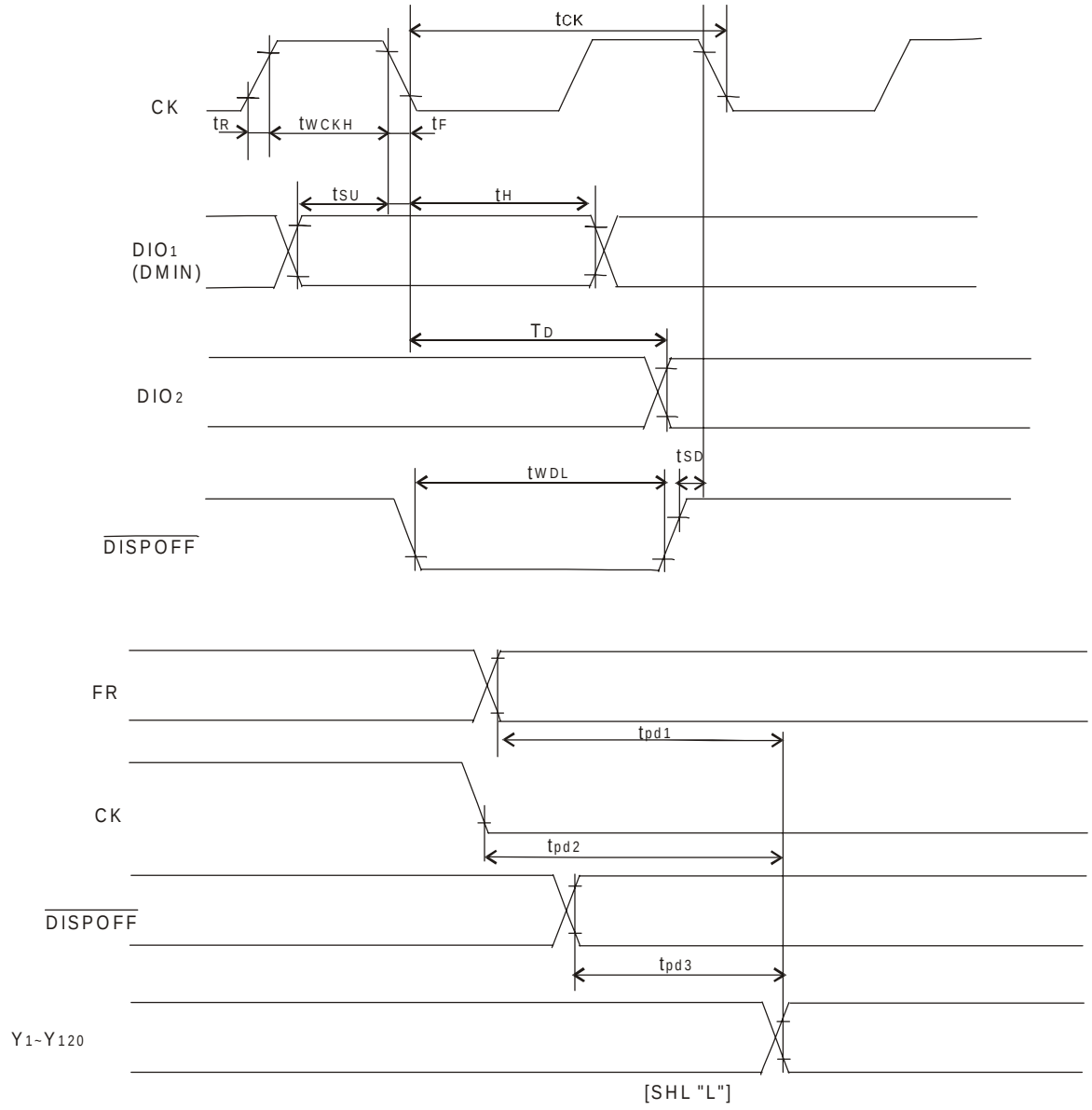


**Fig. 11.** Timing

## SYSTEM CONFIGURATION EXAMPLE

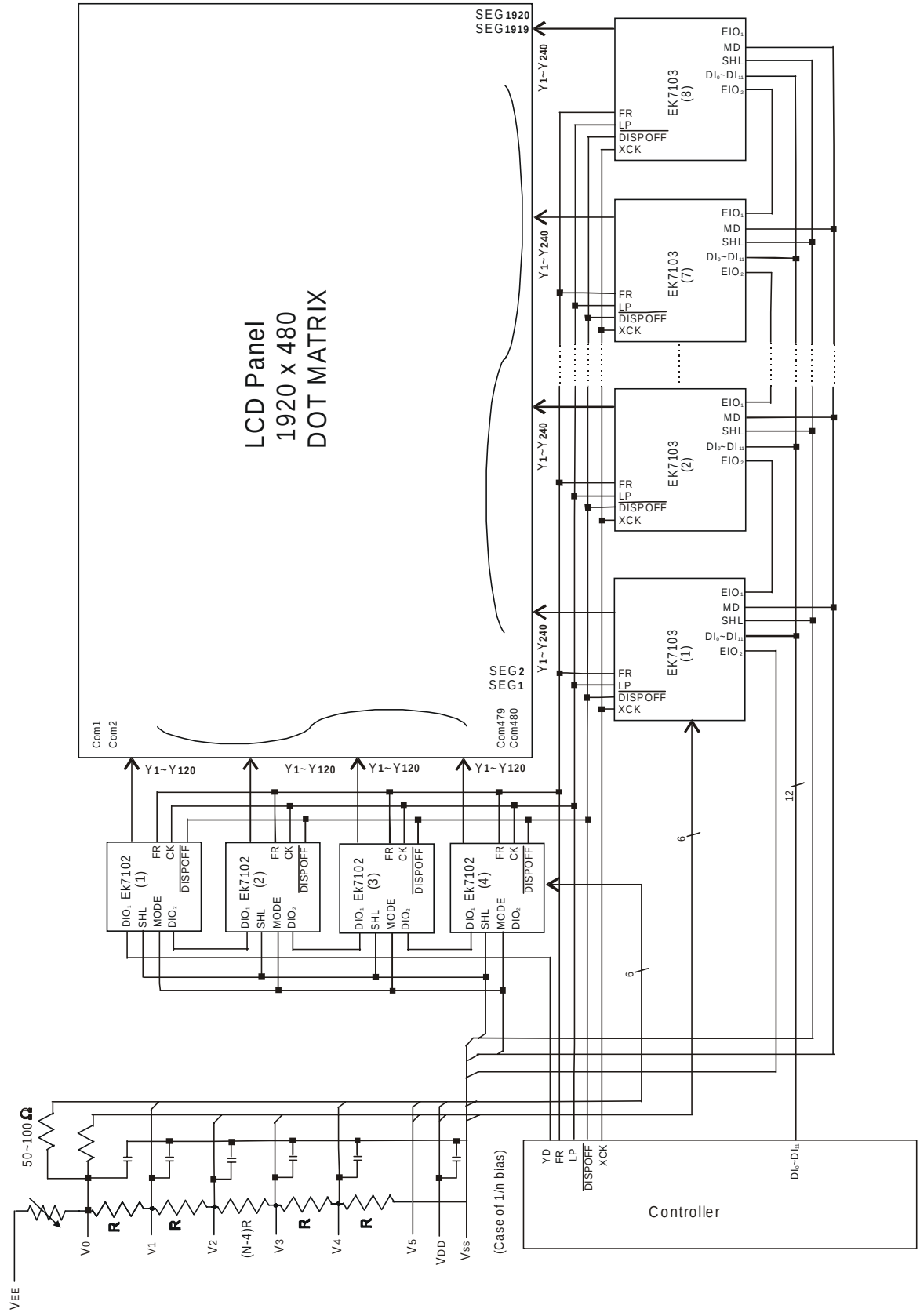


**Fig. 12.**