

Eureka Microelectronics, Inc.



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Data Sheet

EK7010

240 Output Segment/
Common LCD Driver



240 Output Segment/Common LCD Driver

Description

The EK7010 is a 240 output segment/common LCD driver adaptable to drive a large scale dot matrix panel. It uses the Tape Carrier Package(TCP) to greatly reduce the size of the LCD module. EK7010 consumes very little power. Large LCD panels can be assembled by cascading EK7010s. In Segment Mode, the input data can be either 4-bit parallel or 8-bit parallel, selected by the Mode Select pin (MD).

Features

- CMOS process
- Logic power supply : 2.5V to 5.5V
- Low power consumption
- 240 LCD display output
- Supply voltage for LCD driver :15 to 40V
- Package : TCP, COG available

Features in Segment mode

- Shift clock frequency : 20MHz max. at $V_{DD}=5V$
- 4bit/8bit parallel input
- Automatic transfer of enable signal
- Automatic counting in the chip select mode. The internal clock is stopped by automatically counting 240 of input data.

Features in Common mode

- Shift clock frequency : 4MHz max. at $V_{DD}=5V$
- Built-in 240-bit bidirectional shift register
- Single mode (240-bit shift register) or Dual Mode (two 120-bit shift registers) with these options:
 1. $Y1 \rightarrow Y240$ Single mode
 2. $Y240 \rightarrow Y1$ Single mode
 3. $Y1 \rightarrow Y120, Y121 \rightarrow Y240$ Dual mode
 4. $Y240 \rightarrow Y121, Y120 \rightarrow Y1$ Dual mode

Block Diagram

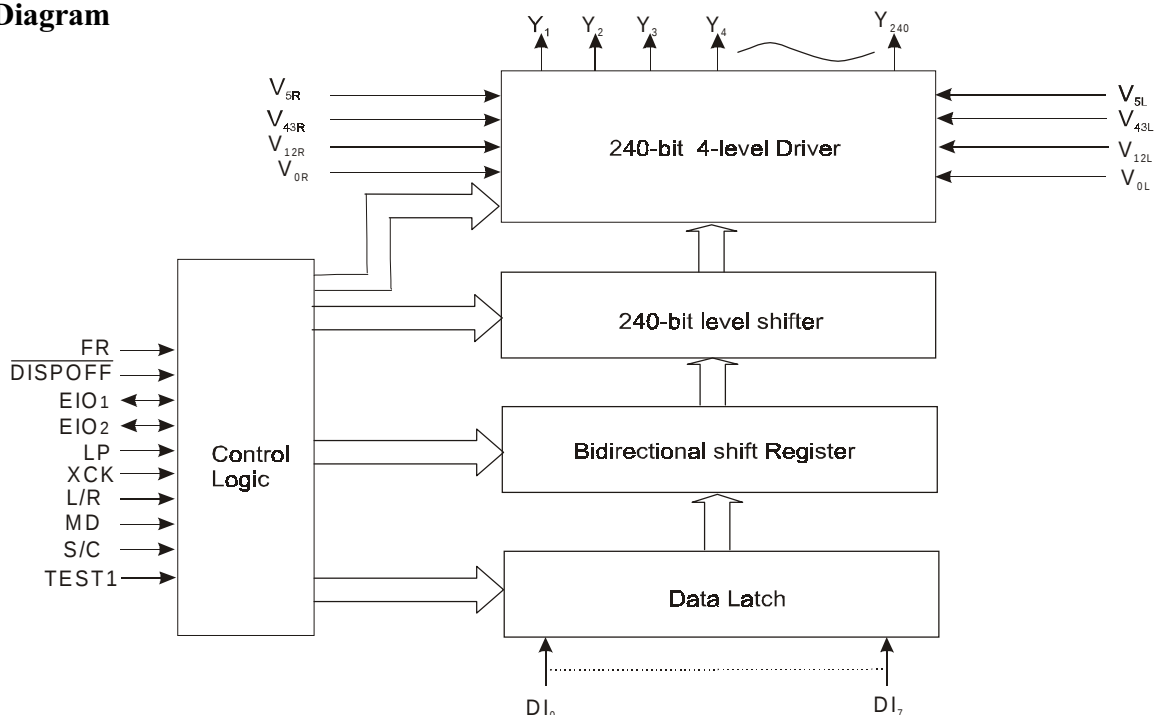


Fig.1
1

Pin Configuration

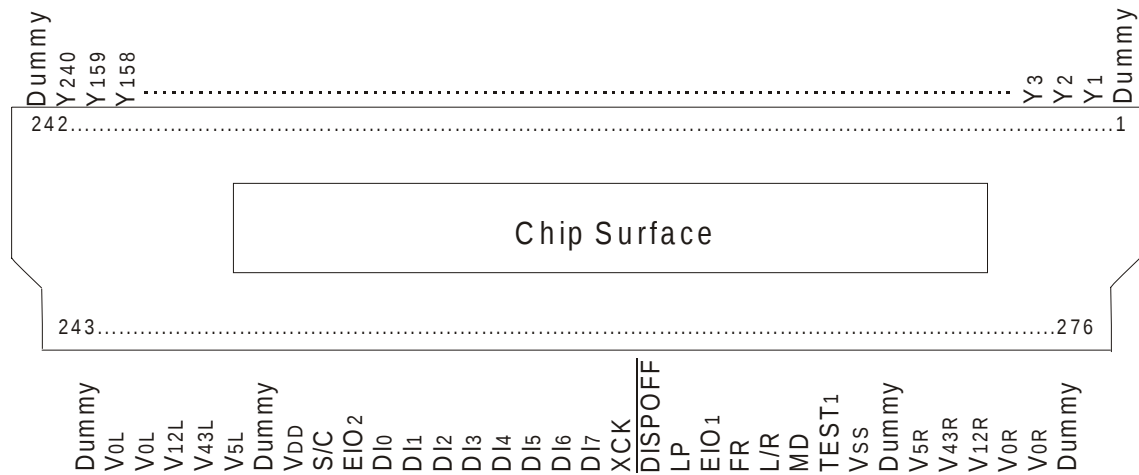


Fig.2

Pin Designations

Pin No.	Symbol	I/O	Designation
2 to 241	Y1-Y240	O	LCD output
244, 245, 274, 275	V0L, V0R	-	Power supply for LCD driver level
246, 273	V12L, V12R	-	Power supply for LCD driver level
247, 272	V43L, V43R	-	Power supply for LCD driver level
248, 271	V5L, V5R	-	Power supply for LCD driver level
269	V _{SS}	-	Display data shift direction selection
250	V _{DD}	-	Power supply for logic circuit(+2.5 to +5.5V)
251	S/C	I	Segment mode/common mode selection
252	EIO2	I/O	Input/output for chip select or data of shift register
253 to 259	DI0-DI6	I	Input display data it for segment mode
260	DI7	I	Input display data for Segment mode, or Dual mode data input for common mode.
261	XCK	I	Display data shift clock input for segment mode
262	$\overline{\text{DISPOFF}}$	I	Control pin input for deselect output
263	LP	I	Latch pulse input in common mode Shift clock input for shift register in segment mode
264	EIO1	I/O	Input/output for chip select or data of shift register in segment mode
265	FR	I	AC-converting signal for LCD driver waveform
266	L/R	I	Mode selection input
267	MD	I	Test mode selection
268	TEST1	I	Test mode selection
1, 242,243, 249, 270, 276	Dummy	-	Dummy PADS

Tab.1

Input/Output Circuit

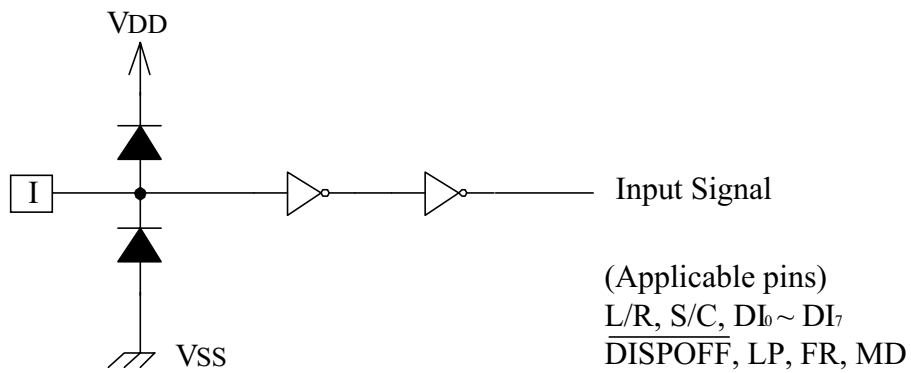


Fig.3 Input Circuit(1)

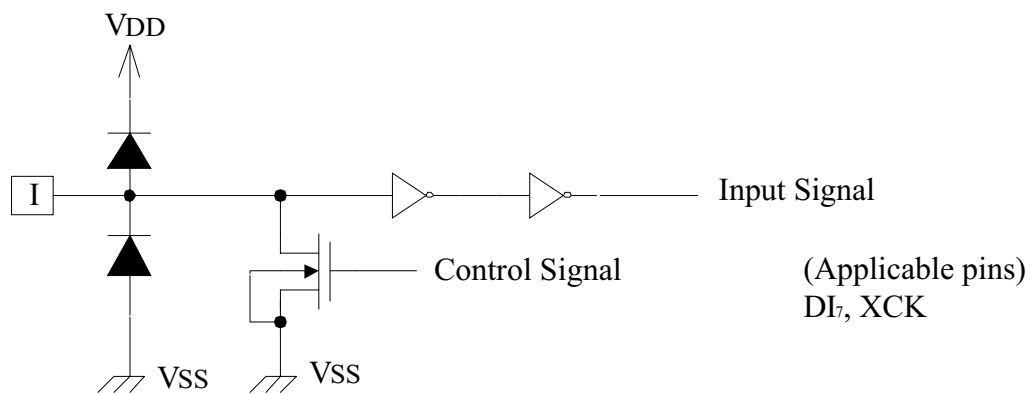


Fig.4 Input Circuit(2)

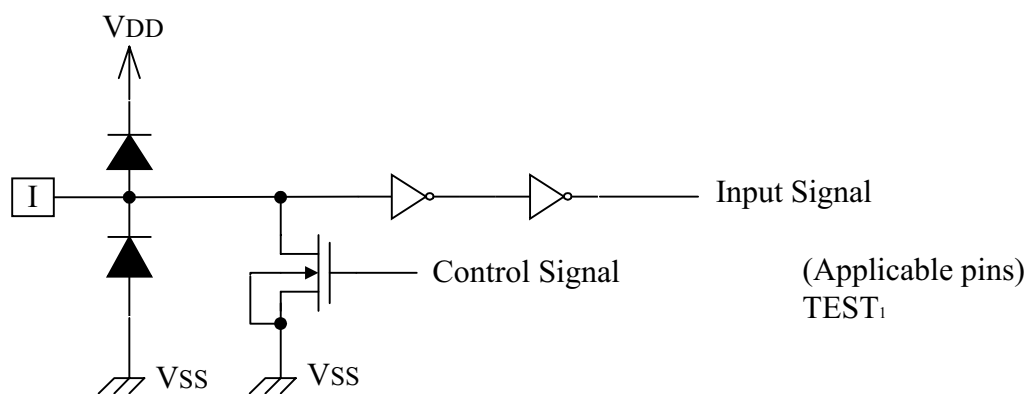


Fig.5 Input Circuit(3)

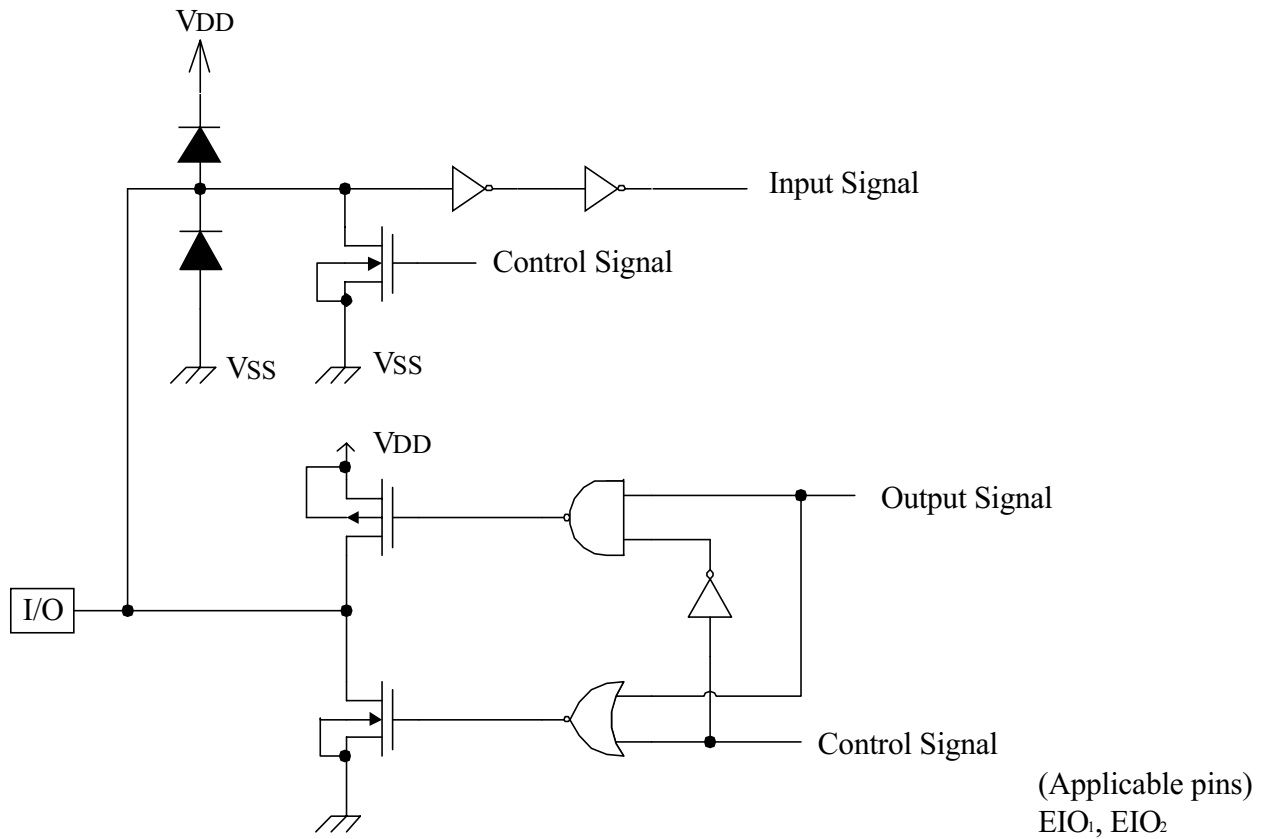


Fig.6 Input/Output Circuit

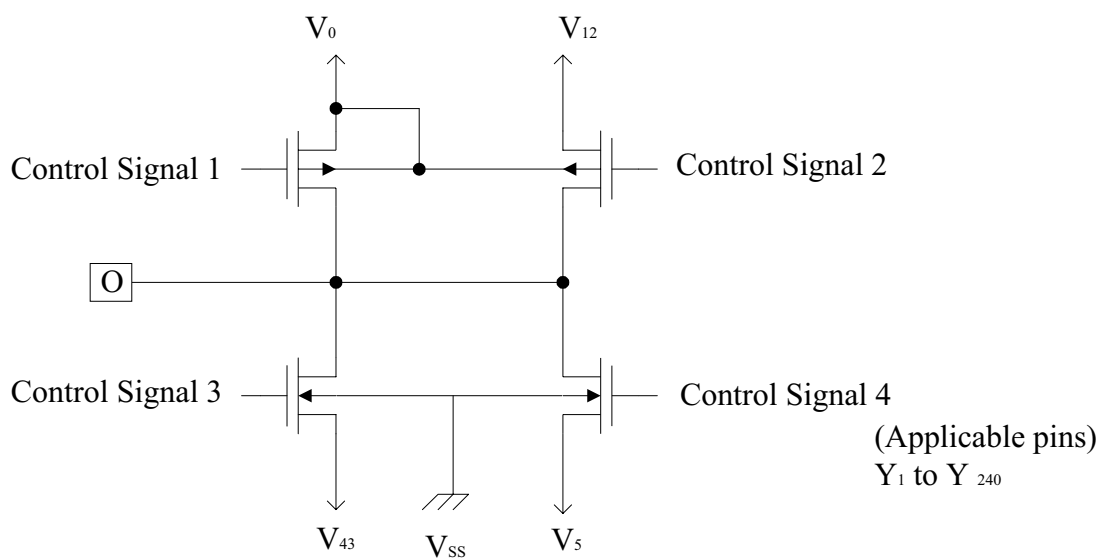


Fig.7 LCD Driver Output Circuit

Pin Functions (Segment mode)

Symbol	Function
V_{DD}	Logic circuit power supply +2.5 to +5.5 V
V_{SS}	Ground pin
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply for LCD driver voltage level ● Normally, the bias voltage used is set by a resistor divider. ● Ensure that voltages are set such that $V_{SS} < V_5 < V_{43} < V_{12} < V_0$. ● V_{iR} and V_{iL} ($i=0, 12, 43, 5$) should be externally connected to reduce the difference between the waveforms of the output pins $Y_1 \sim Y_{240}$.
DI0~DI7	Input for display data ● In 4-bit parallel input mode, input data into the 4 pins DI0~DI3. Connect DI4~DI7 to V_{SS} or V_{DD}. ● In 8-bit parallel input mode, input data into the 8 pins DI0~DI7.
XCK	Input clock pin for displaying data ● Data is read on the falling edge of the clock pulse.
LP	Latch pulse input for displaying data ● Data is latched on the falling edge of the clock pulse.
L/R	Direction selection for reading display data ● When set to V_{SS}, data is read sequentially from Y_{240} to Y_1. ● When set to V_{DD}, data is read sequentially from Y_1 to Y_{240}.
$\overline{DISPOFF}$	Control input to deselect output level ● The input signal is level-shifted from logic voltage level to LC drive voltage level and control LCD drive circuit. ● When set to V_{SS} level "L", the LCD driver output pins ($Y_1 \sim Y_{240}$) are set to level V_5. ● While set to "L", the contents of the line latch are cleared, but read the display data in the data latch regardless of condition of $\overline{DISPOFF}$. When the $\overline{DISPOFF}$ function is cancelled, the driver outputs deselect level (V_{12} or V_{43}), then outputs the contents of the data latch on the next falling edge of the LP. At that time, if $\overline{DISPOFF}$ removal time does not meet the conditions shown in Tab.15, it can not output the reading data correctly.
FR	AC signal for LCD driver output level ● The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. ● Normally, inputs a frame inversion signal. ● The LCD driver output voltage level of output pin can be setted using the line latch output signal and the FR signal. ● Truth table is shown on Tab.6 & Tab.7.

Tab.2

Pin Functions

(Segment mode)

Symbol	Function
MD	Mode selection ● When set to V_{DD} level "H", 4-bit parallel input mode is selected. ● When set to V_{SS} level "L", 8-bit parallel input mode is selected. ● The relationship between the display data and driver output pins is shown on Tab.8 & Tab.9.
S/C	Segment mode/common mode selection pin ● When set to V_{DD} , segment input mode is set.
EIO1 EIO2	Input/Output for chip selection ● When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. ● When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. ● During output, set to "H" while $LP \cdot \overline{XCK}$ is "H" and after 240-bit data have been read, set to "L" for one cycle (from falling edge of XCK to next falling edge of XCK), after which it returns to "H". ● During input, after the LP signal is input, the chip is selected while EI is set to "L". After 240-bits of data have been read, the chip is deselected.
TEST1	Test mode selection ● During normal operation, tie to V_{SS} level "L".
Y_1 - Y_{240}	LCD driver output ● Corresponding directly to each bit of the data latch, one level(V_0 , V_{12} , V_{43} , or V_5) is selected for output. ● Truth table values is shown on Tab.6 & Tab.7 .

Tab.3

Pin Functions (Common mode)

Symbol	Function
V_{DD}	Logic circuit power supply pin connects to +2.5 to +5.5 V.
V_{SS}	Ground pin.
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LCD driver voltage bias ● Normally, the bias voltage is setted by a resistor divider ● Ensure that voltages are setted such that ($V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$) ● V_{iR} and V_{iL} ($i=0, 12, 43, 5$) should be externally connected to reduce the difference between the waveforms of the output pins $Y_1 \sim Y_{240}$.
EIO_1	Bidirectional shift register input/output. ● Output when L/R is setted at V_{SS} level "L", input when L/R is at V_{DD} level "H". ● When EIO_1 is used as input pin, it will be pull-down. ● When EIO_1 is used as output pin, it not be pull-down.
EIO_2	Bidirectional shift register input/output. ● Input when L/R is setted at V_{SS} level "L". output when L/R is at V_{DD} level "H". ● When EIO_2 is used as input, it will be pull-down. ● When EIO_2 is used as output, it will not be pull-down.
LP	Bidirectional shift register clock pulse input ● Data is shifted on the falling edge of the clock pulse.
L/R	Bidirectional shift register shift direction selection ● When set to V_{SS}, data is shifted from Y_{240} to Y_1. ● When set to V_{DD}, data is shifted from Y_1 to Y_{240}.
$\overline{DISPOFF}$	Control input pin to deselect output level ● The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. ● When set to "L", the LCD driver output pins ($Y_1 \sim Y_{240}$) are set to level V_5. ● While set to "L", the contents of the shift register are cleared. When the $\overline{DISPOFF}$ function is canceled, the driver outputs deselect level (V_{12} or V_{43}). and the shift data is read on the falling edge of the LP. At that time, if the $\overline{DISPOFF}$ removal time does not meet the conditions shown in Fig.16, then the shift data is not read correctly.
FR	AC signal input for LCD driver output level ● The input signal is level-shifted from logic voltage level to LCD driver voltage level, and controls LCD drive circuit. ● The LCD driver output voltage level can be set by using the shift register output signal and the FR signal. ● Truth table is shown on Tab.6 & Tab.7.

Tab.4

Pin Functions (Common mode)

Symbol	Function
MD	Mode selection ● When set to V _{SS} level "L", Single Mode operation is selected, when set to V _{DD} level "H", Dual Mode operation is selected.
DI ₇	Dual Mode data input ● According to the data shift direction of the data shift register, data can be input starting from the 121th bit ● When the chip is used as Dual Mode, DI ₇ will be pull-down. ● When the chip is used as Single Mode, DI ₇ will not be pull-down.
S/C	Segment mode/common mode selection ● When set to V _{SS} level "L", Common Mode is setted.
DI ₀ ~DI ₆	Not used ● Connect DI ₀ ~DI ₆ to V _{SS} or V _{DD} . Avoiding floating.
XCK	Not used ● XCK is pull-down in common mode, so connect them to V _{SS} or open.
TEST ₁	Test mode select ● During normal operation, tie to V _{SS} level "L".
Y ₁ ~Y ₂₄₀	LCD driver output ● Corresponding directly to each bit of the shift register, one level (V ₀ , V ₁₂ , V ₄₃ , or V ₅) is selected. ● Truth table is shown on Tab.6 & Tab.7.

Tab.5

Functional Operations

Truth Table

(Segment Mode)

FR	Latch Data	$\overline{\text{DISPOFF}}$	Driver Output Voltage Level(Y_1 - Y_{240})
L	L	H	V ₄₃
L	H	H	V ₅
H	L	H	V ₁₂
H	H	H	V ₀
X	X	L	V ₅

Here, $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, H:V_{DD} (+2.5 to +5.5V), L:V_{SS}(0 V)

X:Don't care

Tab.6

(Common Mode)

FR	Latch Data	$\overline{\text{DISPOFF}}$	Driver Output Voltage Level(Y_1 - Y_{240})
L	L	H	V ₄₃
L	H	H	V ₀
H	L	H	V ₁₂
H	H	H	V ₅
X	X	L	V ₅

Here, $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, H:V_{DD} (+2.5 to +5.5V), L:V_{SS}(0 V)

X:Don't care

Tab.7

Note:There have two kinds of power supply (logic level voltage, LCD drive voltage) for LCD driver.

Supply proper voltage according to each power pin specification.

“Don't care” means that it should be connected to “H” or “L”. Do not leave them open.

Relationship between the Display Data and Driver Output pins

(Segment Mode)

(a)8-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Figure of Clock						
					30 clock	29 clock	28 clock		3 clock	2 clock	1 clock
L	L	Output	Input	DI0	Y1	Y9	Y17		Y217	Y225	Y233
				DI1	Y2	Y10	Y18		Y218	Y226	Y234
				DI2	Y3	Y11	Y19		Y219	Y227	Y235
				DI3	Y4	Y12	Y20		Y220	Y228	Y236
				DI4	Y5	Y13	Y21		Y221	Y229	Y237
				DI5	Y6	Y14	Y22		Y222	Y230	Y238
				DI6	Y7	Y15	Y23		Y223	Y231	Y239
				DI7	Y8	Y16	Y24		Y224	Y232	Y240
L	H	Input	Output	DI0	Y240	Y232	Y224		Y24	Y16	Y8
				DI1	Y239	Y231	Y223		Y23	Y15	Y7
				DI2	Y238	Y230	Y222		Y22	Y14	Y6
				DI3	Y237	Y229	Y221		Y21	Y13	Y5
				DI4	Y236	Y228	Y220		Y20	Y12	Y4
				DI5	Y235	Y227	Y219		Y19	Y11	Y3
				DI6	Y234	Y226	Y218		Y18	Y10	Y2
				DI7	Y233	Y225	Y217		Y17	Y9	Y1

Tab.8

(b)4-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Figure of Clock						
					60 clock	59 clock	58 clock		3 clock	2 clock	1 clock
H	L	Output	Input	DI0	Y1	Y5	Y9		Y229	Y233	Y237
				DI1	Y2	Y6	Y10		Y230	Y234	Y238
				DI2	Y3	Y7	Y11		Y231	Y235	Y239
				DI3	Y4	Y8	Y12		Y232	Y236	Y240
H	H	Input	Output	DI0	Y240	Y236	Y232		Y12	Y8	Y4
				DI1	Y239	Y235	Y231		Y11	Y7	Y3
				DI2	Y238	Y234	Y230		Y10	Y6	Y2
				DI3	Y237	Y233	Y229		Y9	Y5	Y1

Tab.9

(Common Mode)

MD	L/R	Data Transfer Direction	EIO ₁	EIO ₂	DI7
L (Single)	L(shift to left)	$Y_{240} \rightarrow Y_1$	Output	Input	X
	H(shift to right)	$Y_1 \rightarrow Y_{240}$	Input	Output	X
H (Dual)	L(shift to left)	$Y_{240} \rightarrow Y_{121}$ $Y_{120} \rightarrow Y_1$	Output	Input	Input
	H(shift to right)	$Y_1 \rightarrow Y_{120}$ $Y_{121} \rightarrow Y_{240}$	Input	Output	Input

Tab.10

L: V_{SS} (0 V), H: V_{DD} (+2.5V to +5.5V), X: Don't Care

Note: "Don't care" means that it should be connected to "H" or "L". Do not leave them open.

Connection Examples of Plural Segment Drives

(a) Case of L/R="L"

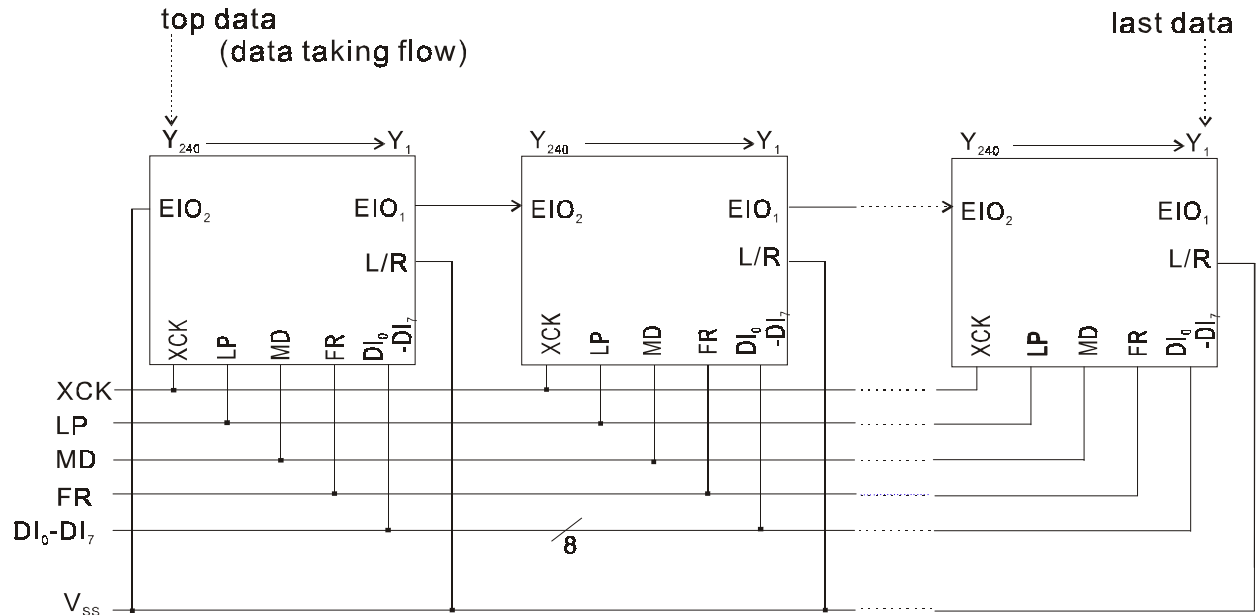


Fig.8

(b) Case of L/R="H"

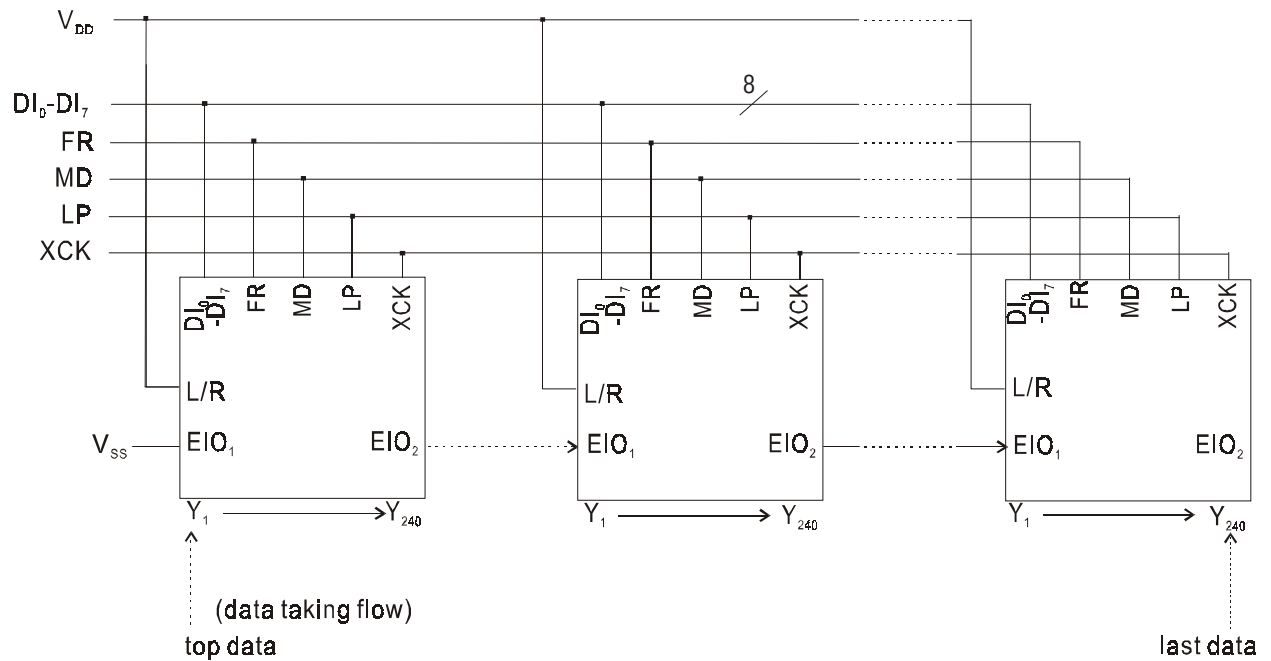


Fig.9

Timing Chart of 4-Device cascade Connection of Segment Drivers

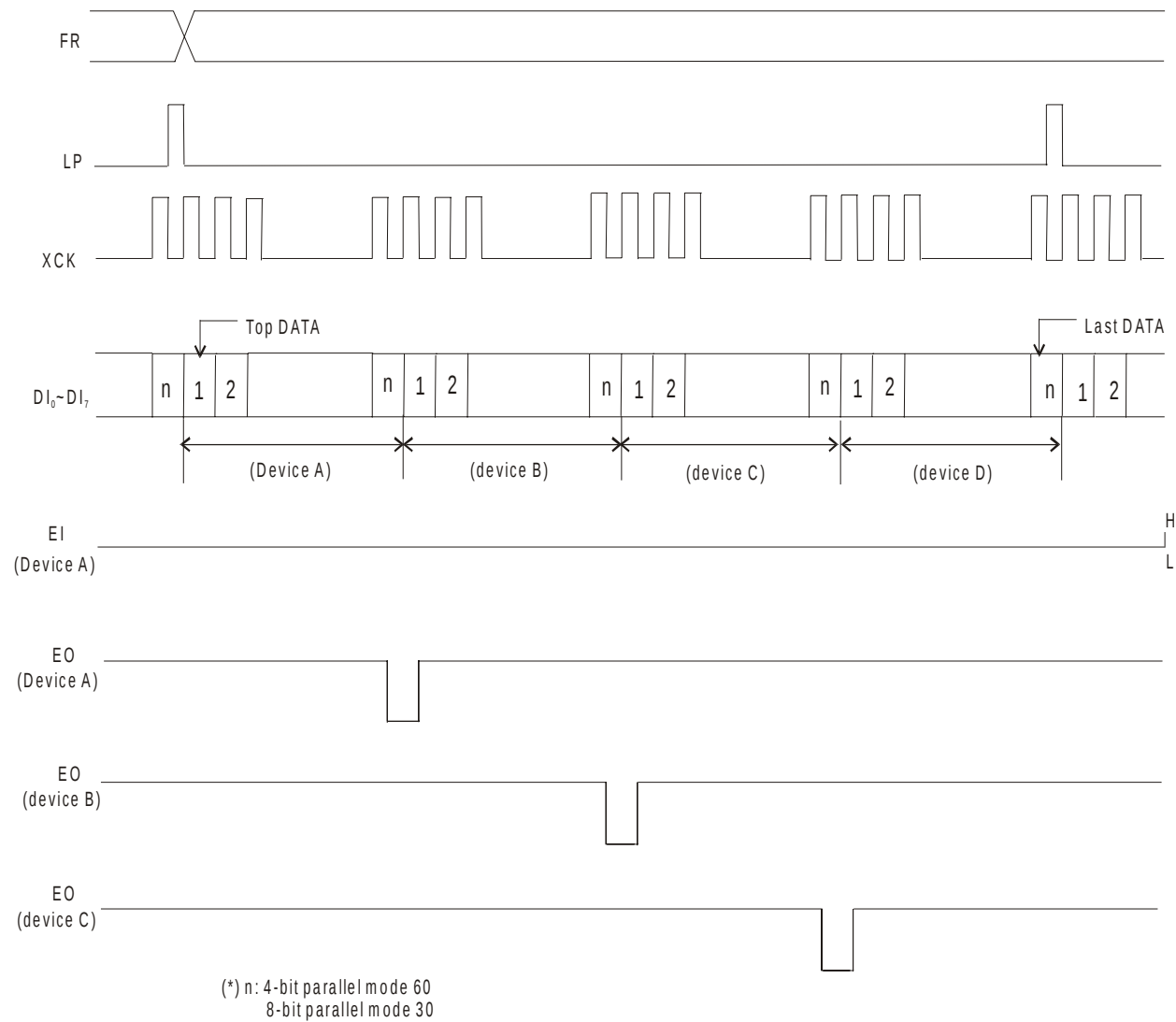


Fig.10

Connection Examples for Plural Common Drivers

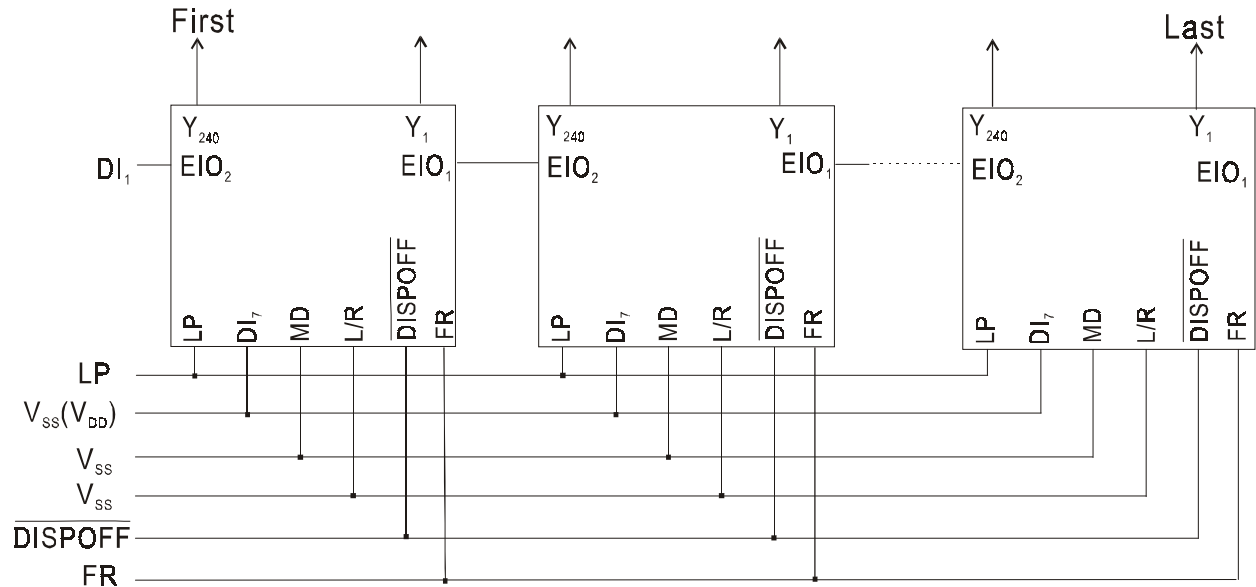


Fig.11 Single Mode (Shifting toward left)

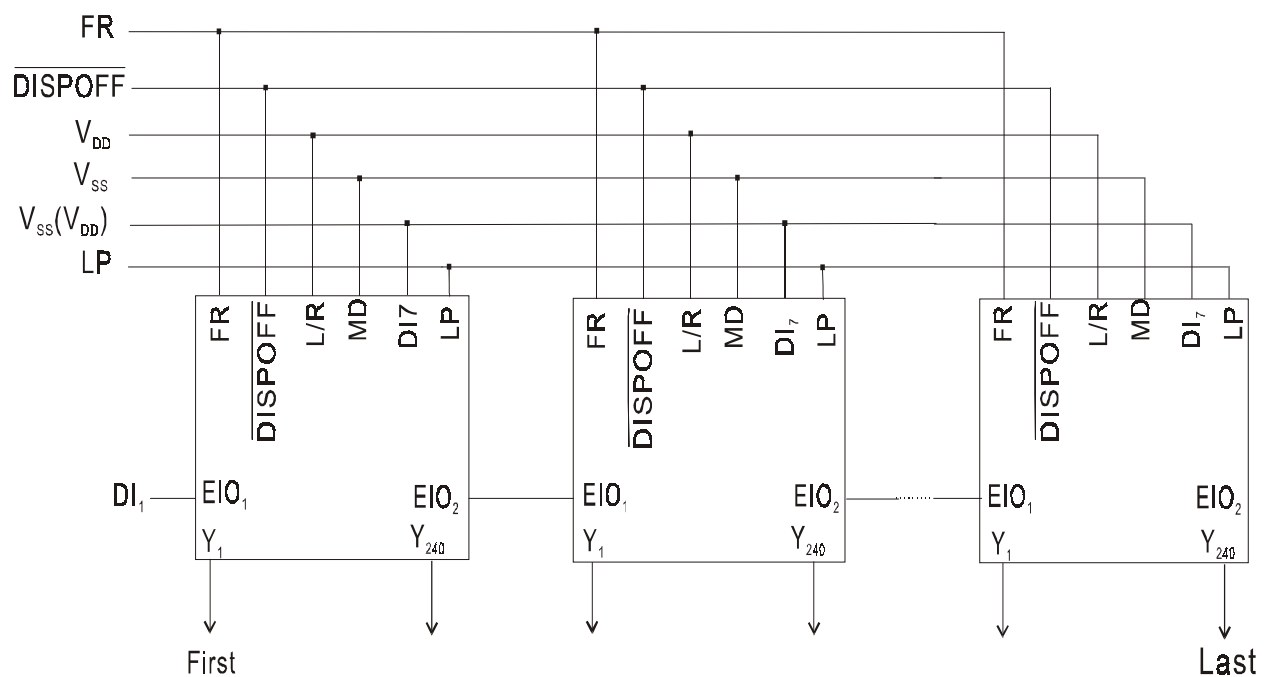


Fig.12 Single Mode (Shifting toward right)

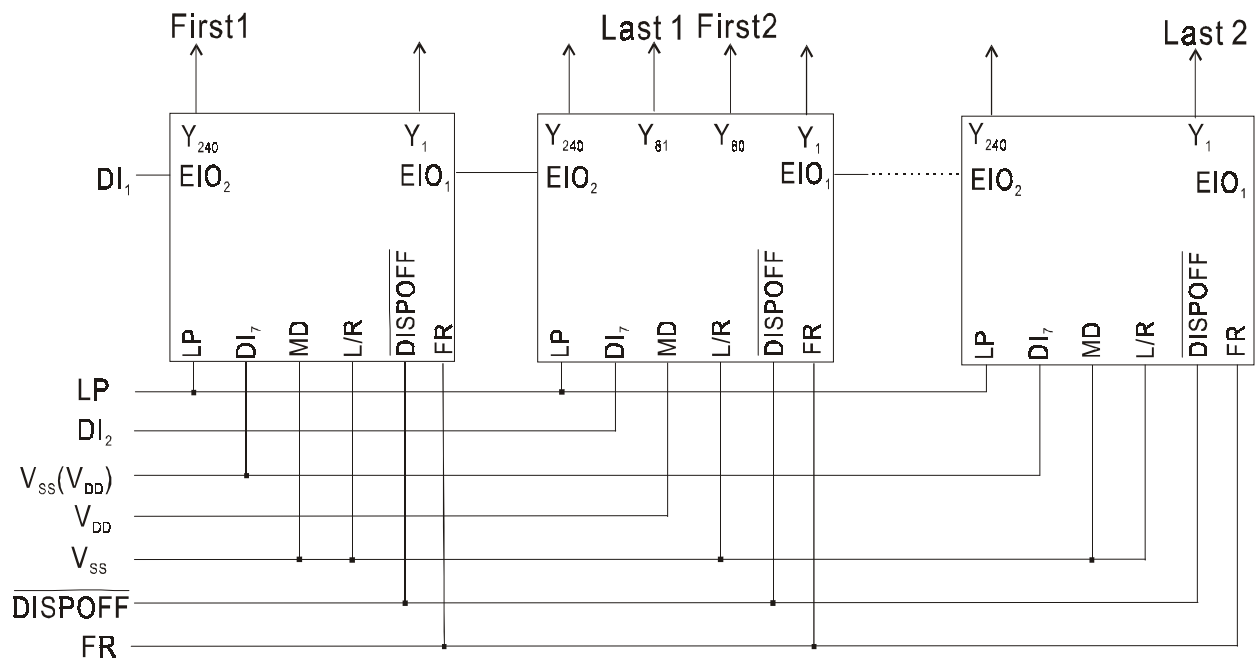


Fig.13 Dual Mode (Shifting toward left)

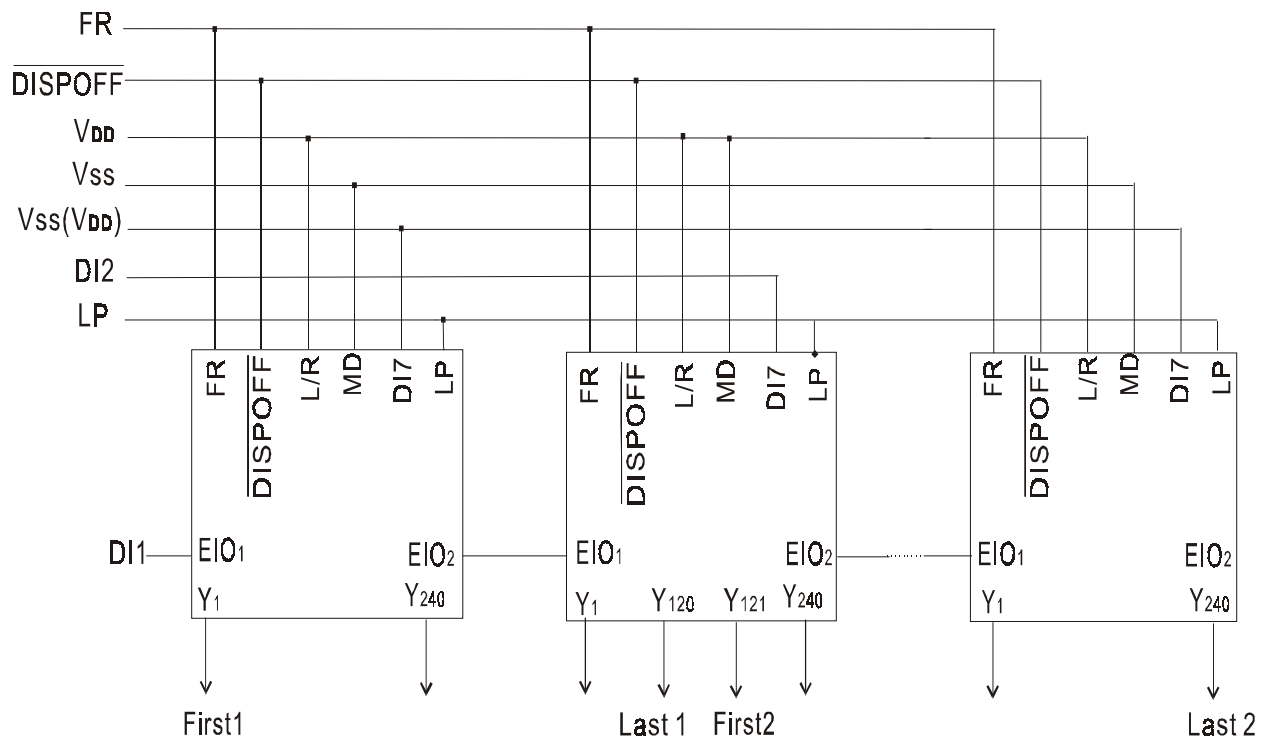


Fig.14 Dual Mode (Shifting toward right)

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable Pins	Ratings	Unit
Supply voltage(1)	V_{DD}	Ta=25°C Referenced to V_{SS} (0 V)	V_{DD}	-0.3 to +7.0	V
Supply voltage(2)	V_0		V_{0L}, V_{0R}	-0.3 to +45.0	V
	V_{12}		V_{12L}, V_{12R}	-0.3 to $V_0+0.3$	V
	V_{43}		V_{43L}, V_{43R}	-0.3 to $V_0+0.3$	V
	V_5		V_{5L}, V_{5R}	-0.3 to $V_0+0.3$	V
Input voltage	V_I		DI ₀₋₇ , XCK, LP, L/R, FR, MD, S/C, EIO ₁ , EIO ₂ , $\overline{\text{DISPOFF}}$	-0.3 to $V_{DD}+0.3$	V
Storage temperature	Tstg			-45 to +125	°C

Tab.11

Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage(1)	V_{DD}	Referenced to V_{SS} (0 V)	V_{DD}	+2.5		+5.5	V
Supply voltage(2)	V_0		V_{0L}, V_{0R}	+15.0		+40	V
Storage temperature	T_{opr}			-20		+85	°C

Tab.12

Note: Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$.

Electrical Characteristics

DC Characteristics

(Segment Mode)

($V_{SS}=V_5=0\text{ V}$, $V_{DD}=+2.5\text{V to }+5.5\text{V}$, $V_0=+15.0\text{ to }+40\text{ V}$, $T_a=-20\text{ to }+85\text{ }^\circ\text{C}$)

Parameter	Symb- ol	Conditions		Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V _{IH}			DI _{0~7} , XCK, LP, L/R, FR, MD, S/C, EIO ₁ , EIO ₂ , DISPOFF	0.8V _{DD}			V
	V _{IL}						0.2V _{DD}	V
Output voltage	V _{OH}	I _{OH} =-0.4mA		EIO ₁ ,EIO ₂	V _{DD} -0.4			V
	V _{OL}	I _{OL} =+0.4mA					+0.4	V
Input leakage current	I _{LIH}	V _I =V _{DD}		DI _{0~7} , XCK, LP, L/R, FR, MD, S/C, EIO ₁ , EIO ₂ , DISPOFF			+10.0	μA
	I _{LIL}	V _I =V _{SS}					-10.0	μA
Output resistance	R _{ON}	ΔV _{ON} =0.5V	V ₀ =+40.0V	Y ₁ ~Y ₂₄₀		1.0	1.5	KΩ
			V ₀ =+30.0V			1.5	2.0	
			V ₀ =+20.0V			2.0	2.5	
Stand-by current	I _{STB}	*1		V _{SS}			75.0	μA
Consumed current(1) (Deselection)	I _{DD1}	*2		V _{DD}			2.0	mA
Consumed current(2) (Selection)	I _{DD2}	*3		V _{DD}			12.0	mA
Consoumed current	I ₀	*4		V ₀			1.5	mA

Tab.13

Note:

*1 $V_{DD}=+5.0\text{V}$, $V_0=+40\text{V}$, $V_I=V_{SS}$.

*2 $V_{DD}=+5.0\text{V}$, $V_0=+40\text{V}$, $f_{XCK}=20\text{MHz}$, No-load, $EI=V_{DD}$.

The input data is turned over by data taking clock (4-bit parallel input mode)

*3 $V_{DD}=+5.0\text{V}$, $V_0=+40\text{V}$, $f_{XCK}=20\text{MHz}$, No-load, $EI=V_{SS}$.

The input data is turned over by data taking clock (4-bit parallel input mode).

*4 $V_{DD}=+5.0\text{V}$, $V_0=+40\text{V}$, $f_{XCK}=20\text{MHz}$, $f_{LP}=41.6\text{KHz}$, $f_{FR}=80\text{Hz}$, No-load.

The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode)

($V_{SS}=V_5=0\text{ V}$, $V_{DD}=+2.5\text{V to }+5.5\text{V}$, $V_0=+15.0\text{ to }+40\text{ V}$, $T_a=-20\text{ to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Conditions		Applicable pins	Min.	Typ.	Max.	Un- it
Input voltage	V _{IH}			DI ₀₋₇ , XCK, LP, L/R, FR, MD, S/C, EIO ₁ , EIO ₂ , <u>DISPOFF</u>	0.8V _{DD}			V
	V _{IL}						0.2V _{DD}	V
Output voltage	V _{OH}	I _{OH} =-0.4mA		EIO ₁ , EIO ₂	V _{DD} -0.4			V
	V _{OL}	I _{OL} =+0.4mA					+0.4	V
Input leakage current	I _{LH}	V _i =V _{DD}		DI ₀₋₆ , LP, L/R, FR, MD, S/C, <u>DISPOFF</u>			+10.0	μA
	I _{LIL}	V _i =V _{SS}		DI ₀₋₇ , XCK, LP, L/R, FR, MD, S/C, EIO ₁ , EIO ₂ , <u>DISPOFF</u>			-10.0	μA
Input pull-down current	I _{PD}	V _i =V _{DD}		XCK,EIO ₁ EIO ₂ , DI ₇			100.0	μA
Output resistance	R _{ON}	ΔV _{ON} =0.5V	V ₀ =+40.0V	Y ₁ ~Y ₂₄₀		1.0	1.5	KΩ
			V ₀ =+30.0V			1.5	2.0	
			V ₀ =+20.0V			2.0	2.5	
Stand-by current	I _{STB}	*1		V _{SS}			75.0	μA
Consumed current(1)	I _{DD}	*2		V _{DD}			120.0	μA
Consumed current(2)	I _O	*2		V ₀			240.0	μA

Tab.14

*1 $V_{DD}=+5.0\text{V}$, $V_0=+40\text{V}$, $V_1=V_{SS}$.

*2 $V_{DD}=+5.0\text{V}$, $V_0=+40\text{V}$, $f_{LP}=41.6\text{KHz}$, $f_{FR}=80\text{Hz}$ case of 1/480 duty operation, No-load.

AC Characteristics

(Segment Mode 1)

($V_{SS}=V_5=0$ V, $V_{DD}=+4.5$ V to $+5.5$ V, $V_0=+15.0$ to $+40$ V, $T_a=-20$ to $+85$ °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	$t_r, t_f \leq 10$ ns	50			ns
Shift clock "H" pulse width	t_{WCKH}		15			ns
Shift clock "L" pulse width	t_{WCKL}		15			ns
Data setup time	t_{DS}		10			ns
Data Hold time	t_{DH}		12			ns
Latch pulse "H" pulse width	t_{WLPH}		15			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		30			ns
Latch pulse rise to Shift clock rise time	t_{LS}		25			ns
Latch pulse fall to Shift clock fall time	t_{LH}		25			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Enable setup time	t_s		10			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			μ s
Output delay time(1)	t_D	$C_L=15$ pF			30	ns
Output delay time(2)	t_{pd1}, t_{pd2}	$C_L=15$ pF			1.2	μ s
Output delay time(3)	t_{pd3}	$C_L=15$ pF			1.2	μ s

Tab.15

Note:

*1 Take the cascade connection into consideration.

*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.

(Segment Mode 2)

($V_{SS}=V_5=0$ V, $V_{DD}=+2.5$ V to $+4.5$ V, $V_0=+15.0$ to $+40$ V, $T_a=-20$ to $+85$ °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	$t_r, t_f \leq 11$ ns	66			ns
Shift clock "H" pulse width	t_{WCKH}		23			ns
Shift clock "L" pulse width	t_{WCKL}		23			ns
Data setup time	t_{DS}		15			ns
Data Hold time	t_{DH}		23			ns
Latch pulse"H"pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		50			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift clock fall time	t_{LH}		30			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Enable setup time	t_s		15			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			μs
Output delay time(1)	t_D	$C_L=15$ pF			41	ns
Output delay time(2)	t_{pd1}, t_{pd2}	$C_L=15$ pF			1.2	μs
Output delay time(3)	t_{pd3}	$C_L=15$ pF			1.2	μs

Tab.16

Note:

*1 Take the cascade connection into consideration.

*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.

(Segment Mode 3)

($V_{SS}=V_5=0$ V, $V_{DD}=+2.5$ V to $+3.0$ V, $V_0=+15.0$ to $+40$ V, $T_a=-20$ to $+85$ °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	$t_r, t_f \leq 11$ ns	82			ns
Shift clock "H" pulse width	t_{WCKH}		28			ns
Shift clock "L" pulse width	t_{WCKL}		28			ns
Data setup time	t_{DS}		20			ns
Data Hold time	t_{DH}		23			ns
Latch pulse "H" pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		65			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift clock fall time	t_{LH}		30			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Enable setup time	t_s		15			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			μs
Output delay time(1)	t_D	$C_L=15$ pF			57	ns
Output delay time(2)	t_{pd1}, t_{pd2}	$C_L=15$ pF			1.2	μs
Output delay time(3)	t_{pd3}	$C_L=15$ pF			1.2	μs

Tab.17

Note:

*1 Take the cascade connection into consideration.

*2 $(t_{CK}-t_{WCKH}-t_{WCKL})/2$ is maximum in the case of high speed operation.

(Timing Characteristics of Segment Mode)

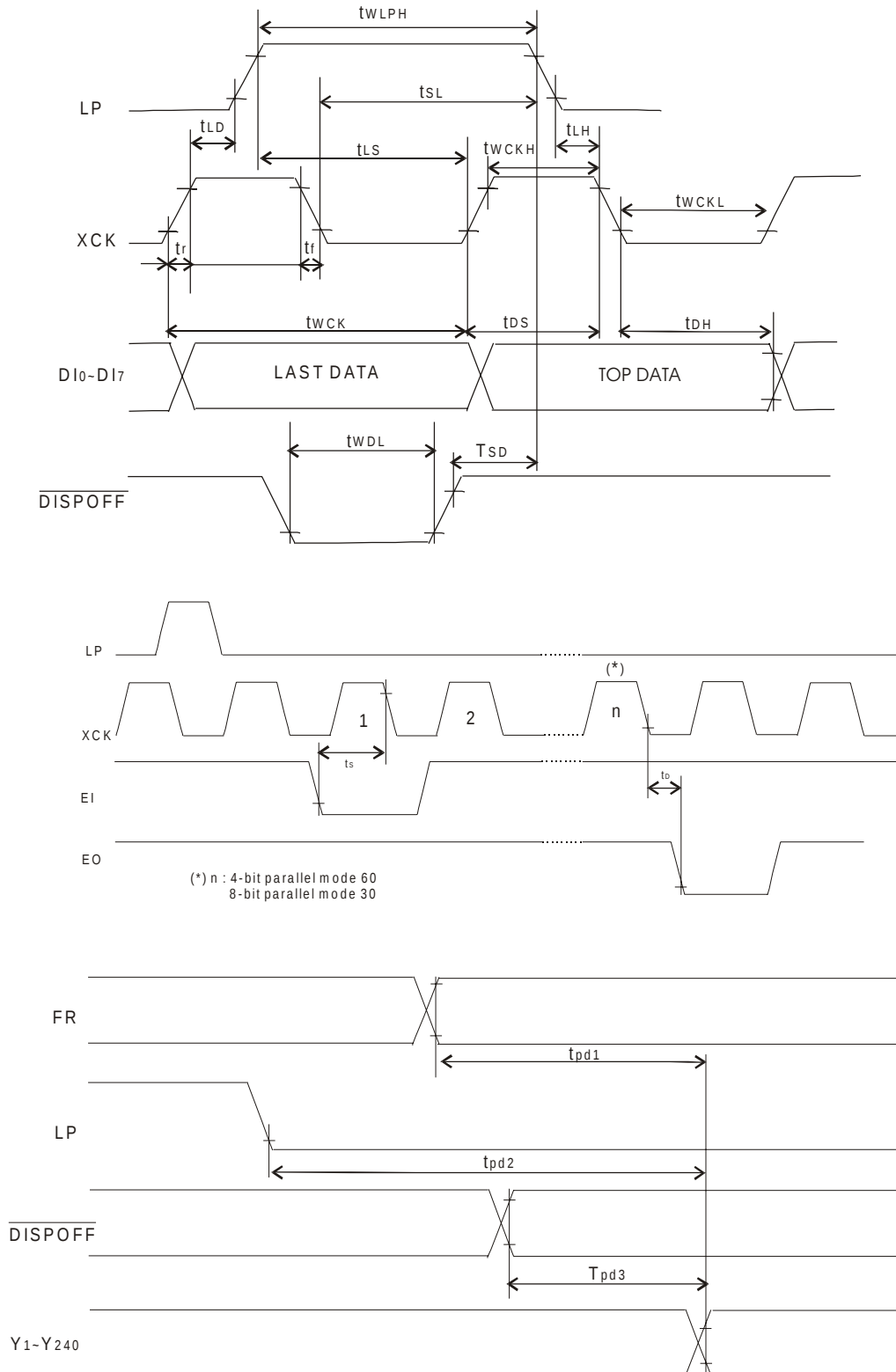


Fig.15

(Common Mode)

($V_{SS}=V_5=0$ V, $V_{DD}=+2.5$ V to $+5.5$ V, $V_0=+15.0$ to $+40$ V, $T_a=-20$ to $+85$ °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	t_{WLP}	$t_r, t_f \leq 20$ ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	$V_{DD}=+5.0V \pm 10\%$	15			ns
		$V_{DD}=+2.5V \sim +4.5V$	30			
Data setup time	t_{SU}		30			ns
Data Hold time	t_H		50			ns
Input signal rise time	t_r				50	ns
Input signal fall time	t_f				50	ns
$\overline{DISPOFF}$ removal time	t_{SD}		100			ns
$\overline{DISPOFF}$ " L " pulse width	t_{WDL}		1.2			μs
Output delay time(1)	t_{DL}	$C_L=15pF$			200	ns
Output delay time(2)	t_{pd1}, t_{pd2}	$C_L=15pF$			1.2	μs
Output delay time(3)	t_{pd3}	$C_L=15pF$			1.2	μs

Tab.17

(Timing Characteristics of Common Mode)

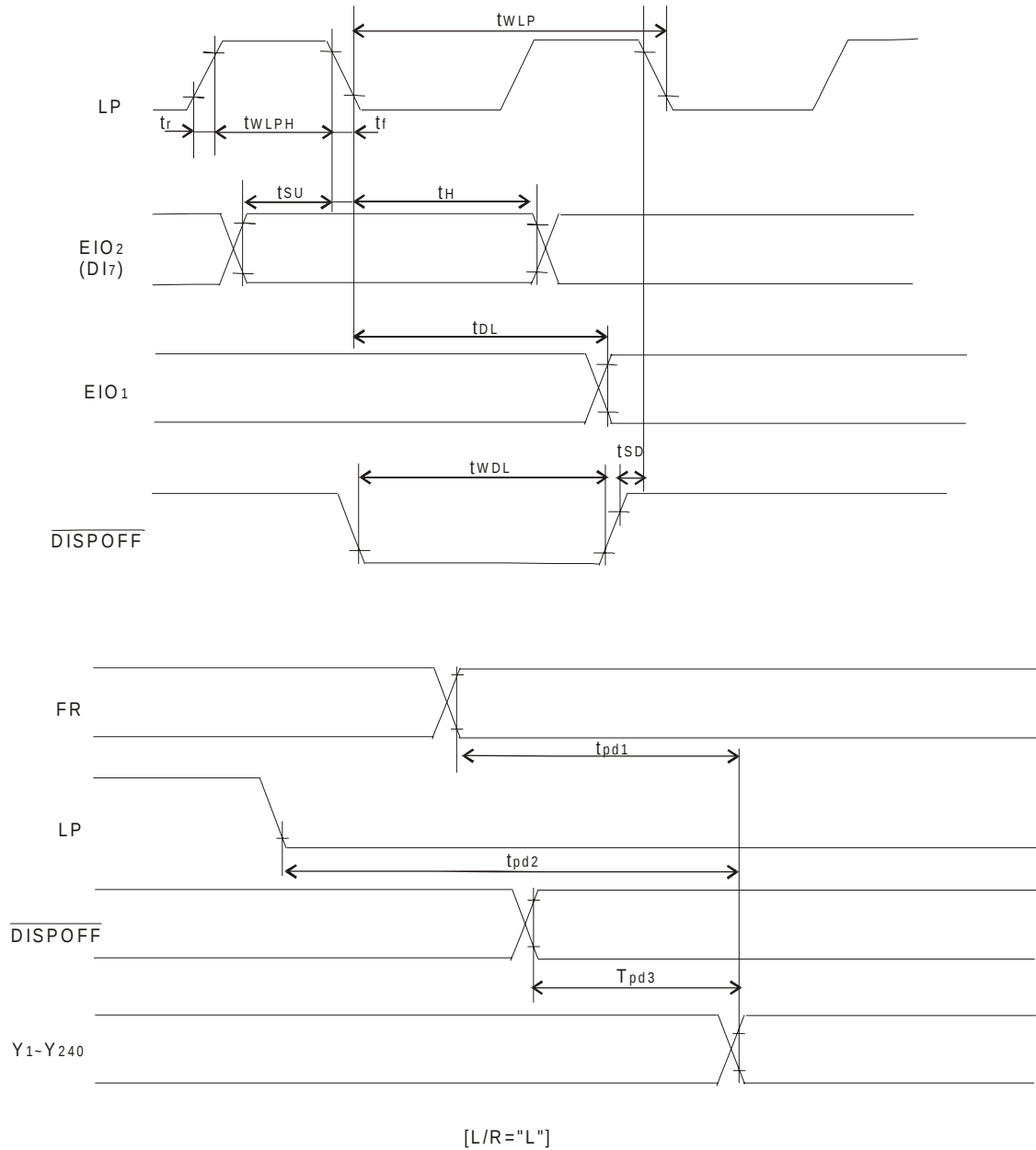


Fig.16

Example of system Configuration

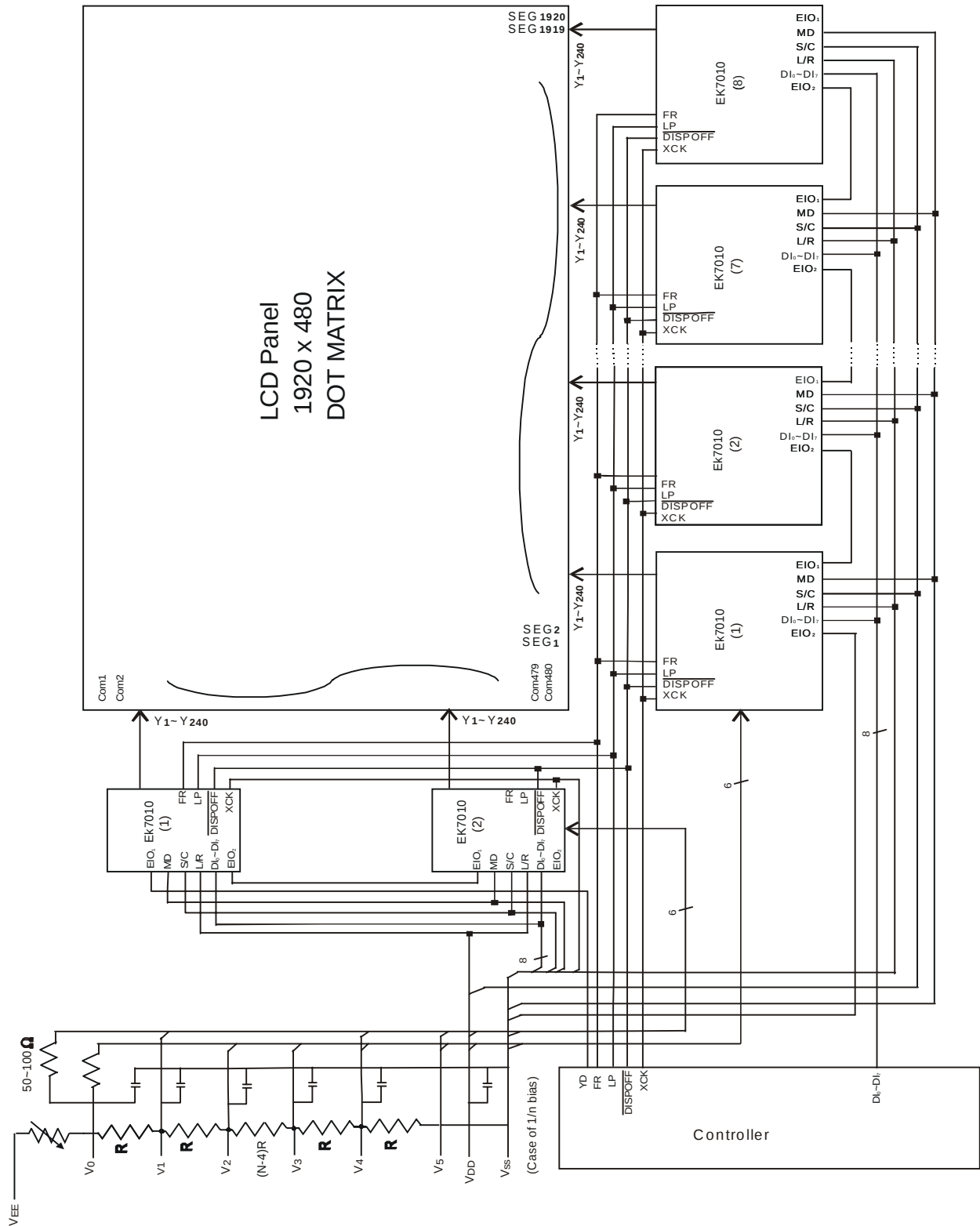


Fig.17

Example of Typical Characteristic

Parameter	Condition	Min.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time	Ta=+25°C , Vss=0V, V _{DD} =+5.0V		10		ns

Tab.18

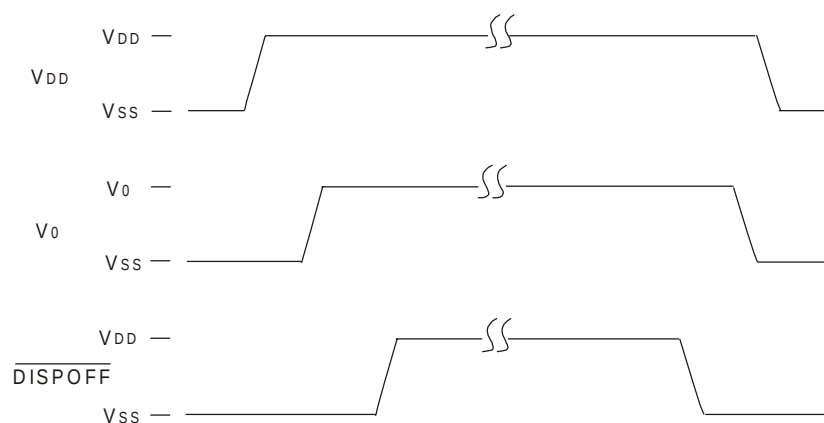
Precaution

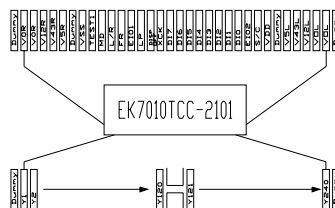
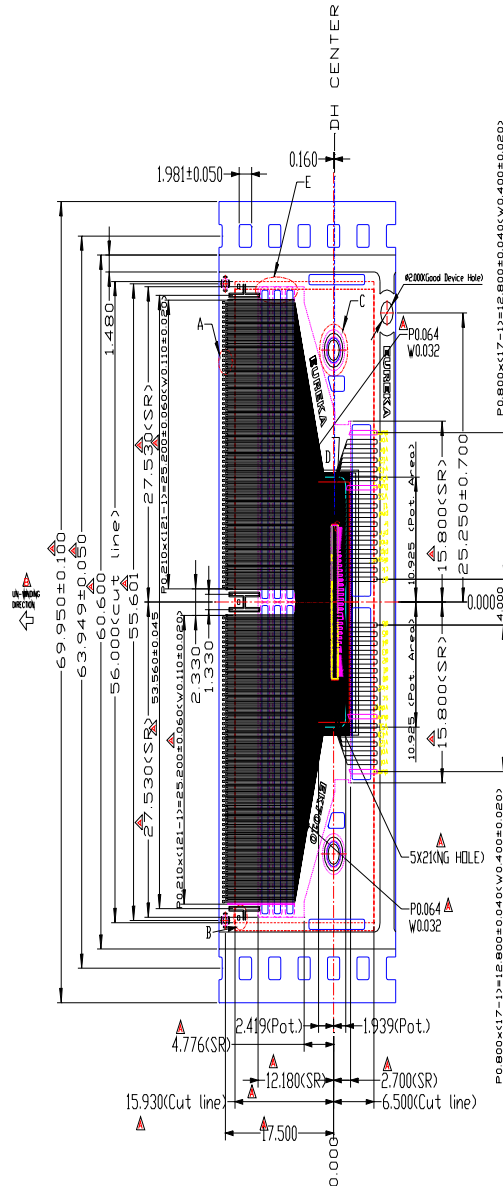
- Precaution when connecting or disconnecting the power

This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- We recommend you connecting the serial resistor(50~100Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. And set up the suitable value of the resistor in consideration of LCD display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LCD drive power supply after resetting logic condition of this LSI inside on $\overline{\text{DISPOFF}}$ function. After that, cancel the $\overline{\text{DISPOFF}}$ function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_s on $\overline{\text{DISPOFF}}$ function. After that, disconnect the logic system power after disconnecting the LCD drive power. When connecting the power supply, show the following recommend sequence.





NOTE:

1:GENERAL TOLERANCE :±0.050MM

2:ALL CHAMFER IS R0.20

3:MATERIAL

PI :UPILEXS 75±8um THICKNESS

ADHESIVE:TORAY #7100 12±4um THICKNESS

CU :SLP 25um

SOLDER RESIST:AE-70-M11 26±14um

OTHER TOLERANCE :±0.300

FLEX COATING:FS100L

4:PLATING

SN:0.21±0.05um

5:6 SPROCKET HOLES(28.5MM) FOR 1 TAPE SITE

