Eureka Microelectronics,Inc.

EK7010CG

240 Output Segment/ Common LCD Driver

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240 Output Segment/Common LCD Driver

Description

The EK7010 is a 240 output segment/common LCD driver adaptable to drive a large scale dot matrix panel. It uses the Tape Carrier Package(TCP) to greatly reduce the size of the LCD module. EK7010 consumes very little power. Large LCD panels can be assembled by cascading EK7010s. In Segment Mode, the input data can be either 4-bit parallel or 8-bit parallel, selected by the Mode Select pin (MD).

Features

- CMOS process
- Logic power supply : 2.5V to 5.5V
- Low power consumption
- 240 LCD display output
- Supply voltage for LCD driver :15 to 40V
- Package : TCP, COG available

Features in Segment mode

- Shift clock frequency : 20MHz max. at V_{DD}= 5V
- 4bit/8bit parallel input
- Automatic transfer of enable signal
- Automatic counting in the chip select mode. The internal clock is stoped by automatically counting 240 of input data.

Features in Common mode

- Shift clock frequency : 4MHz max. at V_{DD}=5V
- Built-in 240-bit bidirectional shift register
- Single mode (240-bit shift register) or Dual Mode (two 120-bit shift registers) with these options:
  1. Y1 ⟶ Y240 Single mode
  2. Y240 ⟶ Y1 Single mode
  3. Y1 ⟶ Y120, Y121 ⟶ Y240 Dual mode
  4. Y240 ⟶ Y121, Y120 ⟶ Y1 Dual mode

Block Diagram

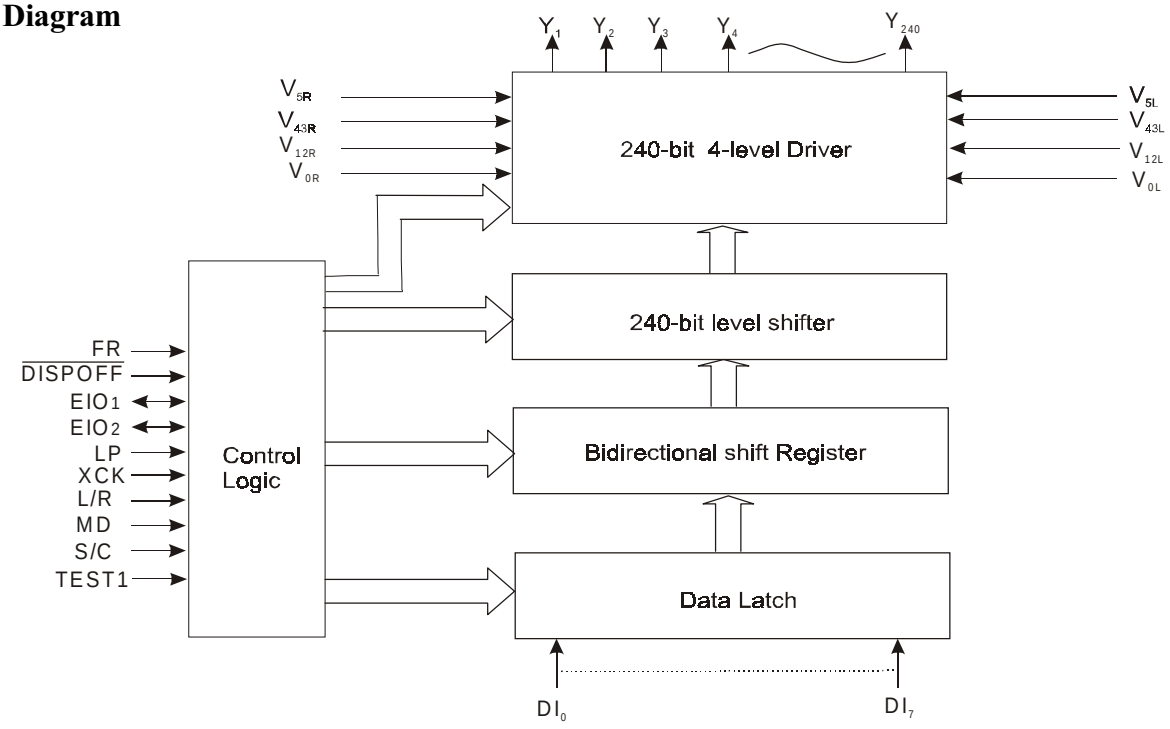


Fig.1

Input/Output Circuit

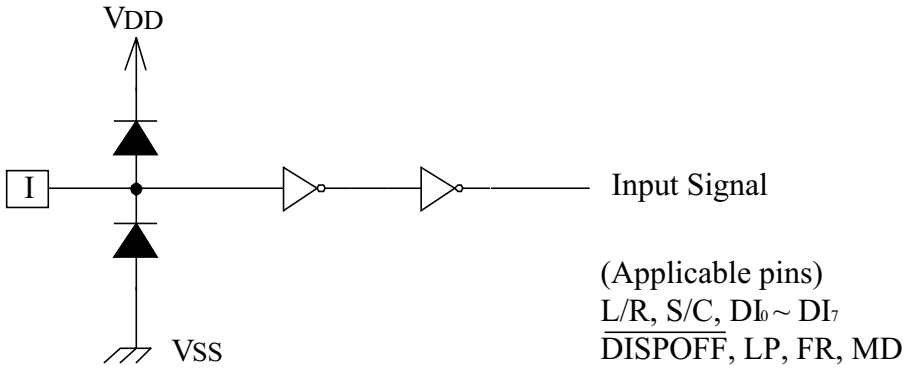


Fig.3 Input Circuit(1)

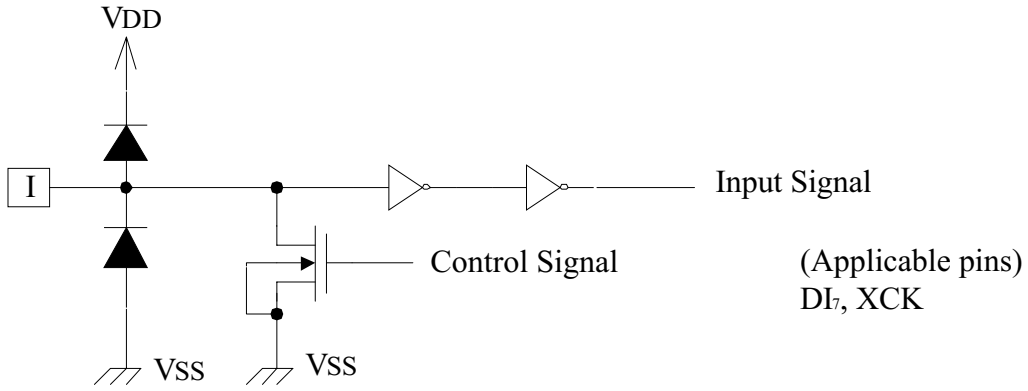


Fig.4 Input Circuit(2)

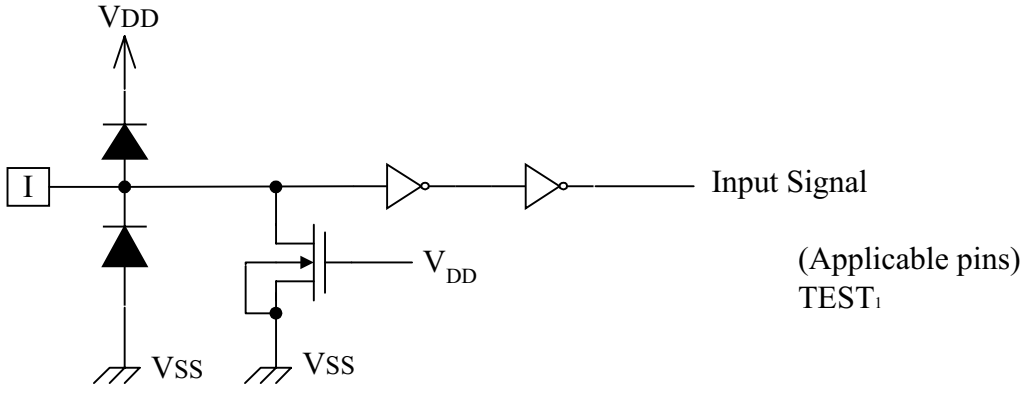


Fig.5 Input Circuit(3)

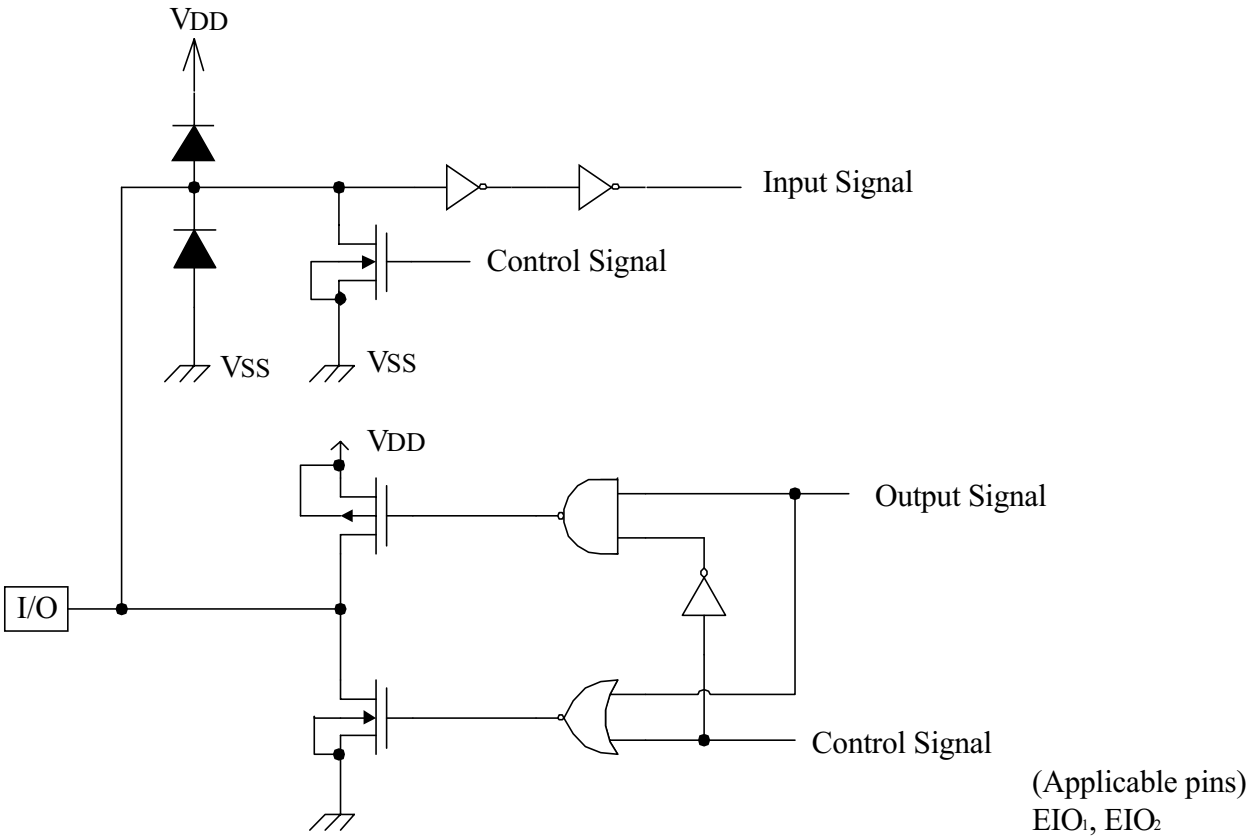


Fig.6 Input/Output Circuit

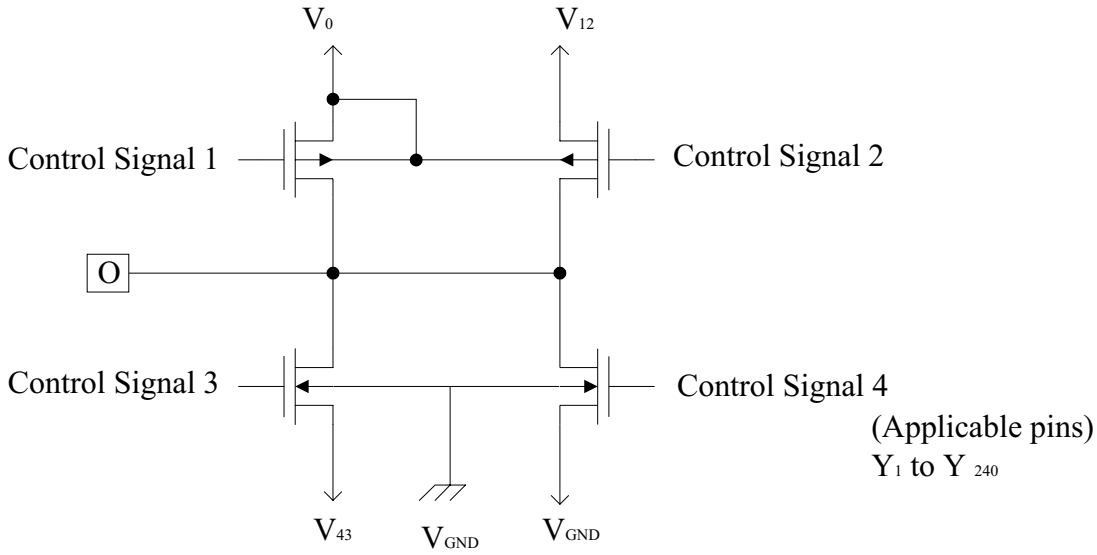


Fig.7 LCD Driver Output Circuit

Pin Functions
(Segment mode)

Symbol	Function
V_{DD}	Logic circuit power supply +2.5 to +5.5 V
V_{SS},V_{GND}	Logic circuit and high voltage ground pin
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L}	Power supply for LCD driver voltage level ● Normally, the bias voltage used is set by a resistor divider. ● Ensure that voltages are set such that $V_{SS} \leq V_{GND} < V_{43} < V_{12} < V_0$. ● V_{iR} and V_{iL} (i=0, 12, 43) should be externally connected to reduce the difference between the waveforms of the output pins $Y_1 \sim Y_{240}$.
DI_0~DI_7	Input for display data ● In 4-bit parallel input mode, input data into the 4 pins DI_0~DI_3 Connect DI_4-DI_7 to V_{SS} or V_{DD}. ● In 8-bit parallel input mode, input data into the 8 pins DI_0~DI_7.
XCK	Input clock pin for displaying data ● Data is read on the falling edge of the clock pulse.
LP	Latch pulse input for displaying data ● Data is latched on the falling edge of the clock pulse.
L/R	Direction selection for reading display data ● When set to V_{SS} , data is read sequentially from Y_{240} to Y_1. ● When set to V_{DD}, data is read sequentially from Y_1 to Y_{240}.
$\overline{DISPOFF}$	Control input to deselect output level ● The input signal is level-shifted from logic voltage level to LC drive voltage level and control LCD drive circuit. ● When set to Vss level "L", the LCD driver output pins (Y_1~Y_{240}) are setted to level V_{GND}. ● While set to "L", the contents of the line latch are cleared, but read the display data in the data latch regardless of condition of $\overline{DISPOFF}$. When the $\overline{DISPOFF}$ function is cancelled, the driver outputs deselect level (V_{12} or V_{43}), then outputs the contents of the data latch on the next falling edge of the LP. At that time, if $\overline{DISPOFF}$ removal time does not meet the conditions shown in Tab.15, it can not output the reading data correctly.
FR	AC signal for LCD driver output level ● The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. ● Normally, inputs a frame inversion signal. ● The LCD driver output voltage level of output pin can be setted using the line latch output signal and the FR signal. ● Truth table is shown on Tab.6 & Tab.7.

Tab.2

Pin Functions
(Segment mode)

Symbol	Function
MD	Mode selection ● When set to V_{DD} level "H", 4-bit parallel input mode is selected. ● When set to V_{SS} level "L", 8-bit parallel input mode is selected. ● The relationship between the display data and driver output pins is shown on Tab.8 & Tab.9.
S/C	Segment mode/common mode selection pin ● When set to V_{DD}, segment input mode is set.
EIO1 EIO2	Input/Output for chip selection ● When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. ● When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. ● During output, set to "H" while LP*$\overline{XCK}$ is "H"and after 240-bit data have been read, set to "L" for one cycle (from falling edge of XCK to next falling edge of XCK), after which it returns to "H". ● During input, after the LP signal is input, the chip is selected while EI is set to "L". After 240-bits of data have been read, the chip is deselected.
TEST1	Test mode selection ● During normal operation, tie to Vss level "L".
Y_1-Y_{240}	LCD driver output ● Corresponding directly to each bit of the data latch, one level(V0, V12, V43, or V_{GND}) is selected for output. ● Truth table values is shown on Tab.6 & Tab.7 .

Tab.3

Pin Functions
(Common mode)

Symbol	Function
V_{DD}	Logic circuit power supply pin connects to +2.5 to +5.5 V.
V_{SS}, V_{GND}	Logic circuit and high voltage ground pin
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L}	Power supply pin for LCD driver voltage bias ● Normally, the bias voltage is setted by a resistor divider ● Ensure that voltages are setted such that ($V_{SS} \leq V_{GND} < V_{43} < V_{12} < V_0$) ● V_{iR} and V_{iL}(i=0, 12, 43) should be externally connected to reduce the difference between the waveforms of the output pins $Y_1 \sim Y_{240}$.
EIO_1	Bidirectional shift register input/output ● Output when L/R is setted at Vss level "L", input when L/R is at V_{DD} level "H". ● When EIO_1 is used as input pin, it will be pull-down. ● When EIO_1 is used as output pin, it not be pull-down.
EIO_2	Bidirectional shift register input/output ● Input when L/R is setted at V_{SS} level "L". output when L/R is at V_{DD} level "H". ● When EIO_2 is used as input, it will be pull-down. ● When EIO_2 is used as output, it will not be pull-down.
LP	Bidirectional shift register clock pulse input ● Data is shifted on the falling edge of the clock pulse.
L/R	Bidirectional shift register shift direction selection ● When set to V_{SS}, data is shifted from Y_{240} to Y_1. ● When set to V_{DD}, data is shifted from Y_1 to Y_{240}.
$\overline{\text{DISPOFF}}$	Control input pin to deselect output level ● The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. ● When set to "L", the LCD driver output pins (Y_1-Y_{240}) are set to level V_{GND}. ● While set to "L", the contents of the shift resister are cleared. When the $\overline{\text{DISPOFF}}$ function is canceled, the driver outputs deselect level (V_{12} or V_{43}). and the shift data is read on the falling edge of the LP. At that time, if the $\overline{\text{DISPOFF}}$ removal time does not meet the conditions shown in Fig.16, then the shift data is not read correctly.
FR	AC signal input for LCD driver output level ● The input signal is level-shifted from logic voltage level to LCD driver voltage level, and controls LCD drive circuit. ● The LCD driver output voltage level can be set by using the shift register output signal and the FR signal. ● Truth table is shown on Tab.6 & Tab.7.

Tab.4

Pin Functions
(Common mode)

Symbol	Function
MD	Mode selection ● When set to Vss level "L", Single Mode operation is selected, when set to V_{DD} level "H", Dual Mode operation is selected.
DI_7	Dual Mode data input ● According to the data shift direction of the data shift register, data can be input starting from the 121th bit ● When the chip is used as Dual Mode, DI_7 will be pull-down. ● When the chip is used as Single Mode, DI_7 will not be pull-down.
S/C	Segment mode/common mode selection ● When set to V_{SS} level "L", Common Mode is setted.
DI_0~DI_6	Not used ● Connect DI_0~DI_6 to V_{SS} or V_{DD}. Avoiding floating.
XCK	Not used ● XCK is pull-down in common mode, so connect them to Vss or open.
$TEST_1$	Test mode select ● During normal operation, tie to V_{SS} level "L".
Y_1~Y_{240}	LCD driver output ● Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_{GND})is selected. ● Truth table is shown on Tab.6 & Tab.7.

Tab.5

Functional Operations

Truth Table

(Segment Mode)

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level(Y_1-Y_{240})
L	L	H	V43
L	H	H	V_{GND}
H	L	H	V12
H	H	H	V0
X	X	L	V_{GND}

Here, Vss ≤ V_{GND} < V43 < V12 < V0, H:VDD (+2.5 to +5.5V), L:Vss(0 V)
X:Don't care

Tab.6

(Common Mode)

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level(Y_1-Y_{240})
L	L	H	V43
L	H	H	V0
H	L	H	V12
H	H	H	V_{GND}
X	X	L	V_{GND}

Here, V_{SS} ≤ V_{GND} < V_{43}< V_{12} < V_0, H:V_{DD} (+2.5 to +5.5V), L:V_{SS}(0 V)
X:Don't care

Tab.7

Note:There have two kinds of power supply (logic level voltage, LCD drive voltage) for LCD driver.
Supply proper voltage according to each power pin specification.
"Don't care" means that it should be connected to "H" or "L". Do not leave them open.

Relationship between the Display Data and Driver Output pins
(Segment Mode)

(a)8-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Figure of Clock						
					30 clock	29 clock	28 clock	.....	3 clock	2 clock	1 clock
L	L	Output	Input	DI_0	Y_1	Y_9	Y17	.....	Y_{217}	Y_{225}	Y_{233}
				DI_1	Y_2	Y_{10}	Y_{18}	.....	Y_{218}	Y_{226}	Y_{234}
				DI_2	Y_3	Y_{11}	Y_{19}	.....	Y_{219}	Y_{227}	Y_{235}
				DI_3	Y_4	Y_{12}	Y20	.....	Y_{220}	Y_{228}	Y_{236}
				DI4	Y_5	Y13	Y21	.....	Y_{221}	Y_{229}	Y_{237}
				DI5	Y_6	Y_{14}	Y22	.....	Y_{222}	Y_{230}	Y_{238}
				DI6	Y_7	Y_{15}	Y23	.....	Y_{223}	Y_{231}	Y_{239}
				DI7	Y_8	Y_{16}	Y24	.....	Y_{224}	Y_{232}	Y_{240}
L	H	Input	Output	DI_0	Y_{240}	Y_{232}	Y_{224}	.....	Y24	Y_{16}	Y_8
				DI_1	Y_{239}	Y_{231}	Y_{223}	.....	Y23	Y_{15}	Y_7
				DI_2	Y_{238}	Y_{230}	Y_{222}	.....	Y22	Y_{14}	Y_6
				DI_3	Y_{237}	Y_{229}	Y_{221}	.....	Y21	Y_{13}	Y_5
				DI4	Y_{236}	Y_{228}	Y_{220}	.....	Y20	Y_{12}	Y_4
				DI5	Y_{235}	Y_{227}	Y_{219}	.....	Y_{19}	Y_{11}	Y_3
				DI6	Y_{234}	Y_{226}	Y_{218}	.....	Y_{18}	Y_{10}	Y_2
				DI7	Y_{233}	Y_{225}	Y_{217}	.....	Y_{17}	Y_9	Y_1

Tab.8

(b)4-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Figure of Clock						
					60 clock	59 clock	58 clock	.....	3 clock	2 clock	1 clock
H	L	Output	Input	DI_0	Y_1	Y_5	Y_9	.....	Y_{229}	Y_{233}	Y_{237}
				DI_1	Y_2	Y_6	Y_{10}	.....	Y_{230}	Y_{234}	Y_{238}
				DI_2	Y_3	Y_7	Y_{11}	.....	Y_{231}	Y_{235}	Y_{239}
				DI_3	Y_4	Y_8	Y_{12}	.....	Y_{232}	Y_{236}	Y_{240}
H	H	Input	Output	DI_0	Y_{240}	Y_{236}	Y_{232}	.....	Y_{12}	Y_8	Y_4
				DI_1	Y_{239}	Y_{235}	Y_{231}	.....	Y_{11}	Y_7	Y_3
				DI_2	Y_{238}	Y_{234}	Y_{230}	.....	Y_{10}	Y_6	Y_2
				DI_3	Y_{237}	Y_{233}	Y_{229}	.....	Y_9	Y_5	Y_1

Tab.9

(Common Mode)

MD	L/R	Data Transfer Direction	EIO1	EIO2	DI7
L (Single)	L(shift to left)	$Y_{240} \rightarrow Y_1$	Output	Input	X
	H(shift to right)	$Y_1 \rightarrow Y_{240}$	Input	Output	X
H (Dual)	L(shift to left)	$Y_{240} \rightarrow Y_{121}$ $Y_{120} \rightarrow Y_1$	Output	Input	Input
	H(shift to right)	$Y_1 \rightarrow Y_{120}$ $Y_{121} \rightarrow Y_{240}$	Input	Output	Input

Tab.10

L: V_{SS}(0 V), H: V_{DD} (+2.5V to +5.5V), X: Don't Care

Note: "Don't care" means that it should be connected to "H" or "L". Do not leave them open.

Connection Examples of Plural Segment Drives

(a) Case of L/R="L"

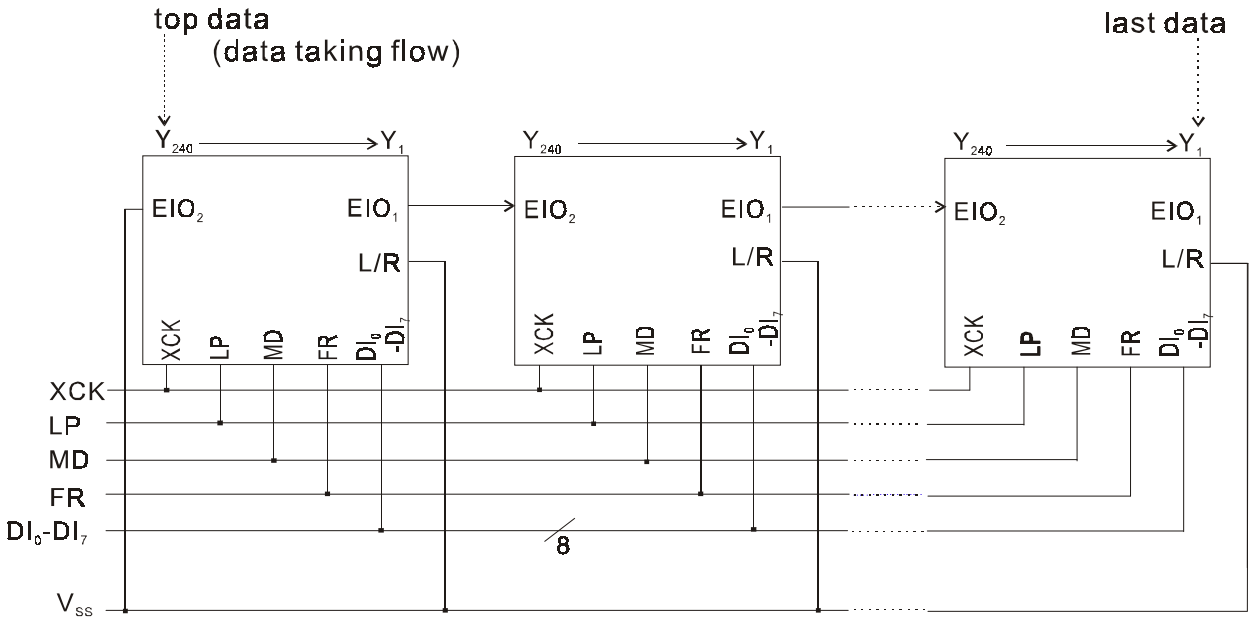


Fig.8

(b) Case of L/R="H"

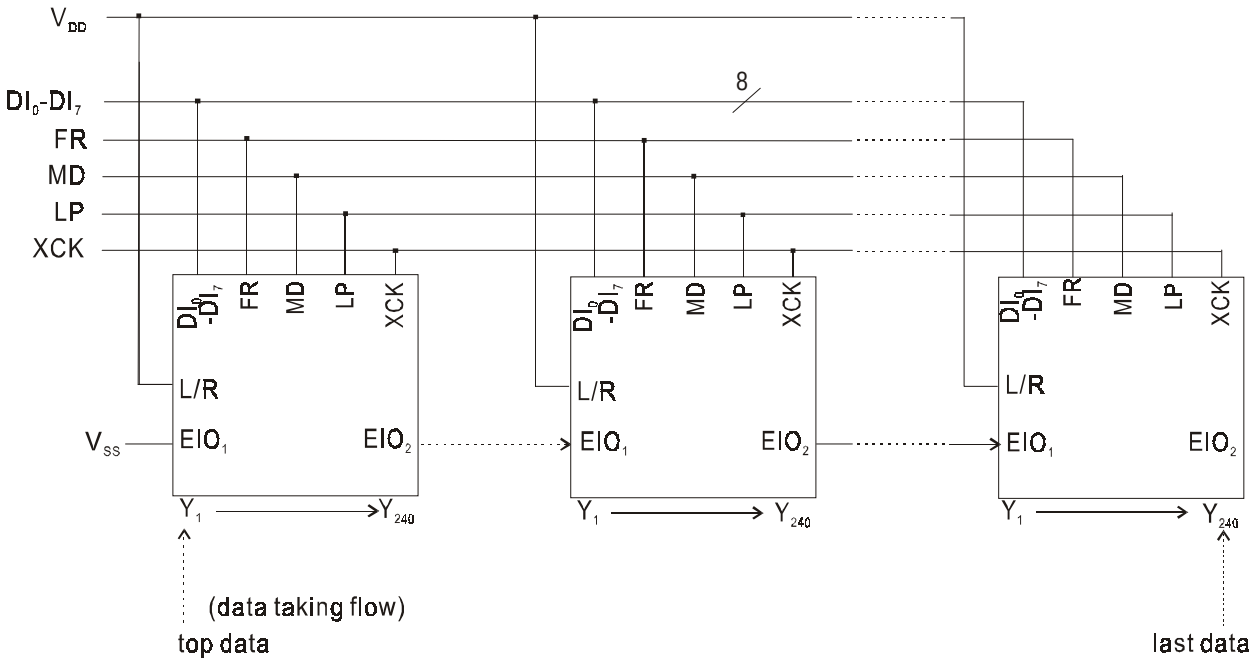


Fig.9

Timing Chart of 4-Device cascade Connection of Segment Drivers

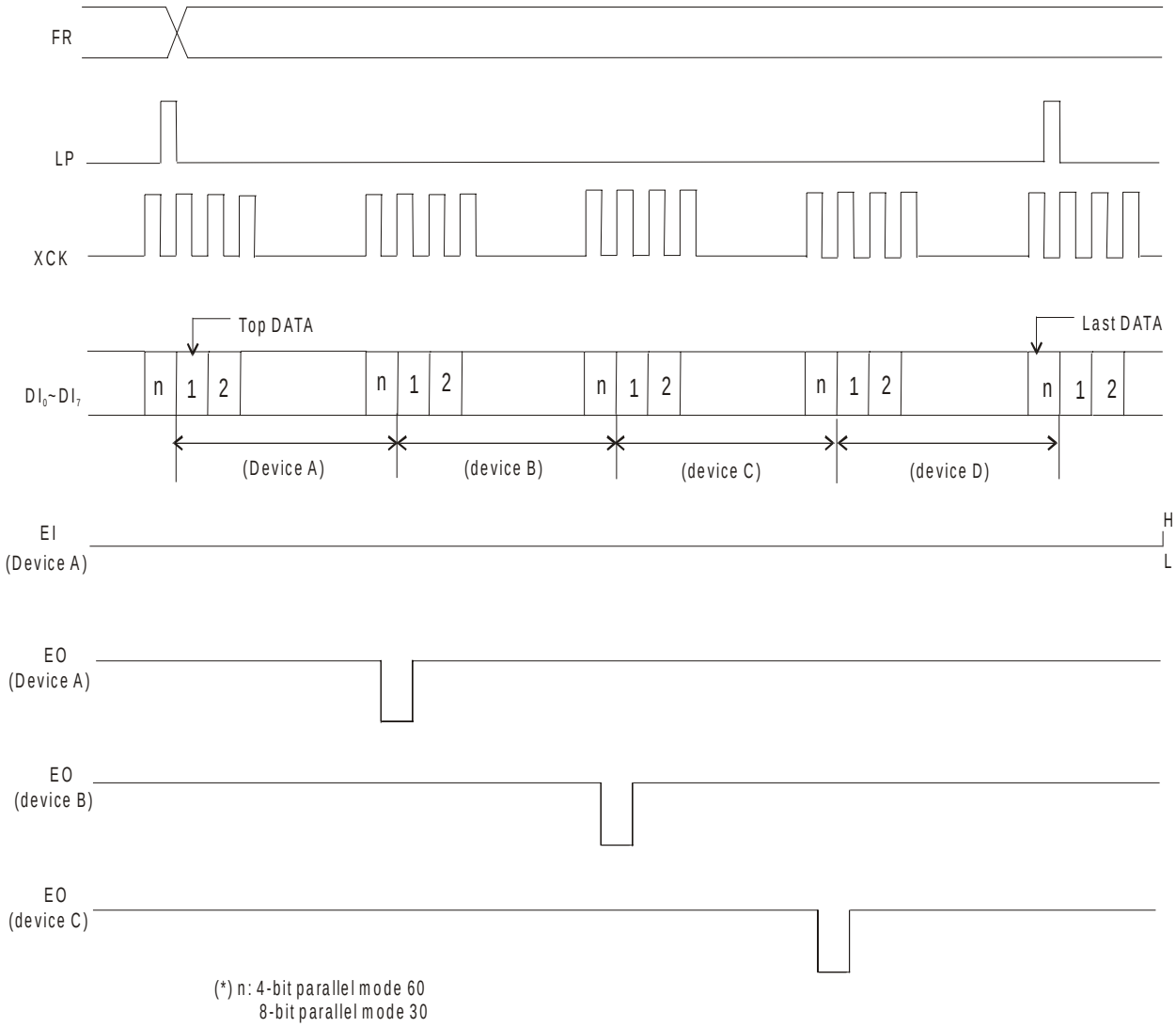


Fig.10

Connection Examples for Plural Common Drivers

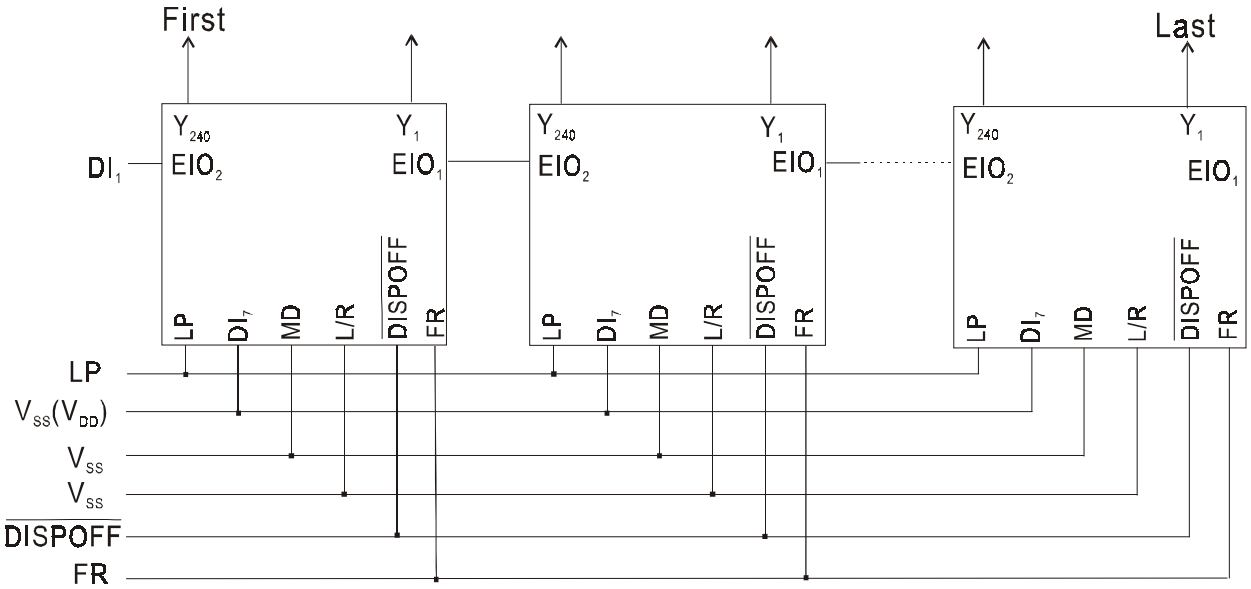


Fig.11 Single Mode (Shifting toward left)

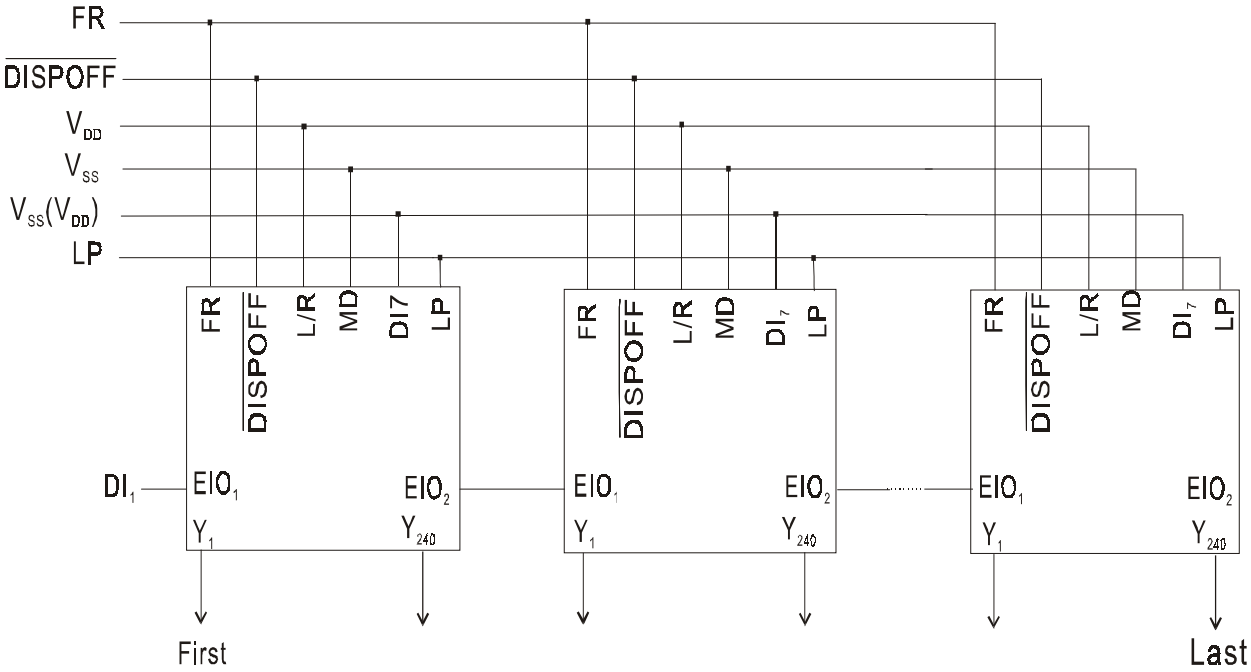


Fig.12 Single Mode (Shifting toward right)

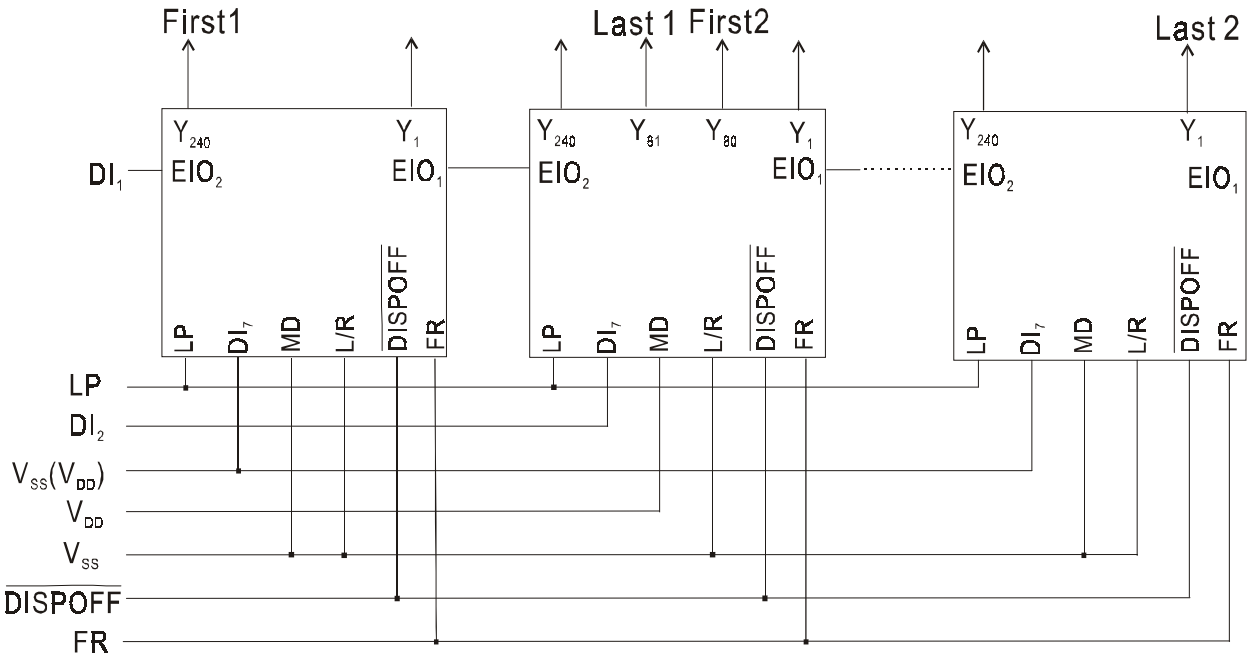


Fig.13 Dual Mode (Shifting toward left)

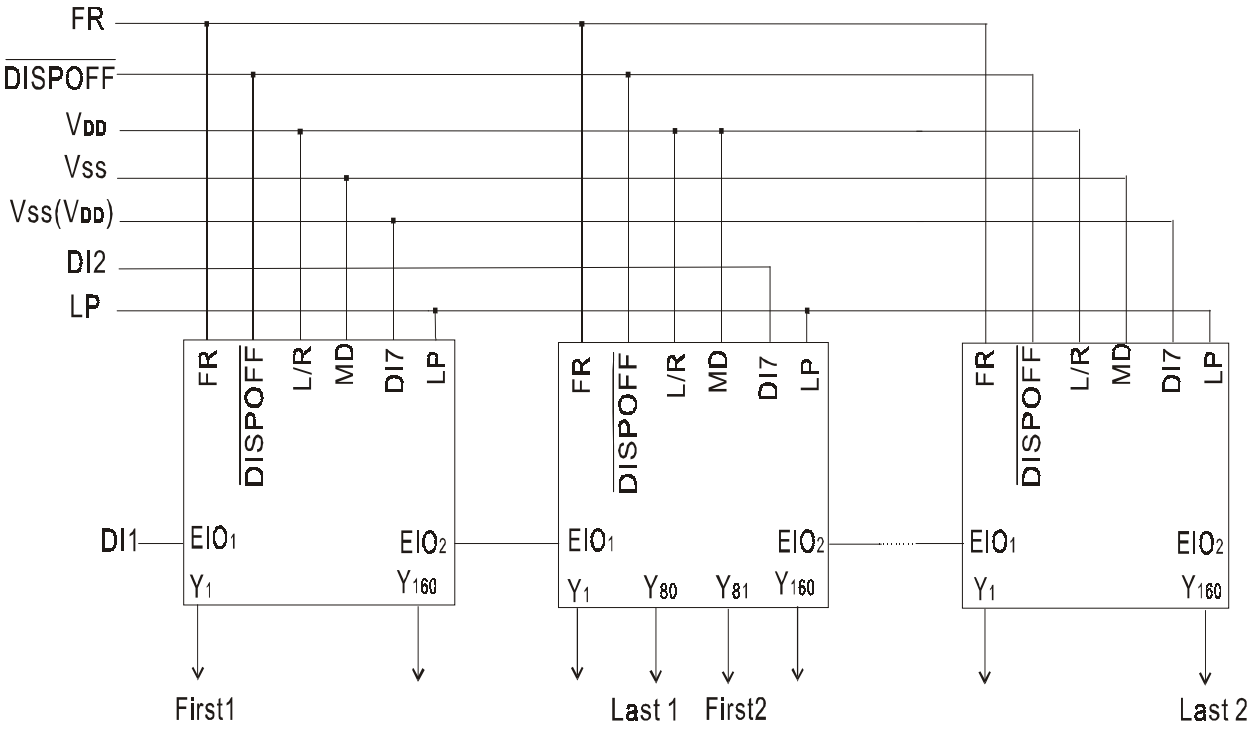


Fig.14 Dual Mode (Shifting toward right)

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable Pins	Ratings	Unit
Supply voltage(1)	V_{DD}	Ta=25°C Referenced to V_{SS}(0 V)	V_{DD}	-0.3 to +7.0	V
Supply voltage(2)	V_0		V_{0L},V_{0R}	-0.3 to +45.0	V
	V_{12}		V_{12L},V_{12R}	-0.3 to V_0+0.3	V
	V_{43}		V_{43L},V_{43R}	-0.3 to V_0+0.3	V
	V_{GND}		V_{GND}	-0.3 to V_0+0.3	V
Input voltage	V_I	Referenced to V_{SS}	DI_{0-7}, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	-0.3 to V_{DD}+0.3	V
Storage temperature	Tstg			-45 to +125	°C

Tab.11

Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage(1)	V_{DD}	Referenced to V_{SS} (0 V)	V_{DD}	+2.5		+5.5	V
Supply voltage(2)	V_0		V_{0L}, V_{0R}	+15.0		+40	V
Storage temperature	T_{opr}			-20		+85	°C

Tab.12

Note:Ensure that voltages are set such that $V_{SS} \leq V_{GND} < V_{43} < V_{12} < V_0$.

Electrical Characteristics

DC Characteristics
(Segment Mode)
(V_{SS}=V_{GND}=0 V, V_{DD}=+2.5V to +5.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Conditions		Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}			$DI_{0\sim7}$, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	$0.8V_{DD}$			V
	V_{IL}						$0.2V_{DD}$	V
Output voltage	V_{OH}	I_{OH}=-0.4mA		EIO_1,EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA					+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}		$DI_{0\sim7}$, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			+10.0	μA
	I_{LIL}	V_I=V_{SS}					-10.0	μA
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V	V_0=+40.0V	$Y_1\sim Y_{240}$		1.0	1.5	KΩ
			V_0=+30.0V			1.5	2.0	
			V_0=+20.0V			2.0	2.5	
Stand-by current	I_{STB}	*1		Vss			75.0	μA
Consumed current(1) (Deselection)	I_{DD1}	*2		V_{DD}			2.0	mA
Consumed current(2) (Selection)	I_{DD2}	*3		V_{DD}			12.0	mA
Consoumed current	I_0	*4		V_0			1.5	mA

Tab.13

Note:

*1 V_{DD}=+5.0V, V_0=+40V, V_I=V_{SS}.

*2 V_{DD}=+5.0V, V_0=+40V, f_{XCK}=20MHz, No-load, EI=V_{DD}.
The input data is turned over by data taking clock (4-bit parallel input mode)

*3 V_{DD}=+5.0V, V_0=+40V, f_{XCK}=20MHz, No-load, EI=V_{SS}.
The input data is turned over by data taking clock (4-bit parallel input mode).

*4 V_{DD}=+5.0V, V_0=+40V, f_{XCK}=20MHz, f_{LP}=41.6KHz, f_{FR}=80Hz, No-load.
The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode)

(V_{SS}=V_{GND}=0 V, V_{DD}=+2.5V to +5.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}		$DI_{0\sim7}$, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	0.8V_{DD}			V
	V_{IL}					0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4mA	EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA				+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}	$DI_{0\sim6}$, LP, L/R, FR, MD, S/C, $\overline{DISPOFF}$			+10.0	μA
	I_{LIL}	V_I=V_{SS}	$DI_{0\sim7}$, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			-10.0	μA
Input pull-down current	I_{PD}	V_I=V_{DD}	XCK,$EIO_1$$EIO_2$, DI_7			100.0	μA
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0=+40.0V	Y_1~Y_{240}		1.0	1.5	KΩ
		$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0=+30.0V			1.5	2.0	
		$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0=+20.0V			2.0	2.5	
Stand-by current	I_{STB}	*1	Vss			75.0	μA
Consumed current(1)	I_{DD}	*2	V_{DD}			120.0	μA
Consumed current(2)	I_O	*2	V_0			240.0	μA

Tab.14

*1 V_{DD}=+5.0V, V0=+40V, V_I=V_{SS}.

*2 V_{DD}=+5.0V, V0=+40V, f_{LP}=41.6KHz, f_{FR}=80Hz case of 1/480 duty operation, No-load.

AC Characteristics

(Segment Mode 1)

(V_{SS}=V_{GND}=0 V, V_{DD}=+4.5V to +5.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	t_r,t_f ≤ 10 ns	50			ns
Shift clock "H" pulse width	t_{WCKH}		15			ns
Shift clock "L" pulse width	t_{WCKL}		15			ns
Data setup time	t_{DS}		10			ns
Data Hold time	t_{DH}		12			ns
Latch pulse"H"pulse width	t_{WLPH}		15			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		30			ns
Latch pulse rise to Shift clock rise time	t_{LS}		25			ns
Latch pulse fall to Shift clock fall time	t_{LH}		25			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Enable setup time	t_s		10			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			μs
Output delay time(1)	t_D	C_L=15pF			30	ns
Output delay time(2)	t_{pd1},t_{pd2}	C_L=15pF			1.2	μs
Output delay time(3)	t_{pd3}	C_L=15pF			1.2	μs

Tab.15

Note:

*1 Take the cascade connection into consideration.

*2 (t_{CK}-t_{WCKH}-t_{WCKL}) /2 is maximum in the case of high speed operation.

(Segment Mode 2)

(V_{SS}=V_{GND}=0 V, V_{DD}=+2.5V to +4.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	t_r,t_f ≤ 11 ns	66			ns
Shift clock "H" pulse width	t_{WCKH}		23			ns
Shift clock "L" pulse width	t_{WCKL}		23			ns
Data setup time	t_{DS}		15			ns
Data Hold time	t_{DH}		23			ns
Latch pulse"H"pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		50			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift clock fall time	t_{LH}		30			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Enable setup time	t_s		15			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			µs
Output delay time(1)	t_D	C_L=15pF			41	ns
Output delay time(2)	t_{pd1},t_{pd2}	C_L=15pF			1.2	µs
Output delay time(3)	t_{pd3}	C_L=15pF			1.2	µs

Tab.16

Note:

*1 Take the cascade connection into consideration.

*2 (t_{CK}-t_{WCKH}-t_{WCKL}) /2 is maximum in the case of high speed operation.

(Segment Mode 3)

(V_{SS}=V_{GND}=0 V, V_{DD}=+2.5V to +3.0V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	t_r ,t_f ≤ 11 ns	82			ns
Shift clock "H" pulse width	t_{WCKH}		28			ns
Shift clock "L" pulse width	t_{WCKL}		28			ns
Data setup time	t_{DS}		20			ns
Data Hold time	t_{DH}		23			ns
Latch pulse "H" pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		65			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift clock fall time	t_{LH}		30			ns
Input signal rise time *2	t_r				50	ns
Input signal fall time *2	t_f				50	ns
Enable setup time	t_s		15			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			μs
Output delay time(1)	t_D	C_L=15pF			57	ns
Output delay time(2)	t_{pd1},t_{pd2}	C_L=15pF			1.2	μs
Output delay time(3)	t_{pd3}	C_L=15pF			1.2	μs

Tab.17

Note:

*1 Take the cascade connection into consideration.

*2 (t_{CK}-t_{WCKH}-t_{WCKL}) /2 is maximum in the case of high speed operation.

(Timing Characteristics of Segment Mode)

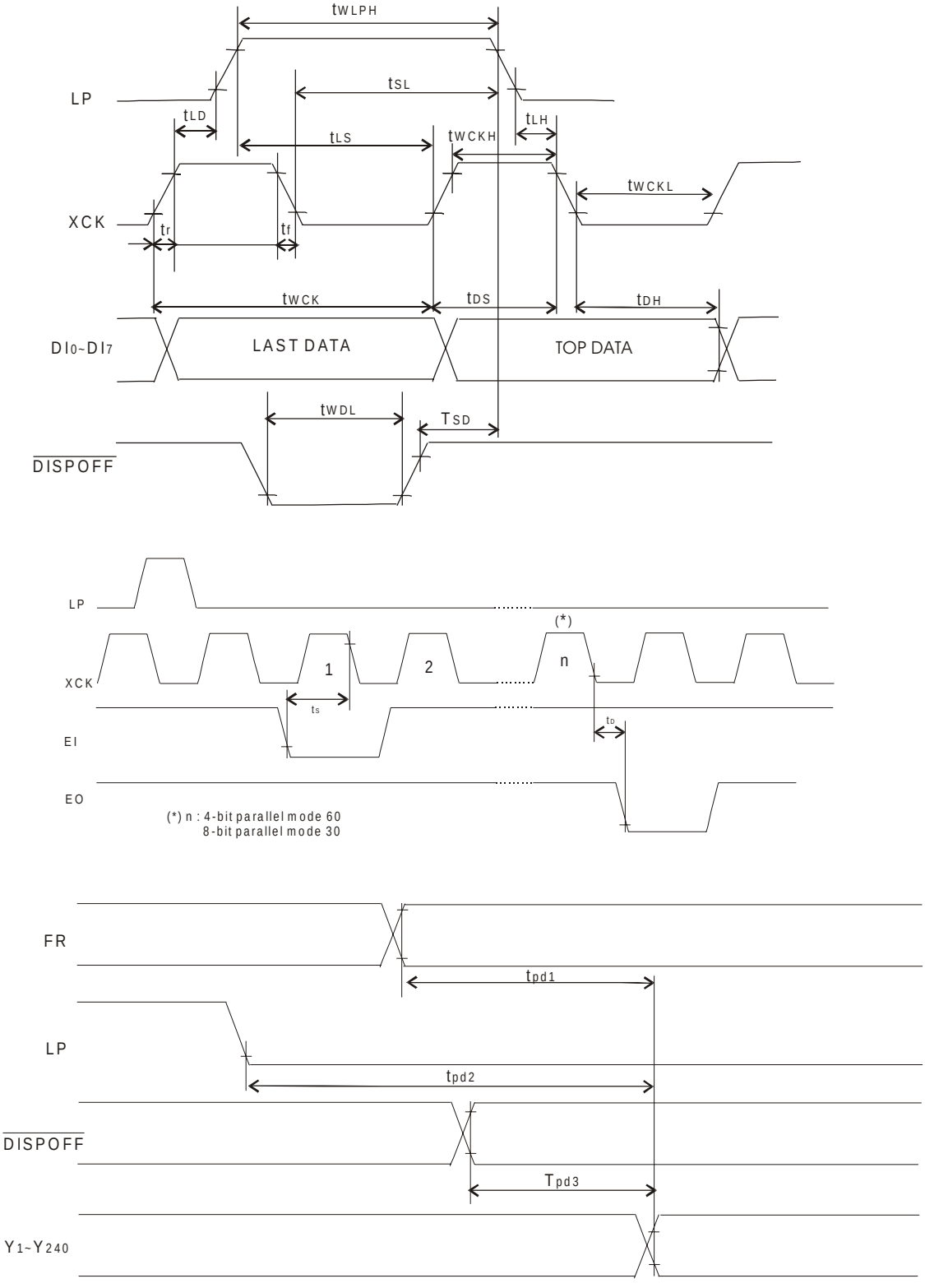


Fig.15

(Common Mode)

(V_{SS}=V_{GND}=0 V, V_{DD}=+2.5V to +5.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	t_{WLP}	t_r ,t_f ≤ 20 ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD}=+5.0V±10%	15			ns
		V_{DD}=+2.5V~ +4.5V	30			
Data setup time	t_{SU}		30			ns
Data Hold time	t_H		50			ns
Input signal rise time	t_r				50	ns
Input signal fall time	t_f				50	ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			µs
Output delay time(1)	t_{DL}	C_L=15pF			200	ns
Output delay time(2)	t_{pd1}, t_{pd2}	C_L=15pF			1.2	µs
Output delay time(3)	t_{pd3}	C_L=15pF			1.2	µs

Tab.17

(Timing Characteristics of Common Mode)

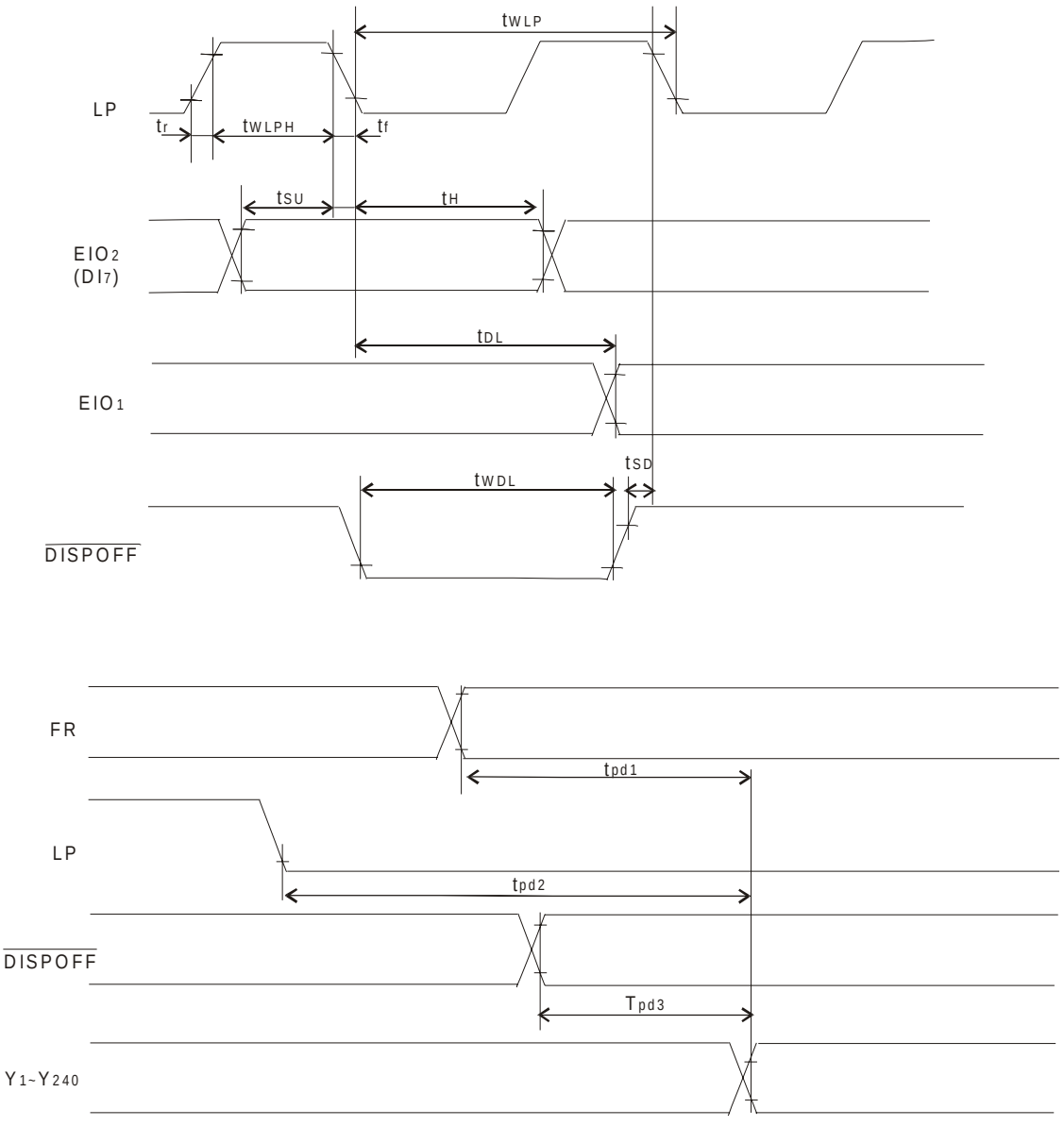


Fig.16

Example of system Configuration

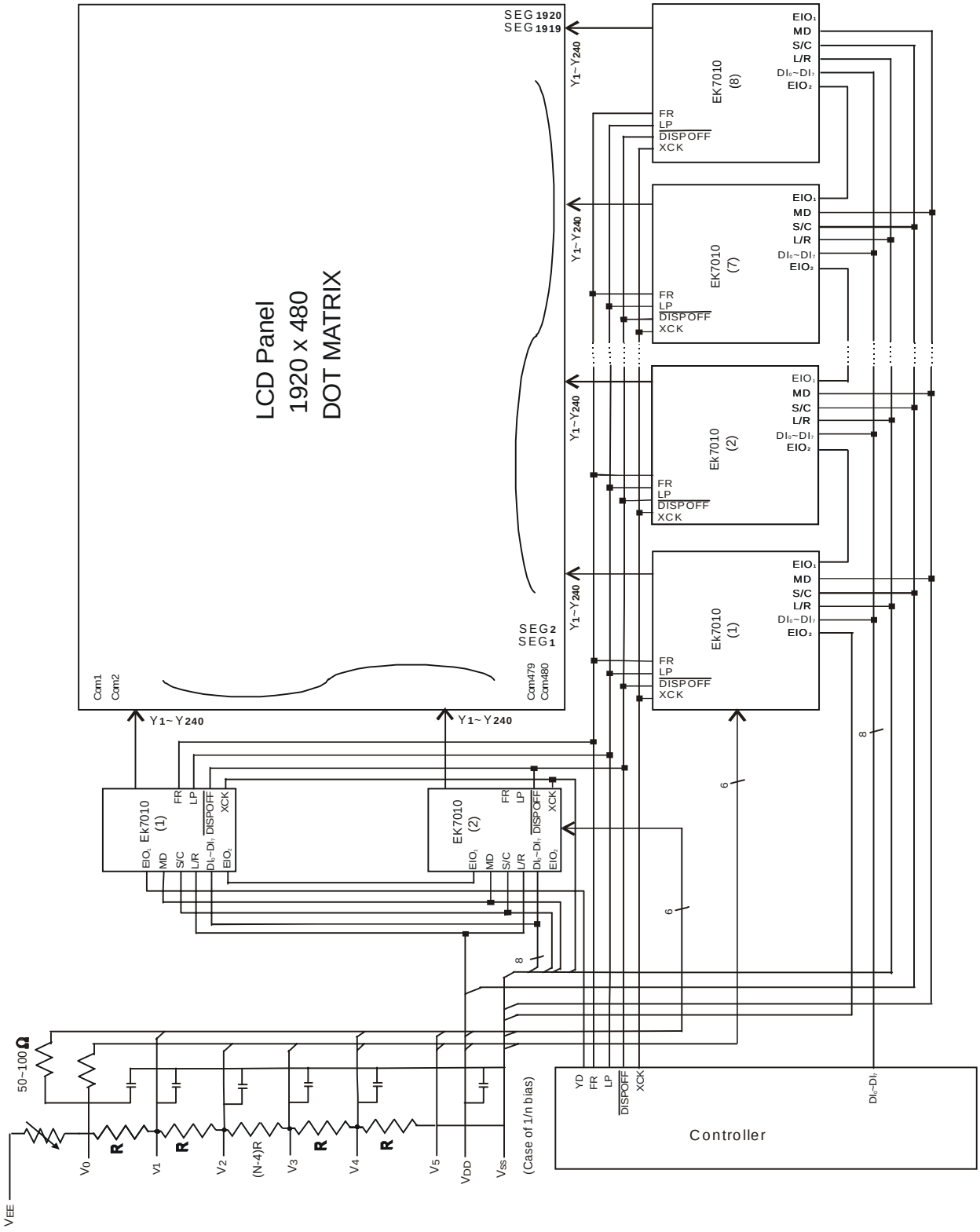


Fig.17

Example of Typical Characteristic

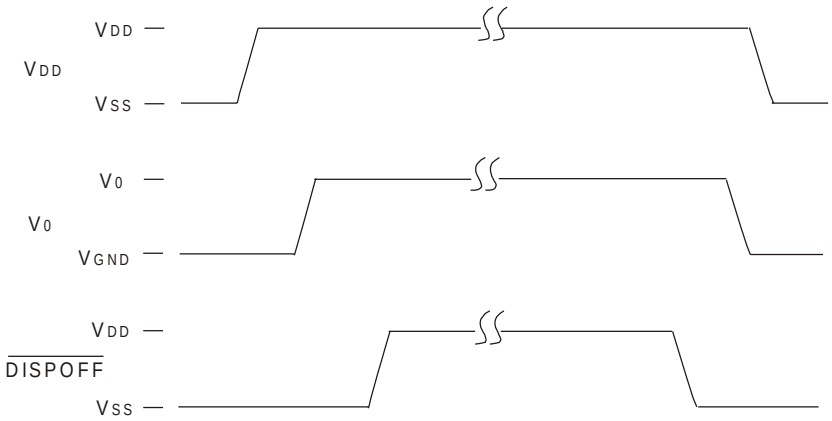
Parameter	Condition	Min.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time	Ta=+25^{0}C , Vss=0V, V_{DD}=+5.0V		10		ns

Tab.18

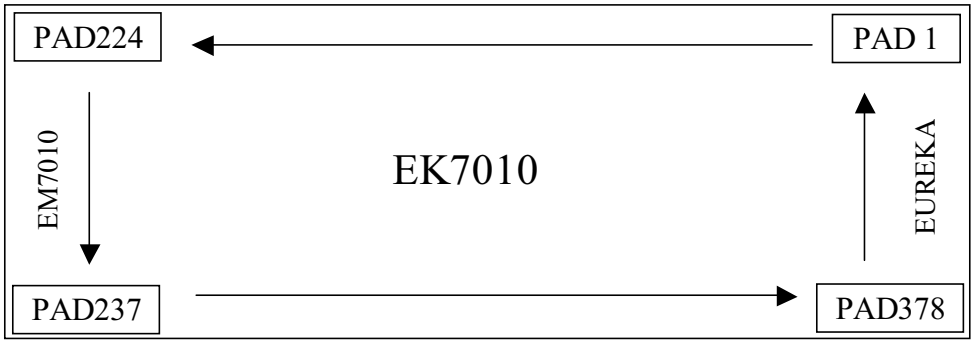
Precaution

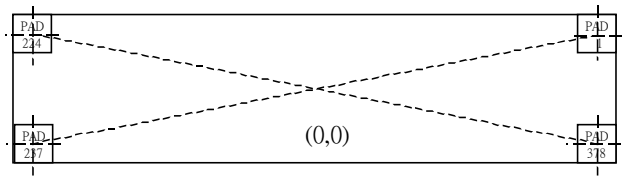
- Precaution when connecting or disconnecting the power
  This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating. The detail is as follows.
- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- We recommend you connecting the serial resistor(50~100Ω) or fuse to the LCD drive power V_0 of the system as a current limitter. And set up the suitable value of the resistor in consideration of LCD display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LCD drive power supply after resetting logic condition of this LSI inside on $\overline{\text{DISPOFF}}$ function. After that. cancel the $\overline{\text{DISPOFF}}$ function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_{GND} on $\overline{\text{DISPOFF}}$ function. After that, disconnect the logic system power after disconnecting the LCD drive power. When connecting the power supply, show the following recommend sequence.



Chip Size:13623.6um x 1173 um





Wafer thickness : 19mil
Height of Bump : within lot 18m ± 3μm
within wafer < 4μm
within die < 2μm

All pads named Dummy are floating inside the chip and may be used to aid routing on the glass.

In COG applications, the high voltage ground pad V_{GND} should have a separate path to the connector, and not be connected to V_{SS} on the glass. This is to prevent any ground bounce generated by high voltage switching to disturb the logic circuits.

Ensure that logic V_{SS} and high voltage V_{GND} are at the same potential.

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD1	72.8X72.8	Y009	6705	480	*85.2 X 85.2*
PAD2	42.8X72.8	Y010	6630	480	55.2 X 85.2
PAD3	42.8X72.8	Y011	6570	480	55.2 X 85.2
PAD4	42.8X72.8	Y012	6510	480	55.2 X 85.2
PAD5	42.8X72.8	Y013	6450	480	55.2 X 85.2
PAD6	42.8X72.8	Y014	6390	480	55.2 X 85.2
PAD7	42.8X72.8	Y015	6330	480	55.2 X 85.2
PAD8	42.8X72.8	Y016	6270	480	55.2 X 85.2
PAD9	42.8X72.8	Y017	6210	480	55.2 X 85.2
PAD10	42.8X72.8	Y018	6150	480	55.2 X 85.2
PAD11	42.8X72.8	Y019	6090	480	55.2 X 85.2
PAD12	42.8X72.8	Y020	6030	480	55.2 X 85.2
PAD13	42.8X72.8	Y021	5970	480	55.2 X 85.2
PAD14	42.8X72.8	Y022	5910	480	55.2 X 85.2
PAD15	42.8X72.8	Y023	5850	480	55.2 X 85.2
PAD16	42.8X72.8	Y024	5790	480	55.2 X 85.2
PAD17	42.8X72.8	Y025	5730	480	55.2 X 85.2
PAD18	42.8X72.8	Y026	5670	480	55.2 X 85.2
PAD19	42.8X72.8	Y027	5610	480	55.2 X 85.2
PAD20	42.8X72.8	Y028	5550	480	55.2 X 85.2
PAD21	42.8X72.8	Y029	5490	480	55.2 X 85.2
PAD22	42.8X72.8	Y030	5430	480	55.2 X 85.2
PAD23	42.8X72.8	Y031	5370	480	55.2 X 85.2
PAD24	42.8X72.8	Y032	5310	480	55.2 X 85.2
PAD25	42.8X72.8	Y033	5250	480	55.2 X 85.2
PAD26	42.8X72.8	Y034	5190	480	55.2 X 85.2
PAD27	42.8X72.8	Y035	5130	480	55.2 X 85.2
PAD28	42.8X72.8	Y036	5070	480	55.2 X 85.2
PAD29	42.8X72.8	Y037	5010	480	55.2 X 85.2
PAD30	42.8X72.8	Y038	4950	480	55.2 X 85.2
PAD31	42.8X72.8	Y039	4890	480	55.2 X 85.2
PAD32	42.8X72.8	Y040	4830	480	55.2 X 85.2
PAD33	42.8X72.8	Y041	4770	480	55.2 X 85.2
PAD34	42.8X72.8	Y042	4710	480	55.2 X 85.2
PAD35	42.8X72.8	Y043	4650	480	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD36	42.8X72.8	Y044	4590	480	55.2 X 85.2
PAD37	42.8X72.8	Y045	4530	480	55.2 X 85.2
PAD38	42.8X72.8	Y046	4470	480	55.2 X 85.2
PAD39	42.8X72.8	Y047	4410	480	55.2 X 85.2
PAD40	42.8X72.8	Y048	4350	480	55.2 X 85.2
PAD41	42.8X72.8	Y049	4290	480	55.2 X 85.2
PAD42	42.8X72.8	Y050	4230	480	55.2 X 85.2
PAD43	42.8X72.8	Y051	4170	480	55.2 X 85.2
PAD44	42.8X72.8	Y052	4110	480	55.2 X 85.2
PAD45	42.8X72.8	Y053	4050	480	55.2 X 85.2
PAD46	42.8X72.8	Y054	3990	480	55.2 X 85.2
PAD47	42.8X72.8	Y055	3930	480	55.2 X 85.2
PAD48	42.8X72.8	Y056	3870	480	55.2 X 85.2
PAD49	42.8X72.8	Y057	3810	480	55.2 X 85.2
PAD50	42.8X72.8	Y058	3750	480	55.2 X 85.2
PAD51	42.8X72.8	Y059	3690	480	55.2 X 85.2
PAD52	42.8X72.8	Y060	3630	480	55.2 X 85.2
PAD53	42.8X72.8	Y061	3570	480	55.2 X 85.2
PAD54	42.8X72.8	Y062	3510	480	55.2 X 85.2
PAD55	42.8X72.8	Y063	3450	480	55.2 X 85.2
PAD56	42.8X72.8	Y064	3390	480	55.2 X 85.2
PAD57	42.8X72.8	Y065	3330	480	55.2 X 85.2
PAD58	42.8X72.8	Y066	3270	480	55.2 X 85.2
PAD59	42.8X72.8	Y067	3210	480	55.2 X 85.2
PAD60	42.8X72.8	Y068	3150	480	55.2 X 85.2
PAD61	42.8X72.8	Y069	3090	480	55.2 X 85.2
PAD62	42.8X72.8	Y070	3030	480	55.2 X 85.2
PAD63	42.8X72.8	Y071	2970	480	55.2 X 85.2
PAD64	42.8X72.8	Y072	2910	480	55.2 X 85.2
PAD65	42.8X72.8	Y073	2850	480	55.2 X 85.2
PAD66	42.8X72.8	Y074	2790	480	55.2 X 85.2
PAD67	42.8X72.8	Y075	2730	480	55.2 X 85.2
PAD68	42.8X72.8	Y076	2670	480	55.2 X 85.2
PAD69	42.8X72.8	Y077	2610	480	55.2 X 85.2
PAD70	42.8X72.8	Y078	2550	480	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD71	42.8X72.8	Y079	2490	480	55.2 X 85.2
PAD72	42.8X72.8	Y080	2430	480	55.2 X 85.2
PAD73	42.8X72.8	Y081	2370	480	55.2 X 85.2
PAD74	42.8X72.8	Y082	2310	480	55.2 X 85.2
PAD75	42.8X72.8	Y083	2250	480	55.2 X 85.2
PAD76	42.8X72.8	Y084	2190	480	55.2 X 85.2
PAD77	42.8X72.8	Y085	2130	480	55.2 X 85.2
PAD78	42.8X72.8	Y086	2070	480	55.2 X 85.2
PAD79	42.8X72.8	Y087	2010	480	55.2 X 85.2
PAD80	42.8X72.8	Y088	1950	480	55.2 X 85.2
PAD81	42.8X72.8	Y089	1890	480	55.2 X 85.2
PAD82	42.8X72.8	Y090	1830	480	55.2 X 85.2
PAD83	42.8X72.8	Y091	1770	480	55.2 X 85.2
PAD84	42.8X72.8	Y092	1710	480	55.2 X 85.2
PAD85	42.8X72.8	Y093	1650	480	55.2 X 85.2
PAD86	42.8X72.8	Y094	1590	480	55.2 X 85.2
PAD87	42.8X72.8	Y095	1530	480	55.2 X 85.2
PAD88	42.8X72.8	Y096	1470	480	55.2 X 85.2
PAD89	42.8X72.8	Y097	1410	480	55.2 X 85.2
PAD90	42.8X72.8	Y098	1350	480	55.2 X 85.2
PAD91	42.8X72.8	Y099	1290	480	55.2 X 85.2
PAD92	42.8X72.8	Y100	1230	480	55.2 X 85.2
PAD93	42.8X72.8	Y101	1170	480	55.2 X 85.2
PAD94	42.8X72.8	Y102	1110	480	55.2 X 85.2
PAD95	42.8X72.8	Y103	1050	480	55.2 X 85.2
PAD96	42.8X72.8	Y104	990	480	55.2 X 85.2
PAD97	42.8X72.8	Y105	930	480	55.2 X 85.2
PAD98	42.8X72.8	Y106	870	480	55.2 X 85.2
PAD99	42.8X72.8	Y107	810	480	55.2 X 85.2
PAD100	42.8X72.8	Y108	750	480	55.2 X 85.2
PAD101	42.8X72.8	Y109	690	480	55.2 X 85.2
PAD102	42.8X72.8	Y110	630	480	55.2 X 85.2
PAD103	42.8X72.8	Y111	570	480	55.2 X 85.2
PAD104	42.8X72.8	Y112	510	480	55.2 X 85.2
PAD105	42.8X72.8	Y113	450	480	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD106	42.8X72.8	Y114	390	480	55.2 X 85.2
PAD107	42.8X72.8	Y115	330	480	55.2 X 85.2
PAD108	42.8X72.8	Y116	270	480	55.2 X 85.2
PAD109	42.8X72.8	Y117	210	480	55.2 X 85.2
PAD110	42.8X72.8	Y118	150	480	55.2 X 85.2
PAD111	42.8X72.8	Y119	90	480	55.2 X 85.2
PAD112	42.8X72.8	Y120	30	480	55.2 X 85.2
PAD113	42.8X72.8	Y121	-30	480	55.2 X 85.2
PAD114	42.8X72.8	Y122	-90	480	55.2 X 85.2
PAD115	42.8X72.8	Y123	-150	480	55.2 X 85.2
PAD116	42.8X72.8	Y124	-210	480	55.2 X 85.2
PAD117	42.8X72.8	Y125	-270	480	55.2 X 85.2
PAD118	42.8X72.8	Y126	-330	480	55.2 X 85.2
PAD119	42.8X72.8	Y127	-390	480	55.2 X 85.2
PAD120	42.8X72.8	Y128	-450	480	55.2 X 85.2
PAD121	42.8X72.8	Y129	-510	480	55.2 X 85.2
PAD122	42.8X72.8	Y130	-570	480	55.2 X 85.2
PAD123	42.8X72.8	Y131	-630	480	55.2 X 85.2
PAD124	42.8X72.8	Y132	-690	480	55.2 X 85.2
PAD125	42.8X72.8	Y133	-750	480	55.2 X 85.2
PAD126	42.8X72.8	Y134	-810	480	55.2 X 85.2
PAD127	42.8X72.8	Y135	-870	480	55.2 X 85.2
PAD128	42.8X72.8	Y136	-930	480	55.2 X 85.2
PAD129	42.8X72.8	Y137	-990	480	55.2 X 85.2
PAD130	42.8X72.8	Y138	-1050	480	55.2 X 85.2
PAD131	42.8X72.8	Y139	-1110	480	55.2 X 85.2
PAD132	42.8X72.8	Y140	-1170	480	55.2 X 85.2
PAD133	42.8X72.8	Y141	-1230	480	55.2 X 85.2
PAD134	42.8X72.8	Y142	-1290	480	55.2 X 85.2
PAD135	42.8X72.8	Y143	-1350	480	55.2 X 85.2
PAD136	42.8X72.8	Y144	-1410	480	55.2 X 85.2
PAD137	42.8X72.8	Y145	-1470	480	55.2 X 85.2
PAD138	42.8X72.8	Y146	-1530	480	55.2 X 85.2
PAD139	42.8X72.8	Y147	-1590	480	55.2 X 85.2
PAD140	42.8X72.8	Y148	-1650	480	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD141	42.8X72.8	Y149	-1710	480	55.2 X 85.2
PAD142	42.8X72.8	Y150	-1770	480	55.2 X 85.2
PAD143	42.8X72.8	Y151	-1830	480	55.2 X 85.2
PAD144	42.8X72.8	Y152	-1890	480	55.2 X 85.2
PAD145	42.8X72.8	Y153	-1950	480	55.2 X 85.2
PAD146	42.8X72.8	Y154	-2010	480	55.2 X 85.2
PAD147	42.8X72.8	Y155	-2070	480	55.2 X 85.2
PAD148	42.8X72.8	Y156	-2130	480	55.2 X 85.2
PAD149	42.8X72.8	Y157	-2190	480	55.2 X 85.2
PAD150	42.8X72.8	Y158	-2250	480	55.2 X 85.2
PAD151	42.8X72.8	Y159	-2310	480	55.2 X 85.2
PAD152	42.8X72.8	Y160	-2370	480	55.2 X 85.2
PAD153	42.8X72.8	Y161	-2430	480	55.2 X 85.2
PAD154	42.8X72.8	Y162	-2490	480	55.2 X 85.2
PAD155	42.8X72.8	Y163	-2550	480	55.2 X 85.2
PAD156	42.8X72.8	Y164	-2610	480	55.2 X 85.2
PAD157	42.8X72.8	Y165	-2670	480	55.2 X 85.2
PAD158	42.8X72.8	Y166	-2730	480	55.2 X 85.2
PAD159	42.8X72.8	Y167	-2790	480	55.2 X 85.2
PAD160	42.8X72.8	Y168	-2850	480	55.2 X 85.2
PAD161	42.8X72.8	Y169	-2910	480	55.2 X 85.2
PAD162	42.8X72.8	Y170	-2970	480	55.2 X 85.2
PAD163	42.8X72.8	Y171	-3030	480	55.2 X 85.2
PAD164	42.8X72.8	Y172	-3090	480	55.2 X 85.2
PAD165	42.8X72.8	Y173	-3150	480	55.2 X 85.2
PAD166	42.8X72.8	Y174	-3210	480	55.2 X 85.2
PAD167	42.8X72.8	Y175	-3270	480	55.2 X 85.2
PAD168	42.8X72.8	Y176	-3330	480	55.2 X 85.2
PAD169	42.8X72.8	Y177	-3390	480	55.2 X 85.2
PAD170	42.8X72.8	Y178	-3450	480	55.2 X 85.2
PAD171	42.8X72.8	Y179	-3510	480	55.2 X 85.2
PAD172	42.8X72.8	Y180	-3570	480	55.2 X 85.2
PAD173	42.8X72.8	Y181	-3630	480	55.2 X 85.2
PAD174	42.8X72.8	Y182	-3690	480	55.2 X 85.2
PAD175	42.8X72.8	Y183	-3750	480	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD176	42.8X72.8	Y184	-3810	480	55.2 X 85.2
PAD177	42.8X72.8	Y185	-3870	480	55.2 X 85.2
PAD178	42.8X72.8	Y186	-3930	480	55.2 X 85.2
PAD179	42.8X72.8	Y187	-3990	480	55.2 X 85.2
PAD180	42.8X72.8	Y188	-4050	480	55.2 X 85.2
PAD181	42.8X72.8	Y189	-4110	480	55.2 X 85.2
PAD182	42.8X72.8	Y190	-4170	480	55.2 X 85.2
PAD183	42.8X72.8	Y191	-4230	480	55.2 X 85.2
PAD184	42.8X72.8	Y192	-4290	480	55.2 X 85.2
PAD185	42.8X72.8	Y193	-4350	480	55.2 X 85.2
PAD186	42.8X72.8	Y194	-4410	480	55.2 X 85.2
PAD187	42.8X72.8	Y195	-4470	480	55.2 X 85.2
PAD188	42.8X72.8	Y196	-4530	480	55.2 X 85.2
PAD189	42.8X72.8	Y197	-4590	480	55.2 X 85.2
PAD190	42.8X72.8	Y198	-4650	480	55.2 X 85.2
PAD191	42.8X72.8	Y199	-4710	480	55.2 X 85.2
PAD192	42.8X72.8	Y200	-4770	480	55.2 X 85.2
PAD193	42.8X72.8	Y201	-4830	480	55.2 X 85.2
PAD194	42.8X72.8	Y202	-4890	480	55.2 X 85.2
PAD195	42.8X72.8	Y203	-4950	480	55.2 X 85.2
PAD196	42.8X72.8	Y204	-5010	480	55.2 X 85.2
PAD197	42.8X72.8	Y205	-5070	480	55.2 X 85.2
PAD198	42.8X72.8	Y206	-5130	480	55.2 X 85.2
PAD199	42.8X72.8	Y207	-5190	480	55.2 X 85.2
PAD200	42.8X72.8	Y208	-5250	480	55.2 X 85.2
PAD201	42.8X72.8	Y209	-5310	480	55.2 X 85.2
PAD202	42.8X72.8	Y210	-5370	480	55.2 X 85.2
PAD203	42.8X72.8	Y211	-5430	480	55.2 X 85.2
PAD204	42.8X72.8	Y212	-5490	480	55.2 X 85.2
PAD205	42.8X72.8	Y213	-5550	480	55.2 X 85.2
PAD206	42.8X72.8	Y214	-5610	480	55.2 X 85.2
PAD207	42.8X72.8	Y215	-5670	480	55.2 X 85.2
PAD208	42.8X72.8	Y216	-5730	480	55.2 X 85.2
PAD209	42.8X72.8	Y217	-5790	480	55.2 X 85.2
PAD210	42.8X72.8	Y218	-5850	480	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD211	42.8X72.8	Y219	-5910	480	55.2 X 85.2
PAD212	42.8X72.8	Y220	-5970	480	55.2 X 85.2
PAD213	42.8X72.8	Y221	-6030	480	55.2 X 85.2
PAD214	42.8X72.8	Y222	-6090	480	55.2 X 85.2
PAD215	42.8X72.8	Y223	-6150	480	55.2 X 85.2
PAD216	42.8X72.8	Y224	-6210	480	55.2 X 85.2
PAD217	42.8X72.8	Y225	-6270	480	55.2 X 85.2
PAD218	42.8X72.8	Y226	-6330	480	55.2 X 85.2
PAD219	42.8X72.8	Y227	-6390	480	55.2 X 85.2
PAD220	42.8X72.8	Y228	-6450	480	55.2 X 85.2
PAD221	42.8X72.8	Y229	-6510	480	55.2 X 85.2
PAD222	42.8X72.8	Y230	-6570	480	55.2 X 85.2
PAD223	42.8X72.8	Y231	-6630	480	55.2 X 85.2
PAD224	72.8X72.8	Y232	-6705	480	*85.2 X 85.2*
PAD225	42.8X72.8	Y233	-6705	330	55.2 X 85.2
PAD226	42.8X72.8	Y234	-6705	270	55.2 X 85.2
PAD227	42.8X72.8	Y235	-6705	210	55.2 X 85.2
PAD228	42.8X72.8	Y236	-6705	150	55.2 X 85.2
PAD229	42.8X72.8	Y237	-6705	90	55.2 X 85.2
PAD230	42.8X72.8	Y238	-6705	30	55.2 X 85.2
PAD231	42.8X72.8	Y239	-6705	-30	55.2 X 85.2
PAD232	42.8X72.8	Y240	-6705	-90	55.2 X 85.2
PAD233	42.8X72.8	V0	-6705	-150	55.2 X 85.2
PAD234	42.8X72.8	V12	-6705	-210	55.2 X 85.2
PAD235	42.8X72.8	V43	-6705	-270	55.2 X 85.2
PAD236	42.8X72.8	V_{GND}	-6705	-330	55.2 X 85.2
PAD237	72.8X72.8	V_{GND}	-6705	-480	*85.2 X 85.2*
PAD238	42.8X72.8	V_{GND}	-6630	-480	55.2 X 85.2
PAD239	42.8X72.8	V_{SS}	-6570	-480	55.2 X 85.2
PAD240	42.8X72.8	Dummy	-6510	-480	55.2 X 85.2
PAD241	42.8X72.8	Dummy	-6450	-480	55.2 X 85.2
PAD242	42.8X72.8	Dummy	-6390	-480	55.2 X 85.2
PAD243	42.8X72.8	Dummy	-6330	-480	55.2 X 85.2
PAD244	42.8X72.8	Dummy	-6270	-480	55.2 X 85.2
PAD245	42.8X72.8	Dummy	-6210	-480	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD246	42.8X72.8	Dummy	-6150	-480	55.2 X 85.2
PAD247	42.8X72.8	Dummy	-6090	-480	55.2 X 85.2
PAD248	42.8X72.8	Dummy	-6030	-480	55.2 X 85.2
PAD249	42.8X72.8	Dummy	-5970	-480	55.2 X 85.2
PAD250	42.8X72.8	Dummy	-5910	-480	55.2 X 85.2
PAD251	42.8X72.8	Dummy	-5850	-480	55.2 X 85.2
PAD252	42.8X72.8	Dummy	-5790	-480	55.2 X 85.2
PAD253	42.8X72.8	Dummy	-5730	-480	55.2 X 85.2
PAD254	42.8X72.8	Dummy	-5670	-480	55.2 X 85.2
PAD255	42.8X72.8	Dummy	-5610	-480	55.2 X 85.2
PAD256	42.8X72.8	Dummy	-5550	-480	55.2 X 85.2
PAD257	42.8X72.8	Dummy	-5490	-480	55.2 X 85.2
PAD258	42.8X72.8	Dummy	-5430	-480	55.2 X 85.2
PAD259	42.8X72.8	Dummy	-5370	-480	55.2 X 85.2
PAD260	42.8X72.8	Dummy	-5310	-480	55.2 X 85.2
PAD261	42.8X72.8	Dummy	-5250	-480	55.2 X 85.2
PAD262	42.8X72.8	Dummy	-5190	-480	55.2 X 85.2
PAD263	42.8X72.8	Dummy	-5130	-480	55.2 X 85.2
PAD264	42.8X72.8	Dummy	-5070	-480	55.2 X 85.2
PAD265	42.8X72.8	Dummy	-5010	-480	55.2 X 85.2
PAD266	42.8X72.8	Dummy	-4950	-480	55.2 X 85.2
PAD267	42.8X72.8	Dummy	-4890	-480	55.2 X 85.2
PAD268	42.8X72.8	Dummy	-4830	-480	55.2 X 85.2
PAD269	42.8X72.8	Dummy	-4770	-480	55.2 X 85.2
PAD270	42.8X72.8	Dummy	-4710	-480	55.2 X 85.2
PAD271	42.8X72.8	Dummy	-4650	-480	55.2 X 85.2
PAD272	42.8X72.8	V_{SS}	-4590	-480	55.2 X 85.2
PAD273	42.8X72.8	V_{SS}	-4530	-480	55.2 X 85.2
PAD274	42.8X72.8	V_{SS}	-4470	-480	55.2 X 85.2
PAD275	42.8X72.8	Dummy	-4410	-480	55.2 X 85.2
PAD276	42.8X72.8	Dummy	-4350	-480	55.2 X 85.2
PAD277	42.8X72.8	Dummy	-4230	-480	55.2 X 85.2
PAD278	42.8X72.8	Dummy	-4110	-480	55.2 X 85.2
PAD279	42.8X72.8	Dummy	-4050	-480	55.2 X 85.2
PAD280	42.8X72.8	Dummy	-3870	-480	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD281	42.8X72.8	vdd:P	-3810	-480	55.2 X 85.2
PAD282	42.8X72.8	vdd:P	-3750	-480	55.2 X 85.2
PAD283	42.8X72.8	vdd:P	-3690	-480	55.2 X 85.2
PAD284	42.8X72.8	Dummy	-3630	-480	55.2 X 85.2
PAD285	42.8X72.8	Dummy	-3450	-480	55.2 X 85.2
PAD286	42.8X72.8	SC	-3330	-480	55.2 X 85.2
PAD287	42.8X72.8	Dummy	-3210	-480	55.2 X 85.2
PAD288	42.8X72.8	Dummy	-3030	-480	55.2 X 85.2
PAD289	42.8X72.8	EIO_2	-2910	-480	55.2 X 85.2
PAD290	42.8X72.8	Dummy	-2790	-480	55.2 X 85.2
PAD291	42.8X72.8	Dummy	-2610	-480	55.2 X 85.2
PAD292	42.8X72.8	D0	-2490	-480	55.2 X 85.2
PAD293	42.8X72.8	Dummy	-2370	-480	55.2 X 85.2
PAD294	42.8X72.8	Dummy	-2190	-480	55.2 X 85.2
PAD295	42.8X72.8	D1	-2070	-480	55.2 X 85.2
PAD296	42.8X72.8	Dummy	-1950	-480	55.2 X 85.2
PAD297	42.8X72.8	Dummy	-1770	-480	55.2 X 85.2
PAD298	42.8X72.8	D2	-1650	-480	55.2 X 85.2
PAD299	42.8X72.8	Dummy	-1530	-480	55.2 X 85.2
PAD300	42.8X72.8	Dummy	-1230	-480	55.2 X 85.2
PAD301	42.8X72.8	Dummy	-930	-480	55.2 X 85.2
PAD302	42.8X72.8	D3	-810	-480	55.2 X 85.2
PAD303	42.8X72.8	Dummy	-690	-480	55.2 X 85.2
PAD304	42.8X72.8	Dummy	-510	-480	55.2 X 85.2
PAD305	42.8X72.8	D4	-390	-480	55.2 X 85.2
PAD306	42.8X72.8	Dummy	-270	-480	55.2 X 85.2
PAD307	42.8X72.8	Dummy	-90	-480	55.2 X 85.2
PAD308	42.8X72.8	D5	30	-480	55.2 X 85.2
PAD309	42.8X72.8	Dummy	150	-480	55.2 X 85.2
PAD310	42.8X72.8	Dummy	330	-480	55.2 X 85.2
PAD311	42.8X72.8	D6	450	-480	55.2 X 85.2
PAD312	42.8X72.8	Dummy	570	-480	55.2 X 85.2
PAD313	42.8X72.8	Dummy	750	-480	55.2 X 85.2
PAD314	42.8X72.8	D7	870	-480	55.2 X 85.2
PAD315	42.8X72.8	Dummy	990	-480	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD316	42.8X72.8	Dummy	1170	-480	55.2 X 85.2
PAD317	42.8X72.8	CK	1290	-480	55.2 X 85.2
PAD318	42.8X72.8	Dummy	1410	-480	55.2 X 85.2
PAD319	42.8X72.8	Dummy	1590	-480	55.2 X 85.2
PAD320	42.8X72.8	DISPOFF	1710	-480	55.2 X 85.2
PAD321	42.8X72.8	Dummy	1830	-480	55.2 X 85.2
PAD322	42.8X72.8	Dummy	2010	-480	55.2 X 85.2
PAD323	42.8X72.8	PLP	2130	-480	55.2 X 85.2
PAD324	42.8X72.8	Dummy	2250	-480	55.2 X 85.2
PAD325	42.8X72.8	Dummy	2430	-480	55.2 X 85.2
PAD326	42.8X72.8	EIO_1	2550	-480	55.2 X 85.2
PAD327	42.8X72.8	Dummy	2670	-480	55.2 X 85.2
PAD328	42.8X72.8	Dummy	2850	-480	55.2 X 85.2
PAD329	42.8X72.8	PFR	2970	-480	55.2 X 85.2
PAD330	42.8X72.8	Dummy	3090	-480	55.2 X 85.2
PAD331	42.8X72.8	Dummy	3270	-480	55.2 X 85.2
PAD332	42.8X72.8	LR	3390	-480	55.2 X 85.2
PAD333	42.8X72.8	Dummy	3510	-480	55.2 X 85.2
PAD334	42.8X72.8	Dummy	3690	-480	55.2 X 85.2
PAD335	42.8X72.8	PMD	3810	-480	55.2 X 85.2
PAD336	42.8X72.8	Dummy	3930	-480	55.2 X 85.2
PAD337	42.8X72.8	Dummy	4110	-480	55.2 X 85.2
PAD338	42.8X72.8	T1	4230	-480	55.2 X 85.2
PAD339	42.8X72.8	Dummy	4350	-480	55.2 X 85.2
PAD340	42.8X72.8	Dummy	4410	-480	55.2 X 85.2
PAD341	42.8X72.8	V_{SS}	4470	-480	55.2 X 85.2
PAD342	42.8X72.8	V_{SS}	4530	-480	55.2 X 85.2
PAD343	42.8X72.8	V_{SS}	4590	-480	55.2 X 85.2
PAD344	42.8X72.8	Dummy	4650	-480	55.2 X 85.2
PAD345	42.8X72.8	Dummy	4710	-480	55.2 X 85.2
PAD346	42.8X72.8	Dummy	4770	-480	55.2 X 85.2
PAD347	42.8X72.8	Dummy	4830	-480	55.2 X 85.2
PAD348	42.8X72.8	Dummy	4890	-480	55.2 X 85.2
PAD349	42.8X72.8	Dummy	4950	-480	55.2 X 85.2
PAD350	42.8X72.8	Dummy	5010	-480	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD351	42.8X72.8	Dummy	5070	-480	55.2 X 85.2
PAD352	42.8X72.8	Dummy	5130	-480	55.2 X 85.2
PAD353	42.8X72.8	Dummy	5190	-480	55.2 X 85.2
PAD354	42.8X72.8	Dummy	5250	-480	55.2 X 85.2
PAD355	42.8X72.8	Dummy	5310	-480	55.2 X 85.2
PAD356	42.8X72.8	Dummy	5370	-480	55.2 X 85.2
PAD357	42.8X72.8	Dummy	5430	-480	55.2 X 85.2
PAD358	42.8X72.8	Dummy	5490	-480	55.2 X 85.2
PAD359	42.8X72.8	Dummy	5550	-480	55.2 X 85.2
PAD360	42.8X72.8	Dummy	5610	-480	55.2 X 85.2
PAD361	42.8X72.8	Dummy	5670	-480	55.2 X 85.2
PAD362	42.8X72.8	Dummy	5730	-480	55.2 X 85.2
PAD363	42.8X72.8	Dummy	5790	-480	55.2 X 85.2
PAD364	42.8X72.8	Dummy	5850	-480	55.2 X 85.2
PAD365	42.8X72.8	Dummy	5910	-480	55.2 X 85.2
PAD366	42.8X72.8	Dummy	5970	-480	55.2 X 85.2
PAD367	42.8X72.8	Dummy	6030	-480	55.2 X 85.2
PAD368	42.8X72.8	Dummy	6090	-480	55.2 X 85.2
PAD369	42.8X72.8	Dummy	6150	-480	55.2 X 85.2
PAD370	42.8X72.8	Dummy	6210	-480	55.2 X 85.2
PAD371	42.8X72.8	Dummy	6270	-480	55.2 X 85.2
PAD372	42.8X72.8	Dummy	6330	-480	55.2 X 85.2
PAD373	42.8X72.8	Dummy	6390	-480	55.2 X 85.2
PAD374	42.8X72.8	Dummy	6450	-480	55.2 X 85.2
PAD375	42.8X72.8	Dummy	6510	-480	55.2 X 85.2
PAD376	42.8X72.8	V_{SS}	6570	-480	55.2 X 85.2
PAD377	42.8X72.8	V_{GND}	6630	-480	55.2 X 85.2
PAD378	72.8X72.8	V_{GND}	6705	-480	*85.2 X 85.2*
PAD379	42.8X72.8	V_{GND}	6705	-330	55.2 X 85.2
PAD380	42.8X72.8	V43	6705	-270	55.2 X 85.2
PAD381	42.8X72.8	V12	6705	-210	55.2 X 85.2
PAD382	42.8X72.8	V0	6705	-150	55.2 X 85.2
PAD383	42.8X72.8	Y001	6705	-90	55.2 X 85.2
PAD384	42.8X72.8	Y002	6705	-30	55.2 X 85.2
PAD385	42.8X72.8	Y003	6705	30	55.2 X 85.2

PAD No.	Bump size	Pad Name	X-coordinate	Y-coordinate	Pad Size (um)
PAD386	42.8X72.8	Y004	6705	90	55.2 X 85.2
PAD387	42.8X72.8	Y005	6705	150	55.2 X 85.2
PAD388	42.8X72.8	Y006	6705	210	55.2 X 85.2
PAD389	42.8X72.8	Y007	6705	270	55.2 X 85.2
PAD390	42.8X72.8	Y008	6705	330	55.2 X 85.2