Eureka Microelectronics,Inc.

EUREKA

Data Sheet

EK5221

Speech Recognition Controller

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Speech Recognition Controller

GENERAL DESCRIPTION

The Eureka Speech Recognition Controller (SRC) is a low-cost microcontroller designed for use in consumer electronics such as toys, dialers, databanks, and PDAs. It is constructed from a recognition core, A/D and D/A converters, audio amplifier and memory. The SRC is a speaker dependent speech recognizer. Its recording time is about 1 second and recognition time is less than 1 second, so it is very suitable for word and phrase recognition applications. It has a serial interface to communicate with external host controller. The SRC can be used as a stand-alone system IC or controlled by an external host. It can be quickly integrated into existing system for new applications.

FEATURES

- Store 10 custom voice patterns and expandable by external memory 2 times training operation
- Recognition time about 1 second
- Serial host interface
- 14.318 MHz operation
- Low power requirements
  - 3.0V ± 10% power supply
  - ~17.5mA in operating mode
  - ~100uA in power down mode
- 100 pin LQFP package or Bare Die

BLOCK DIAGRAM

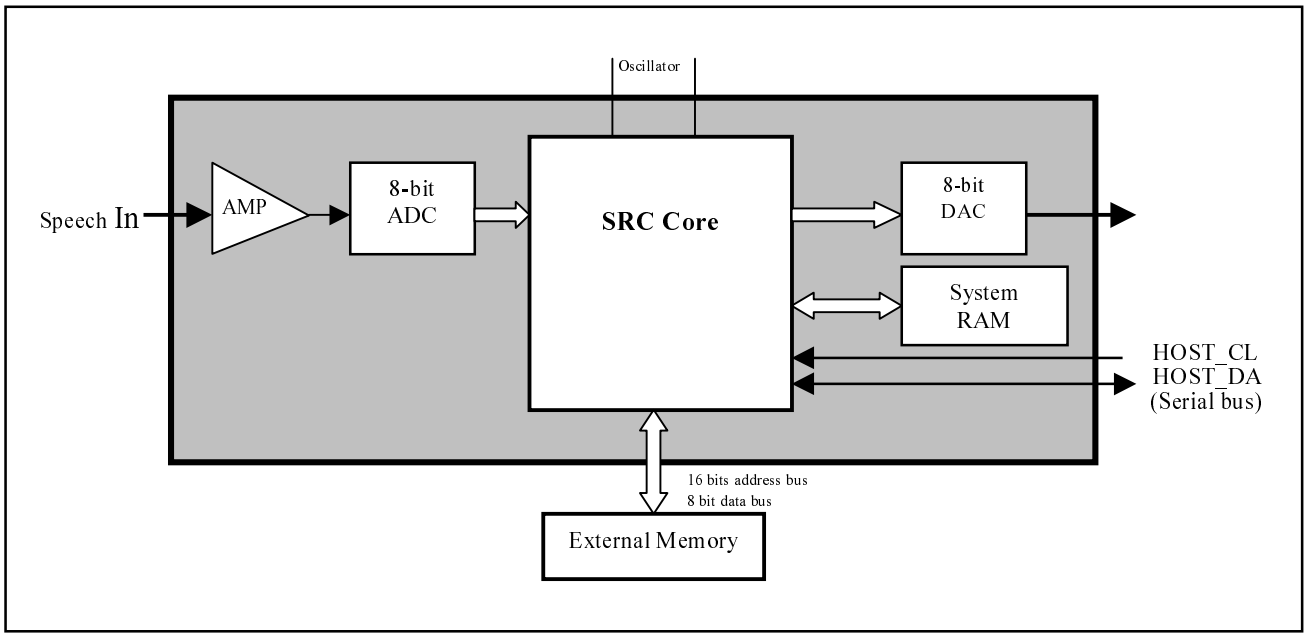


Figure 1. Block Diagram

PIN ASSIGNMENT

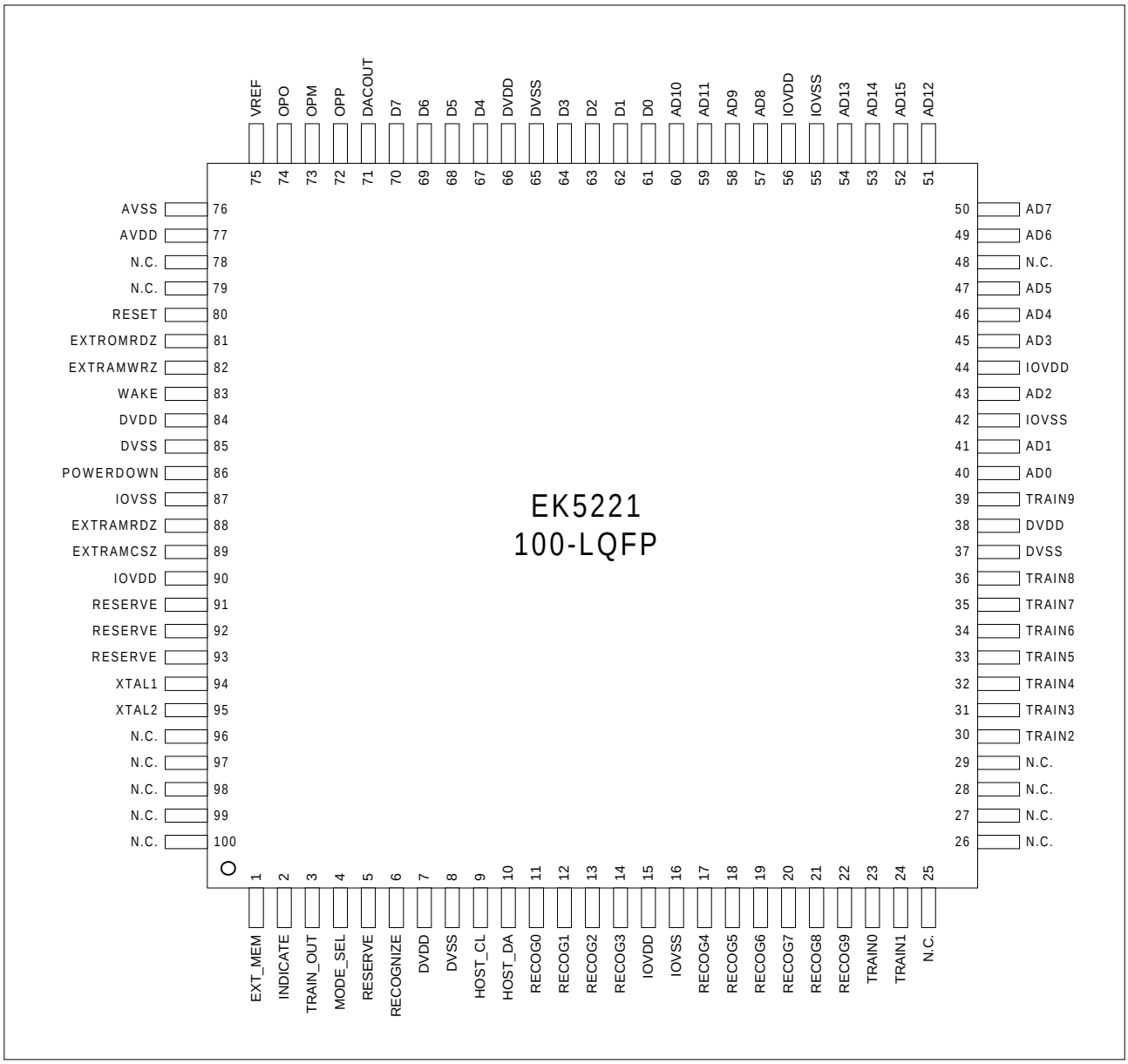


Figure 2. Pin Assignment

PAD DIAGRAM

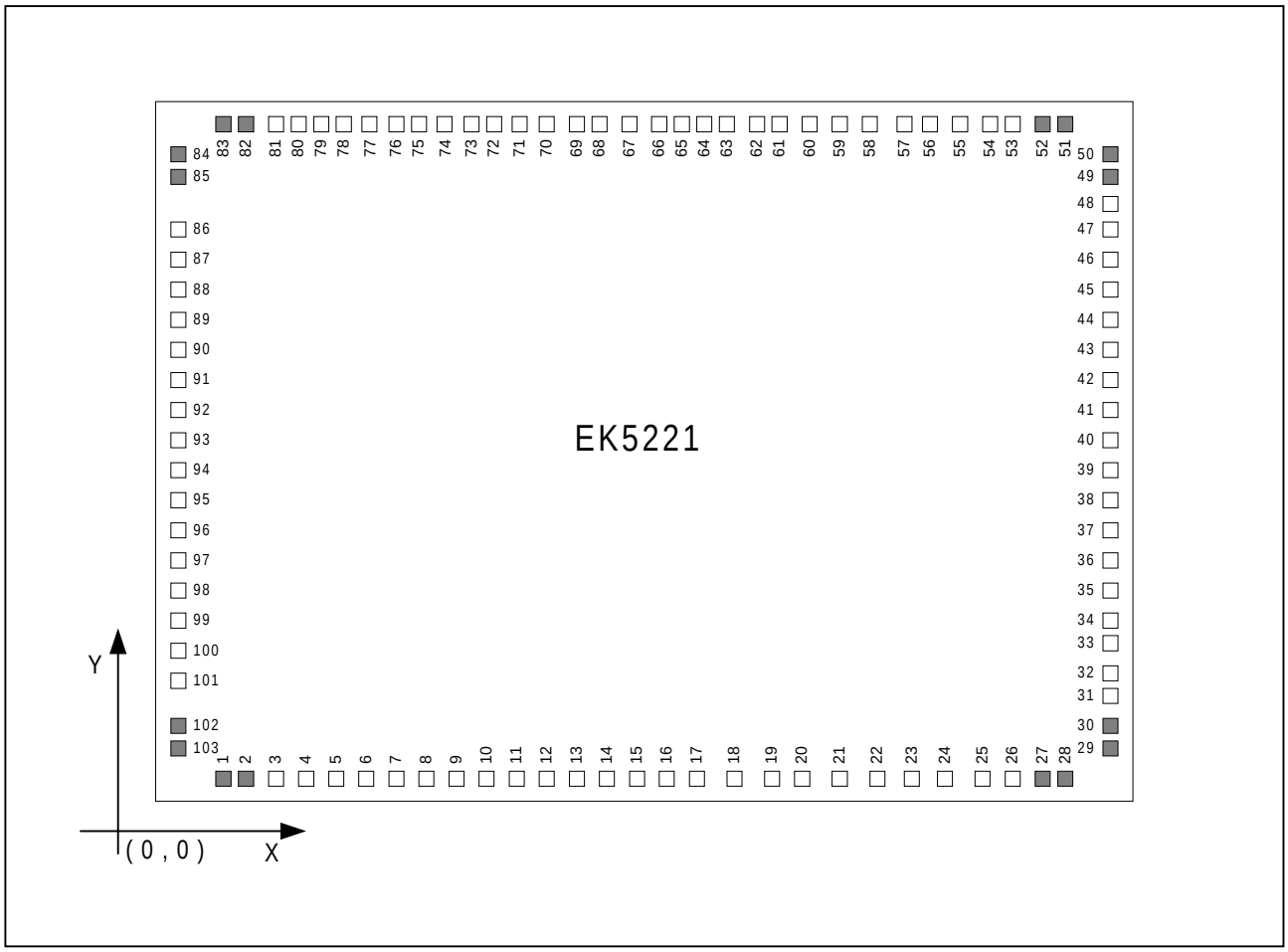


Figure 3. Pad Diagram

Ordering Information

Part Number	Package	Description
EM9701L019A	LQFP-100	Body size：14 x 14 (mm)
EM9701B019A	—	Bare Die

PIN DESCRIPTION

Symbol	Pin No.	I/O	Description
EXT_MEM	1	I	Memory control to select internal memory or external memory for storing pattern. 0: external memory; 1: internal memory.
INDICATE	2	O	Indicates a success/failure occurred during training or recognition. Success: logic "0"; failure: 1 Hz flash signal.
TRAIN_OUT	3	O	Indicates the result of training. This pin is associated with INDICATE to show the result. 1st time training : TRAIN_OUT is logic "0"; 2nd time training: TRAIN_OUT and INDICATE are logic "0" both.
MODE_SEL	4	I	This pin selects stand-alone or external host control mode. 0: stand-alone mode; 1: external host control mode.
RECOGNIZE	6	I	This pin is active low, and it initiates recognition to request action in the recognition mode.
HOST_CL	9	I	This pin is the serial clock input pin.
HOST_DA	10	I/O	This pin is the serial data input / output pin.
RECOG0~ RECOG9	11~14,17~22	O	These pins are active high, indicating which word in the memory is recognized in stand-alone mode.
TRAIN0~ TRAIN9	23~24,30~36,39	I	Input with pull up pins. Set one of them to low when you want to train one word.
AD0-AD15	40-41,43,45~47, 49~50,57~58,60, 59,51,54,53,52	O	External memory address bus.
D0-D7	61-64,67-70	I/O	External memory data bus.
DACOUT	71	O	DAC component analog Output.
OPP	72	I	Operational amplifier input pin, which connects to the internal OP noninterted input terminal.
OPM	73	I	Operational amplifier input pin, which connects to the internal OP inverted input terminal.
OPO	74	O	Operational amplifier output pin.
VREF	75	I	ADC reference voltage, which should be set to $V_{FULL\ SCALE}/2$
RESET	80	I	Reset input signal, active high.
EXTROMRDZ	81	O	External ROM read signal, active low.
EXTRAMWRZ	82	O	External RAM writes signal, active low.
WAKE	83	I	Wake up signal input pin. When the chip is in power-down mode, a low to high transition in WAKE will wake up the chip.
POWERDOWN	86	O	Power-down indication output pin, active high. When the chip is in power-down mode the crystal oscillator will be disabled.
EXTRAMRDZ	88	O	External RAM read signal, active low..

Symbol	Pin No.	I/O	Description
EXTRAMCSZ	89	O	External RAM select signal, active low.
XTAL1	94	I	Crystal input pin for generating system clock. The frequency of the crystal is 14.318 MHz.
XTAL2	95	O	Crystal output pin.
DVDD	7,38,66,84	-	Digital supply voltage.
DVSS	8,37,65,85	-	Digital ground.
AVDD	77	-	Analog supply voltage.
AVSS	76	-	Analog ground.
IOVDD	15,44,56,90	-	Digital supply voltage for input / output pad.
IOVSS	16,42,55,87	-	Digital ground for input / output pad.
RESERVE	5,91~93	-	Reserved. This pin is reserved for future us and should be left open.
N.C.	25~29,48,78~79, 96~100	-	No connection.

FUNCTION DESCRIPTIONS

• Voice Recognition

The Eureka Speech Recognition Controller IC is a speaker dependent speech recognizer. The SRC can support multiple speakers by switching a word or phrase, but only one speaker's words or phrase can be recognized at one time. Users need to train the chip by speaking the word or phrase two times. After training, the SRC extracts significant features stored in its memory. Then, when the user speaks the SRC compares the features of the word or phrase spoken with the previously trained features in order to recognize which word or phrase has been spoken. The SRC will reply to the recognition result. Output pins provide result information to external devices.

Therefore, the SRC can provide a complete interactive user interface. The SRC provides a serial interface to communicate with the external host control mode, and is available as a stand-alone system IC.

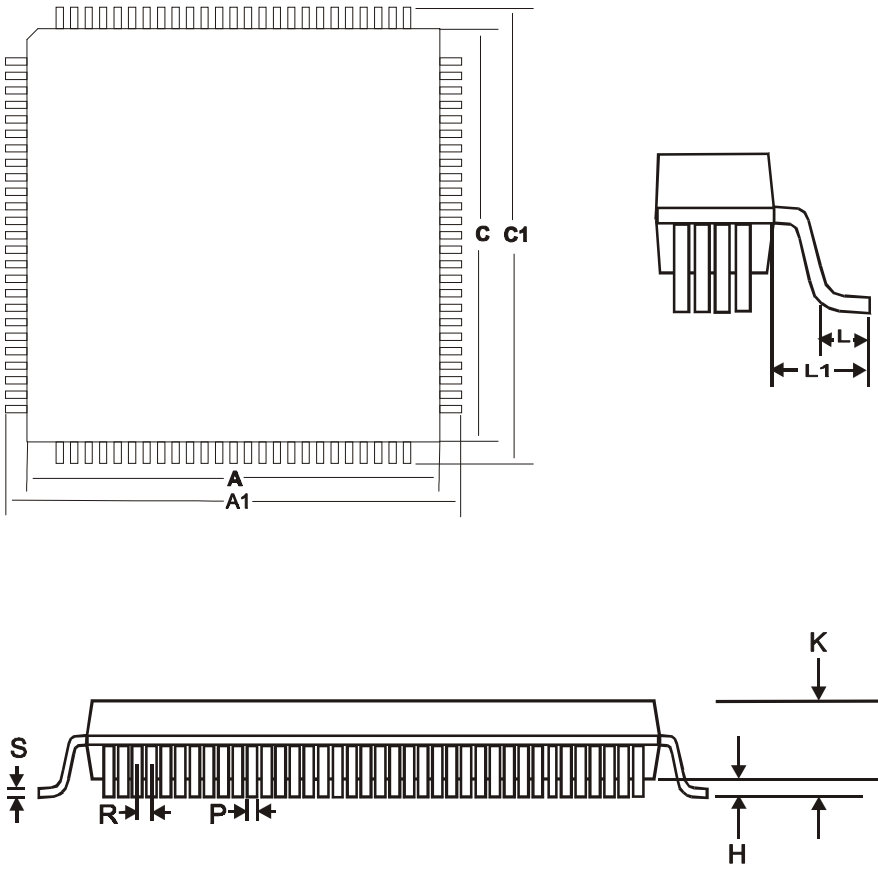
• Memory Interf ces

The internal memory manages SRAM and ROM, in conjunction with the internal memory for voice features and working memory. Stand-alone mode works with no external memory, external host control mode can use external memory.

In the external host control mode, the SRC allows use of ROM, SRAM, and flash memory. For accessing the ROM and RAM address spaces, the SRC provides a separate write RAM (EXTRAMWRZ), read RAM (EXTRAMRDZ), read RAM (EXTRAMRDZ), RAM select (EXTRAMCSZ), and ROM read (EXTROMRDZ) signals. The SRC communicates through serial interface.

Package Mechanical Drawing

100 PIN LQFP
PACKAGE OUTLINE



	Dimension in inch (BASE)			Dimension in mm (REF)		
	min	nom	max	min	nom	max
A	0.53	0.551	0.57	13.5	14	14.5
A1	-	-	0.63	-	-	16
C	0.53	0.551	0.57	13.5	14	14.5
C1	-	-	0.63	-	-	16
H	0.004	-	0.008	0.09	-	0.2
J	0.053	0.055	0.057	1.35	1.4	1.45
K	-	-	0.063	-	-	1.6
L	0.018	0.024	0.03	0.45	0.6	0.75
L1	-	0.039	-	-	1	-
P	-	0.008	-	-	0.203	-
R	-	0.020	-	-	0.508	-
S	-	0.003	-	-	0.08	-