eCOG1 Microcontroller

Low Power Communications Processor

PRELIMINARY

The eCOG1 microcontroller is a low-power microcontroller based on a 16-bit Harvard architecture with a 24-bit word code linear address space (32Mbyte) and 16-bit word linear data address space (128Kbytes). It is available in a 128-pin LQFP with or without the IntAct high-speed serial interface. A comprehensive toolset and C Compiler are available.

- 0 to 25MHz 3.3V processor
- Powerful arithmetic operations
- Barrel Shifter
- Harvard Architecture
- 64Kx16 Data Memory
- 16Mx16 Program Memory
- Built in Emulator (eICE)
- Low power operation
- 64Kbytes FLASH EPROM
- 4Kbytes SRAM
- MMU
- Power-saving code cache
- Code security feature
- External Host Interface
- External Memory Interface
- Fast Vectored Interrupts
- Dual UART
- Dual USART
- Smart Card Interface
- SPI
- I2C
- Consumer IR/IRDA
- 4 channel 12-bit A/D
- Parallel Interface
- 5 Multi Purpose Timers
- Watchdog Timer
- Long Interval Timer
- Real Time Clock
- PWM timers
- Temperature Sensor
- Supply Voltage Sensor
- Power-On Reset
- General Purpose I/O
- 25MHz from watch XTAL
- Interfaces to 8/16/32-bit parts

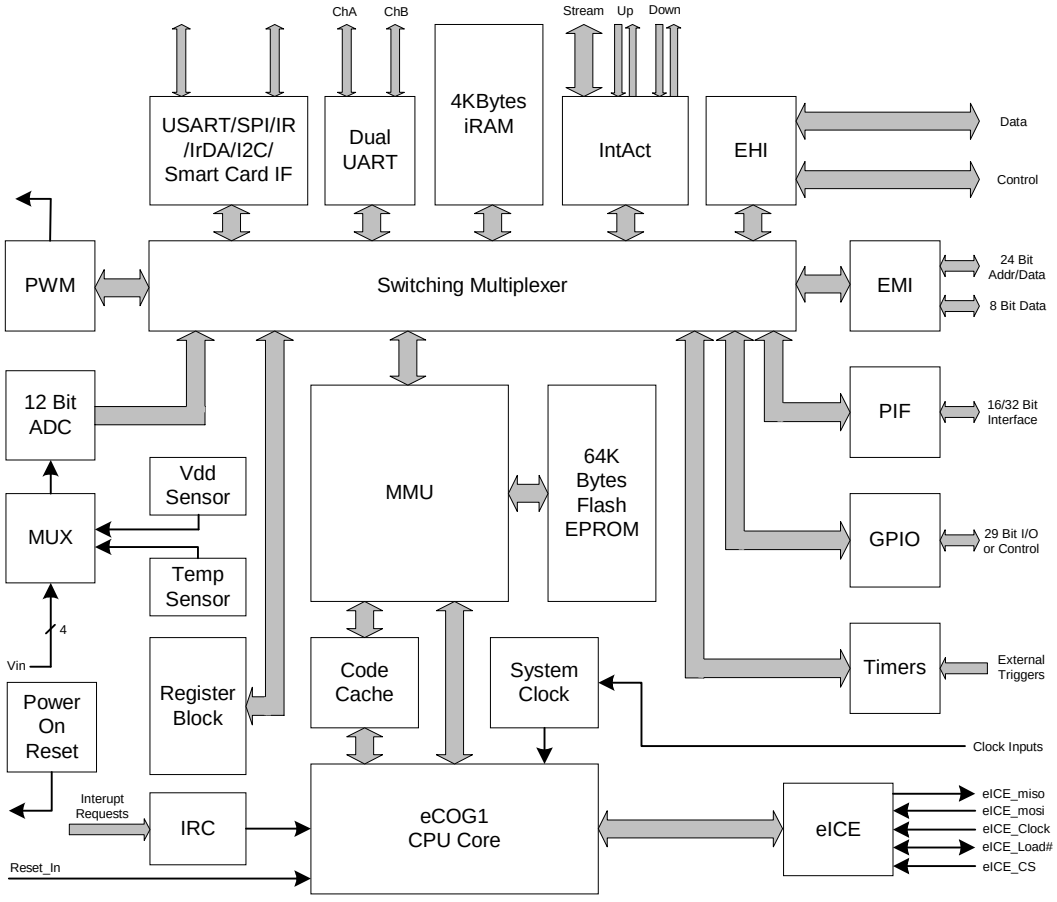


Figure 1 – Internal Block Diagram

CPU Core
- 16-bit 25MHz register-based core
- Harvard architecture
- Supports a full array of 16-bit arithmetic operations, including both signed and unsigned MULtiply and DIVide instructions
- 32MByte linear program memory
- 128KByte linear data memory
- Vectored interrupts

Flash EPROM
- 64Kbytes organized as 32Kx16
- Organized as eight 4Kx16 banks
- Individual Flash banks can be read and/or write protected
- Built in programming algorithm is available under application software control

Code Cache
- 512 line cache
- Reduces power consumption while improving performance
- Both deterministic and non-deterministic modes
- Individual cache lines can be locked
- Can cache both User and Interrupt Mode

MMU
- Performs logical to physical address translations
- Translates between RAM, Program Memory, and external memory devices for both code and data accesses concurrently
- Lookup tables in RAM or Flash can be mapped between each memory area
- Up to 2 concurrent translations to external devices from code addresses
- Up to 3 concurrent translations to external devices from data addresses
- Wait states automatically generated
- Concurrent accesses to same device are prioritized
- Translations are prioritized to allow overlapped translations

DUART
- Two independent RS232 compatible asynchronous double-buffered serial ports
- Full modem support (CTS, RTS, DSR, DTR, DCD, and RI)
- Supporting 5, 6, 7, or 8-bits of data
- 1, 1.5, or 2 stop bits
- Even, odd or no parity
- Automatic end-of-frame guard time insertion of 0- to 64-bit periods
- Receive time-out detection 0 to 64-bit periods
- Software Line Break generation
- Programmable Baud rate generator
- Interrupts generated on full and empty
- Receiver error detection for false start bits, parity errors and frame errors
- Configurable data polarity
- Over-sampling of received data for noise immunity

DUSART
- Two synchronous/asynchronous double-buffered serial ports
- Programmable baud rate generator
- End of frame guard time insertion of 0 to 64-bit periods
- Receive time-out detection 0 to 64-bit periods
- Receiver error detection for false Start bits, Parity errors, Frame errors and Buffer overflow
- Configurable data and clock polarity
- Configurable data packing, MSB or LSB first
- Over sampling receive data for noise immunity

Asynchronous Interface:
- Asynchronous frames supporting 5, 6, 7, or 8-bits of data
- 1, 1.5, or 2 stop bits
- Even, odd or no parity
- Full modem support (CTS, RTS, DSR, DTR, DCD, and RI)
- Software Line Break generation

Synchronous Interface:
- Local or external transmit and receive clock
- Full or half duplex
- Frame sizes from 1 to 16-bits with larger frames possible
- Support for NRZ, RZ
- PM, PWM and ASK modulation if used in conjunction with PWM timer

Host Control Port (HCP)
- Provides direct access internal registers of each USART
- Custom serial protocols may be emulated
- Up to 255 symbols per frame
- Parity may be automatically inserted or tested at the end of each frame
- Start bit edge detection
- Tx/Rx interrupts

SPI
- Multi-slave SPI system
- Four slave select lines
- Both master and slave roles
- Programmable clock polarity and clock/data phase

Smart Card Interface
- ISO 7816 compatible smart card interface
- Multiprocessor support
- Byte level support for T=0 and T=1 transmission protocols
- Detection and generation of the transmission error signal for T=0 protocol
- Automatic retransmission of corrupted bytes for T=0 protocol
- Independent controls for power and ground switching
- Hardware state machine for power up, reset and shutdown sequences

Consumer IR / IrDA
- Programmable baud rates
- Support for low rate (<115.2 kbps) IrDA framing and modulation
- Compatible with common ASK, PM, PPM (e.g. RC-5) modulation schemes
- Variable frame lengths up to 255 bits
- Variable length multi-byte frames
- Half duplex operation supported using an integral transceiver frame duration (maximum 1023 symbols) to separate transmit and receive exchanges
- Raw IR mode (software modem) supported
- Programmable start, stop, data length, frame length and polarities
- Programmable start and stop sequences
- Support for current and future frame formats
- Carrier frequency generation

I^2C
- Two wire I2C compatible port
- Address matching
- ACK bit and wait state insertion
- Multi-master arbitration
- Supports 10-bit addressing and fast mode

External Host Interface (EHI)
- Provides a DMA interface to an external host or FIFO
- Memory mapped peripheral port
- Supports master and slave mode timing
- 16/32-bit data bus
- Request & Acknowledge control lines
- Configurable master mode timing
- Direct DMA connection into internal SRAM (11-bit block address, max 256 byte block size)
- Internal DMA controller supports circular buffer and link list buffer models
- 8-bit external address with 16-bit data
- 3-bit external address with 32-bit data
- Three control lines: chip select, direction and wait
- Configurable control line senses
- Interrupt generated upon transfer

General Purpose I/O (GPIO)
- 29 memory mapped GPIO pins
- Configured as Input, Output, bi-directional
- Directly drive or open drain outputs
- Direct drive LEDs
- Each input can generate an interrupt

External Interrupts
- Any GPIO configured as an Input can generate an interrupt
- Level or edge sensitive interrupts

Parallel Interface (PIO)
- Two 16-bit parallel data ports
- Directly drive, open drain, or tri-state outputs

Timers
- 16-bit Watch Dog Timer
- 16-bit Real Time Clock
- 24-bit Long Interval Timer
- Two 16-bit PWMs CGT1 and CGT2
- Two 16-bit General Purpose Timers/event counters (GPT)
- 16-bit timer (CPT) with multiple event capture registers
- 16-bit ripple counter
- Most timers have pre-scalars

External Memory Interface

- Operates as bus Master and Slave
- Big-endian or little-endian
- Allows both DMA and non DMA accesses to internal memory and I/O registers
- 8, 16 or 32-bit data bus as Master
- 24-bit address bus as Master
- Multiplexed address/data for 16 and 32-bit data busses as Master
- Supports 8-bit and 16-bit transfers as Slave
- 16 and 32-bit data bus and accesses as Slave
- Flag Register for software generated interrupt
- Supports up to 128M Single Data Rate 16-bit wide SDRAMs
- Four Row/Column SDRAM address multiplexing schemes
- SDRAM auto and self refresh supported
- Configurable timing
- Low power SDRAM suspend/standby mode
- SDRAM can be mapped into both code and data space
- Single cycle data space access, code space burst access in conjunction with Code Cache
- Hardware support for software initialization and refresh of SDRAM

Analog Functions

- 12-bit ADC with 8KHz sampling, differential input
- On-chip temperature sensor
- On-chip Power Supply Monitor
- 4 channel analog multiplexer with four input modes:
  - i) Four channel inputs to the ADC for single ended use, using internal voltage reference
  - ii) Three channel inputs to the ADC, one input as external reference
  - iii) Three channel inputs to the ADC, one port as output of the internal reference voltage
  - iv) Two differential inputs

IntAct

- Amino Communications proprietary IntAct® interface
- Secure, high speed communications
- Typically 180Mbit/s data rate
- Provides virtual circuit connections between IntAct devices
- Permits inter-processor communications

Clocks

- Two crystal oscillators
- Low cost 32KHz watch crystal can generate 25MHz internal clock
- Internal PLL
- Second oscillator uses a 5MHz crystal to generate 25MHz internal clock with low jitter

C Compiler suite

- ANSI C Compiler
- Validated to ANSI/ISO/FIPS-160
- ANSI Standard Library
- Macro Assembler
- Software Simulator and debugger

eICE Debugger Interface

- Real-time debug port
- Can program internal Flash
- When BREAK command is locked in the cache, can provide virtually unlimited address breakpoints
- Commands include Reset, Stop, Run, Run to Break
- Non-intrusive read and write to any core register, including PC
- Read and write of any memory location

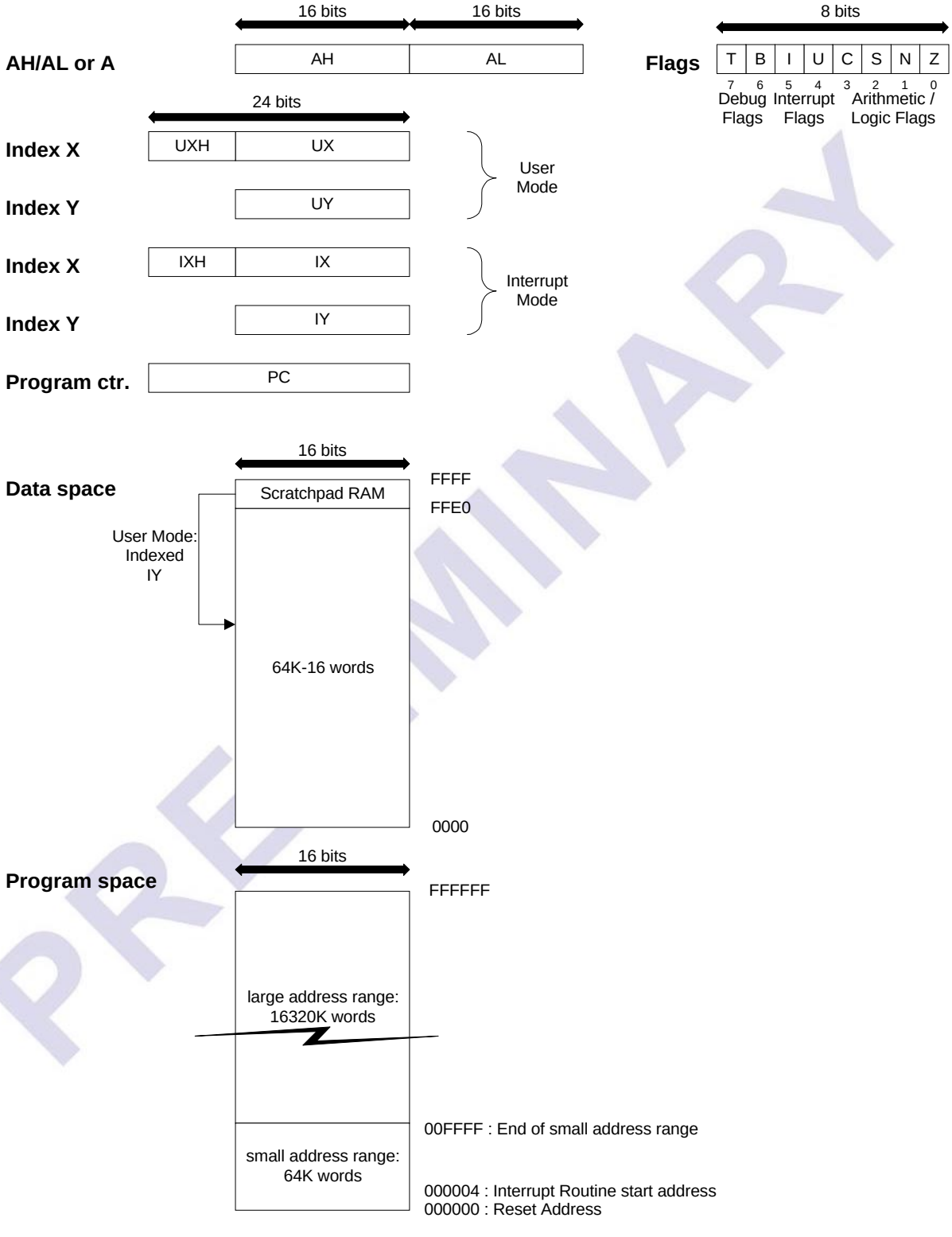
Power Saving Features

- Sleep mode with wake on interrupts
- All peripherals have individual clock domains and can be stopped when not in use

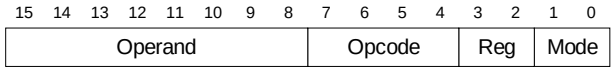
External Ports

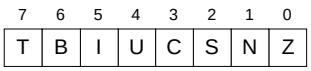
- Peripherals are connected to multiple device pins
- Each port has a unique multiplexing scheme to select port configuration
- Two 4-bit ports
- Ten 8-bit ports

Programmer's Model



Instruction Set





Operand	*Opcode*	*Reg*	*Mode*	*Assembler*		*Operation*	*Flags*
not H'00	H'0	00	00	PREFIX	operand	ARG_EXT = (ARG_EXT<<8) + operand	-
H'00	H'0	00	00	NOP		None	-
H'00	H'0	01	00	BRK		Stop for debug	-
H'00	H'0	10	00	SLEEP		Enter sleep mode	-
H'00	H'0	11	00	SIF		Perform ESIF access during instruction	-
-	H'0	00	01	ST flags	@(<nn>,y)	@(<nn>,y)← flags	-
-	H'0	01	01	LD flags	@(<nn>,y)	flags ← @(<nn>,y)	ALL
-	H'0	11	01	RTI	@(<nn>,y)	PC ← {IXH, IX}; flags ← data	ALL
H'00	H'0	10	01	UNSIGNED		Operation modifier: unsigned	-
H'01	H'0	10	01	SIGNED		-	
H'FF	H'0	10	01	BC		for(AL; AL>0; AL--) @(Y++) ← @(X++)	-
H'FE	H'0	10	01	BRXL		PC ← PC + X[15:0] + 1. X[15:0] sign extended.	-
-	H'0	00	10	ST UX	@(<nn>,y)	@(<nn>,y) ← UX[15:0]	-
-	H'0	01	10	LD UX	@(<nn>,y)	UX[15:0] ← @(<nn>,y)	-
-	H'0	10	10	ST XH	@(<nn>,y)	@(<nn>,y) ← (U==1) ? UX[23:16] : {IX[23:16], UX[23:16]}	-
-	H'0	11	10	LD XH	@(<nn>,y)	(U==1) ? UX[23:16] : {IX[23:16], UX[23:16]} ← @(<nn>,y)	-
-	H'0	00	11	ST UY	@(<nn>,y)	@(<nn>,y) ← UY[15:0]	-
-	H'0	01	11	LD UY	@(<nn>,y)	UY[15:0] ← @(<nn>,y)	-
-	H'1	-	-	LD	reg, data	reg ← data	NZ
-	H'1	-	-	LD.B†	reg, data	reg[15:0] ← data[7:0] or data[15:8] – sign expended	NZ
-	H'1	-	-	LD.BU†	reg, data	reg[15:0]← data[7:0] or data[15:8] – zero extended	NZ
-	H'2	-	00	PRINT	reg, data	None. Debug request for simulators.	-
-	H'2	-	not-00	ST	reg, data	data ← reg	NZ
-	H'2	-	not-00	ST.B†	reg, data	data[7:0] ← reg[7:0]	NZ
				MOV	regd,AL	regd[15:0] ← AL[15:0]: regd == X, XH and Y	
				MOV	regx,AH	regx[15:0] ← AH[15:0]: regx == X, and XH	
				MOV	rega, Y	rega[15:0] ← Y[15:0]: rega == AH and AL	
				MOV24	X:,A	XH[7:0] ← AH[7:0], X[15:0] ← AL[15:0]	

Reg Register Access Field

Reg field	*reg*	*regd*	*regx*	*rega*
00	AH			AH
01	AL	XH	XH	AL
10	X	X	X	
11	Y	Y		

† Indicates UNSIGNED prefix instruction required for this instruction.
<nn> represents the instruction operand for instructions with a specific addressing mode.

Operand	*Opcode*	*Reg*	*Mode*	*Assembler*		*Operation*	*Flags*
-	H'3	-	-	ADD	reg, data	reg ← reg + data	CSNZ
-	H'4	-	-	ADDC	reg, data	reg ← reg + data + C	CSNZ
-	H'5	-	-	SUB	reg, data	reg ← reg – data	CSNZ
-	H'6	-	-	SUBC	reg, data	reg ← reg – data – C	CSNZ
-	H'7	-	-	NADD	reg, data	reg ← -reg + data	CSNZ
-	H'8	-	-	CMP	reg, data	flags ← reg – data	CSNZ
-	H'9	00	-	UMULT†	data	A ← AL * data	-
-	H'9	00	-	SMULT	data	Sign Extend. A ← AL * data	-
-	H'9	01	-	UDIV†	data	AL ← A ÷ data; AH ← rem	-
-	H'9	01	-	SDIV	data	Sign Extend. AL ← A ÷ data; AH ← rem	-
-	H'9	10	-	TST	data	flags ← data	NZ
-	H'9	11	-	BSR	addr	X ← PC + 1; PC ← branch_addr	-
-	H'A	00	-	ASL	data	C←[AH, AL]←0	C
-	H'A	00	-	LSL	data	C←[AH, AL]←0	C
-	H'A	01	-	ASR	data	AH[15]→[AH, AL]→C	C
-	H'A	01	-	LSR†	data	0→[AH,AL]→C	C
-	H'A	10	-	ROL	data	C←[AH,AL]←C	C
-	H'A	11	-	ROR	data	C→[AH,AL]→C	C
-	H'B	-	-	OR	reg, data	reg ← reg | data	NZ
-	H'C	-	-	AND	reg, data	reg ← reg & data	NZ
-	H'D	-	-	XOR	reg, data	reg ← reg ^ data	NZ
-	H'E	00	-	BRA	addr	PC ← branch_addr	-
-	H'E	01	-	BLT	addr	if S = 1 PC ← branch_addr	-
-	H'E	10	-	BPL	addr	if N = 0 PC ← branch_addr	-
-	H'E	11	-	BMI	addr	if N = 1 PC ← branch_addr	-
-	H'F	00	-	BNE	addr	if Z = 0 PC ← branch_addr	-
-	H'F	01	-	BEQ	addr	if Z = 1 PC ← branch_addr	-
-	H'F	10	-	BCC	addr	if C = 0 PC ← branch_addr	-
-	H'F	11	-	BCS	addr	if C = 1 PC ← branch_addr	-

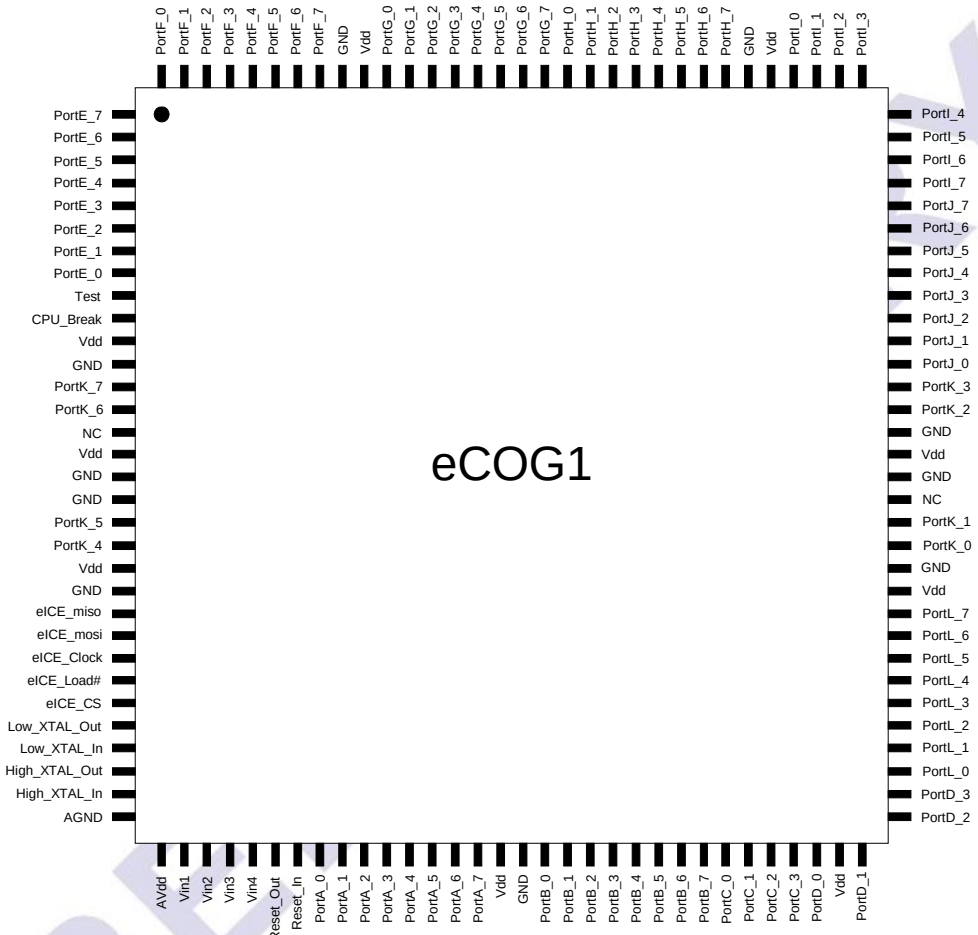
Mode Field

mode	*Data Mode : source or destination*		*Address Mode: Branch Address*	
00	Immediate	data = 16-bit sign extended operand	PC relative	PC + 24-bit operand
01	Direct	data = 16-bit value @ 16-bit operand address	Direct	{XH, @ 16-bit operand address}
10		data = 16-bit value @ X+16-bit operand address	X Relative	{XH, X} + 24-bit sign extended operand
11	Indexed Y	data = 16-bit value @ Y+16-bit operand address	Indexed Y	{XH, @(Y + 16-bit operand)}

mode	*Data Mode Byte Accesses: source or destination*	
00	unused	
01	Direct	data = 8-bit value @ 17-bit operand byte address
10	Indexed X	data = 8-bit value @ 17-bit byte address in {XH,X}+17-bit operand byte address
11	Indexed Y	data = 8-bit value @ 16-bit word address in Y+17-bit operand byte address

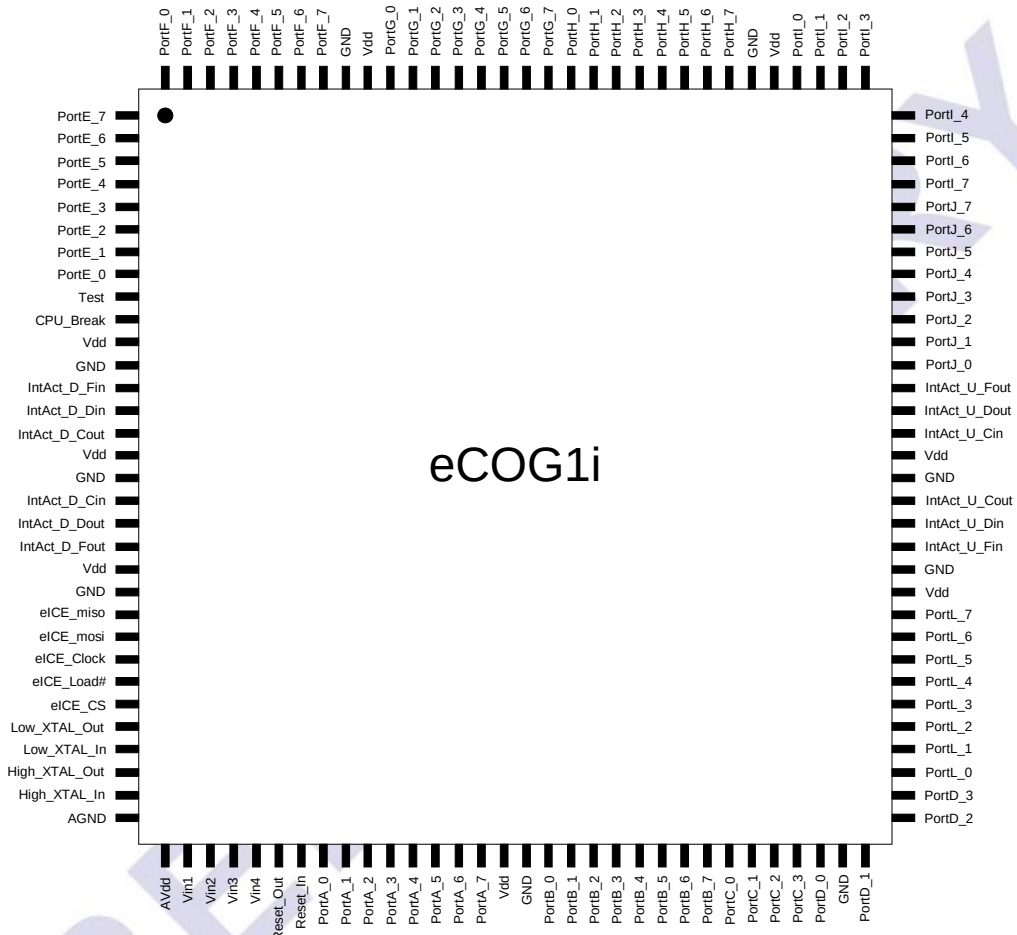
Pin Out of Port K version.

128 pin LQFP. Pin pitch 0.4mm. 14x14mm body. 16x16mm at pin edge.



Pin Out of IntAct version.

128 pin LQFP. Pin pitch 0.4mm. 14x14mm body. 16x16mm at pin edge.



Revision History.

V1.0	First release.
V1.1	Text corrections.
V1.2	Text corrections and new layout.
V1.3	Final pin out.
V1.31	Final final pin out!
V1.32	5 volt compliant inputs removed from datasheet. Not available on first rev.
V1.4	Pin descriptions and port mapping added. Minor changes to block diagram.
V1.41	Additional pin description info. EMI pin out changed. Signal names changed in keeping with industry norm.
V1.42	Additional pin description info.
V 2.0	Layout cleaned up and list of features revised for clarity. Pin out tables removed for brevity
V2.0a	Cleaned up for style – first official outside release 21-Jan-2002
V3.0/a	Clarified some text; Used American English spelling 19-Feb-2002
V3.1	Minor format changes, changed paper size to US Letter

I2C, I^2C, and the I2C interface are patented by Philips Semiconductor. Philips may demand a royalty from designs using the I2C interface.

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