Edge737
Per-Pin Precision Measurement Unit

Description

The Edge737 is a precision measurement unit designed for automatic test equipment and instrumentation. Manufactured in a wide voltage CMOS process, it is a monolithic solution for a per pin PMU.

The Edge737 supports two modes of operation: force current/measure voltage and force voltage/measure current. The Edge737 can force or measure voltage in the range of +7V to –5V. In addition, the Edge737 can force or measure a current of up to 40 mA over four distinct ranges: ± 40 mA, ± 1 mA, ± 100 µA and ± 10 µA.

The Edge737 has an on board window comparator that provides three bits of information: DUT too high, DUT too low, and DUT fail. There is also a monitor function which provides a real time analog voltage signal proportional to either the DUT voltage or current.

On board clamps prevent large transient spikes when changing operating mode or current range. Also, the PMU will survive a direct short over the legal voltage range.

The Edge737 is designed to be a low power, low cost, small footprint solution to allow high pin count testers to support a PMU per pin.

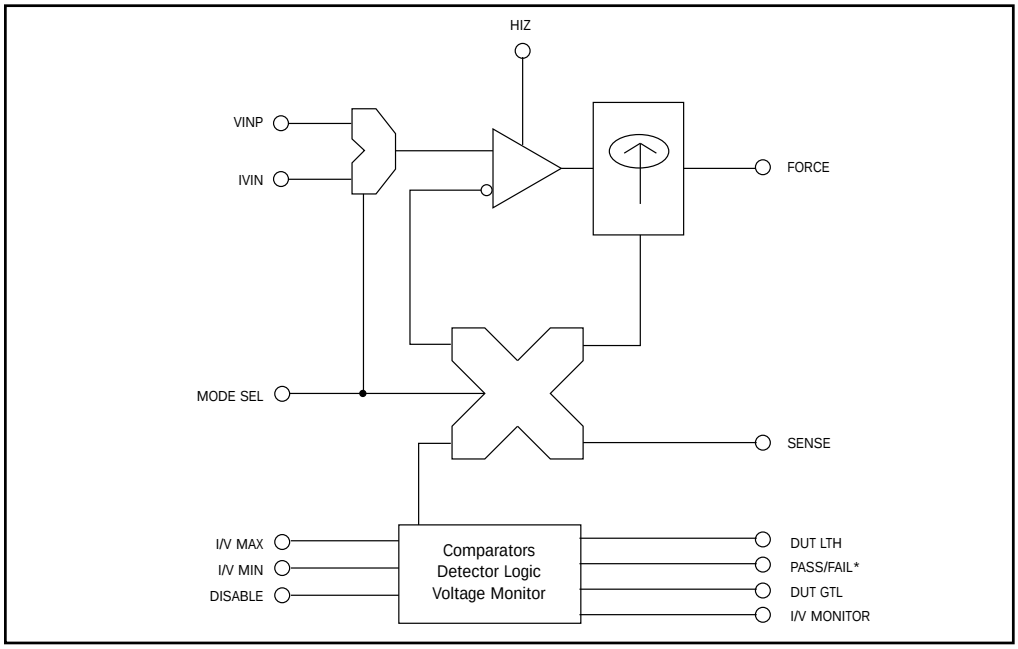
Features

- FV / MI Capability
- FI / MV Capability
- 4 Current Ranges (± 40 mA, ± 1 mA, ± 100 µA, ± 10 µA)
- +7V / –5V I / O Range
- Short Circuit Protection
- Clamps for limiting mode and range select transients

Applications

- Automatic Test Equipment
  - Memory Testers
  - VLSI Testers
  - Mixed Signal Tester

Functional Block Diagram

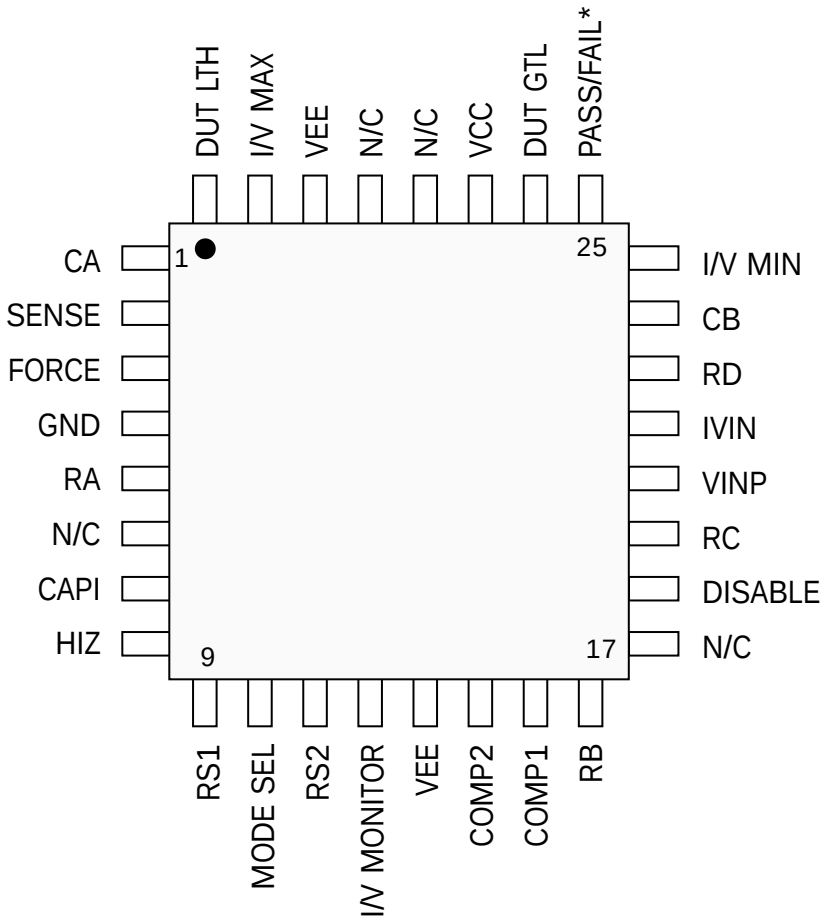


Pin Description

Pin Name	Pin #	Description
VINP	20	Analog voltage input which forces the output voltage at FORCE (FV/MI mode).
IVIN	21	Analog voltage input which forces the output current at FORCE (FI/MV mode).
FORCE SENSE	3 2	Analog output pin which forces current or voltage. Analog input pin which senses voltage (typically connected to FORCE).
MODE SEL	10	TTL compatible input which determines whether the PMU is forcing voltage or forcing current.
RS1, RS2	9, 11	TTL compatible inputs which select one of the four current ranges.
I/V MIN I/V MAX	24 31	Analog input voltages which establish the lower and upper threshold level for the measurement comparator.
DUT LTH DUT GTL	32 26	Digital comparator open drain outputs that indicate the DUT measurement is less than the upper threshold and greater than the lower threshold.
PASS/FAIL*	25	Digital output that indicates whether or not the monitored voltage is between the comparator thresholds. Logic1 corresponds to a measurement that is between comparator thresholds.
DISABLE	18	TTL compatible input which places the digital comparator outputs and I/V MONITOR in high impedance.
HiZ	8	TTL compatible input which places the FORCE output into high impedance.
RA, RB, RC, RD	5, 16 19, 22	External resistors corresponding to ranges A through D.
I/V MONITOR	12	Analog voltage output that provides a real time monitor of either the measured voltage or measured current level.
COMP1 COMP2	15 14	External compensation pins that require an external capacitor connected between the two pins.
VCC	27	Positive analog power supply.
VEE	13, 30	Negative analog power supply.
CA CB	1 23	External compensation pins that require an external capacitor connected between the two pins.
CAPI	7	External compensation pins that require an external capacitor connected to ground.
GND	4	Ground.

Pin Description *(continued)*

32 Pin TQFP
(7 mm x 7 mm x 1.4 mm)
(Top View)



Circuit Description

Circuit Overview

The Edge737 is a parametric test and measurement unit that can :

- Force Voltage / Measure Current
- Force Current / Measure Voltage.

The Edge737 can force or measure voltage over a +7V to -5V range, and force or measure current over four distinct ranges:

- ± 40 mA
- ± 1 mA
- ± 100 µA
- ± 10 µA.

An on board window comparator provides three-bit measurement range classification. Also, a monitor passes a real time analog signal which tracks either the DUT's current or voltage performance.

Control Inputs

MODE SEL is a TTL compatible input which determines whether the PMU forces voltage or current, when it is not placed in a high impedance state by the HIZ input (see Table 1).

HIZ	Mode SEL	PMU Operation
1	X	High Impedance
0	0	FV / MI
0	1	FI / MV

Table 1.

RS1 and RS2 are TTL compatible inputs to an analog MUX which establishes the full scale current range of the PMU. One of four current ranges can be selected by using RS1 and RS2 as shown in Table 2.

Rext Nom	RS1	RS2	Current Range
RA = 200KΩ	0	0	A: ± 10 µA
RB = 20KΩ	0	1	B: ± 100 µA
RC = 2KΩ	1	1	C: ± 1 mA
RD = 50Ω	1	0	D: ± 40 mA

Table 2.

Comparator Outputs

The comparator outputs DUT GTL, DUT LTH, and PASS/FAIL* are open drain outputs. When active (logical 0), they will pull to ground. When disabled (logical 1 or DISABLE = 1), they require an external pull up resistor to a positive voltage to achieve a high state.

Force / Sense

FORCE is an analog output which either forces a current or forces a voltage, depending on which operating mode is selected.

The SENSE pin is a high impedance analog input which measures the DUT voltage input in the FI / MV operating mode.

FORCE and SENSE are brought out to separate pins to allow for remote sensing.

I/V MONITOR

I/V MONITOR is a real time analog output which tracks the sensed parameter. I/V MONITOR functionality is described in Table 3.

Disable	Mode SEL	I/V Monitor
1	X	High Impedance
0	0	Measured Current
0	1	Measured Voltage

Table 3.

In the FI / MV mode, the output voltage is a 1:1 mapping of the DUT voltage. In the FV / MI mode, I/V MONITOR follows the equation:

$$I(measured) = I/V\ MONITOR / (4.0 * REXT).$$

Using nominal values for the external resistors, I/V MONITOR of +8.0V corresponds to Imax and –8.0V corresponds to Imin of the selected current range.

Circuit Description *(continued)*

HIZ

HIZ is a TTL compatible input which places the FORCE output into a high impedance state, regardless of the operating mode (forcing current or voltage.) This function allows the PMU to be connected directly to the pin electronics without an isolation relay while NOT adding any leakage current.

DISABLE

DISABLE is a TTL compatible input which places DUT LTH, DUT GTL, I/V MONITOR, and PASS/FAIL* into high impedance states.

Force Voltage / Measure Current Mode

In the FV / MI mode, VINP is a high input impedance, analog voltage input that maps directly to the voltage forced at the DUT (see Figure 1), where FORCE = VINP.

A current monitor is connected in series with the Op Amp driving the FORCE voltage. This monitor generates a voltage that is proportional to the current passing through it, and its output is brought out to I/V MONITOR. The monitor's voltage may also be evaluated using the Window Comparator whose operation is in accordance with the FV/MI functional truth table (Table 6).

I/V MAX and I/V MIN are high impedance analog inputs that establish the upper and lower thresholds for the window comparator (see Table 4). In the FV / MI mode, a maximum voltage input corresponds to at least a maximum current output. Positive current is defined as current flowing out of the PMU.

I/V MAX I/V MIN	Comparator Threshold
+8.0V 0V –8.0V	> Imax (full scale) 0 < Imin (full scale)

Table 4.

The voltage at I/V MONITOR follows the equation:
I(measured) = I/V MONITOR / (4.0 * REXT).
Nominally, the external resistors (RA, RB, RC, and RD) should be chosen such that Imax * REXT = 2.0V.

Force Current / Measure Voltage Mode

In the FI / MV mode, IVIN is a high input impedance, analog voltage input that is converted into a current (see Table 5) using the following relationship:

$$FORCE = IVIN / (4.0 * REXT)$$

with positive current is defined as current flowing out of the PMU.

IVIN	Forced Current
+8.0V 0V –8.0V	Imax (full scale) 0 Imin (full scale)

Table 5.

The resulting DUT voltage is then tested via the SENSE input by a window comparator, whose functional truth table is shown in Table 7.

I/V MAX and I/V MIN are high impedance analog inputs that establish the upper and lower thresholds for the window comparator. In the FI / MV mode, the reference inputs translate 1:1 to SENSE level thresholds.

Circuit Description *(continued)*

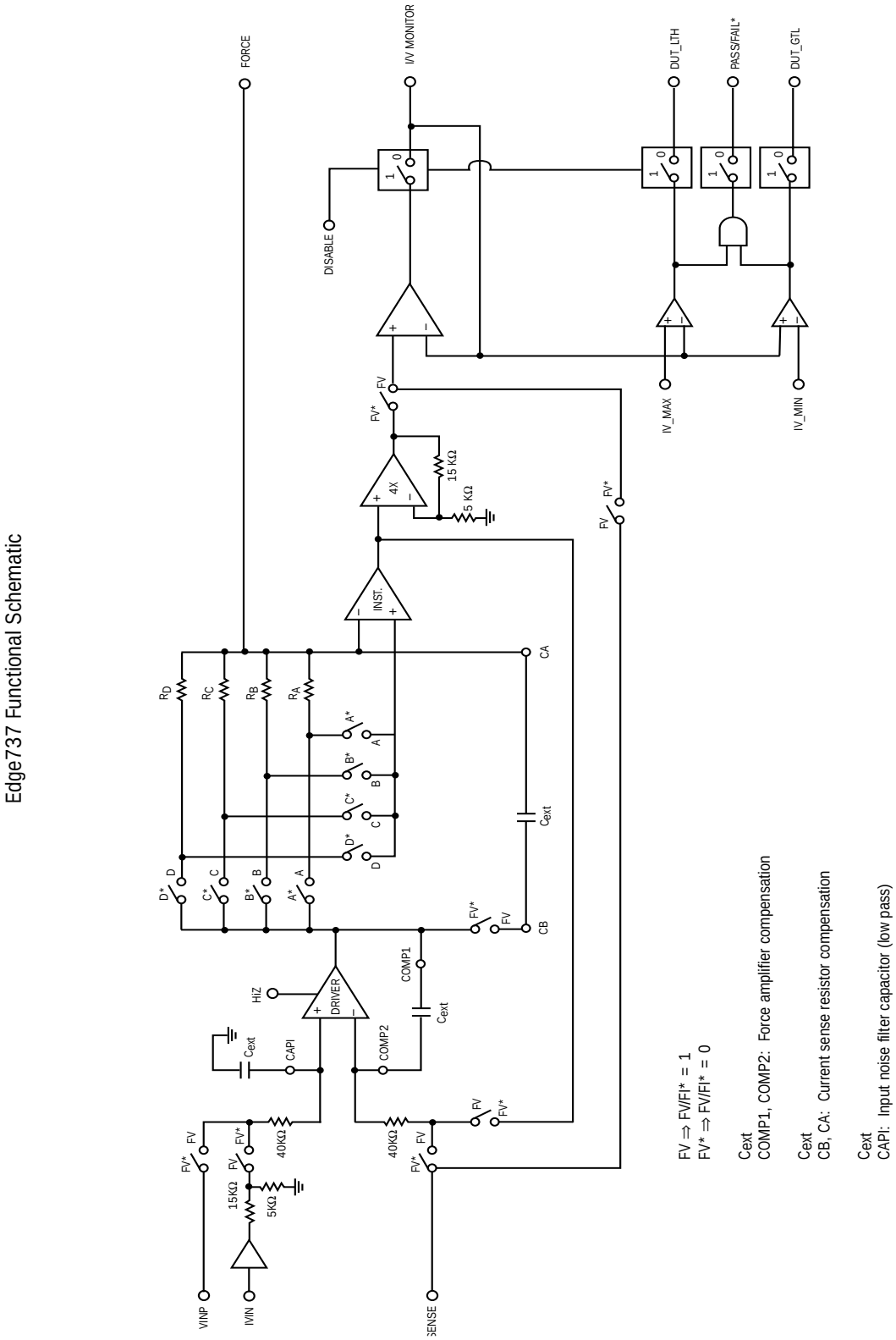


Figure 1. Edge737 Functional Schematic

Circuit Description *(continued)*

TEST CONDITION	DISABLE	DUT LTH	DUT GTL	I/V MONITOR	PASS / FAIL*
X	1	Hi Z	Hi Z	Hi Z	
I/V MONITOR > I/V MAX I/V MONITOR < I/V MAX	0 0	0 1	N/A N/A	I/V MONITOR = Iout * 4.0 * REXT I/V MONITOR = Iout * 4.0 * REXT	0 N/A
I/V MONITOR > I/V MIN I/V MONITOR < I/V MIN	0 0	N/A N/A	1 0	I/V MONITOR = Iout * 4.0 * REXT I/V MONITOR = Iout * 4.0 * REXT	N/A 0
I/V MONITOR < I/V MAX and I/V MONITOR > I/V MIN	0	1	1	I/V MONITOR = Iout * 4.0 * REXT	1

Table 6. FV / MI Truth Table

TEST CONDITION	DISABLE	DUT LTH	DUT GTL	I/V MONITOR	PASS / FAIL*
X	1	Hi Z	Hi Z	Hi Z	
SENSE > I/V MAX SENSE < I/V MAX	0 0	0 1	N/A N/A	I/V MONITOR = SENSE I/V MONITOR = SENSE	0 N/A
SENSE > I/V MIN SENSE < I/V MIN	0 0	N/A N/A	1 0	I/V MONITOR = SENSE I/V MONITOR = SENSE	N/A 0
DUT < I/V MAX and DUT > I/V MIN	0	1	1	I/V MONITOR = SENSE	1

Table 7. FI / MV Truth Table

Circuit Description *(continued)*

REXT Selection

The Edge737 is designed for the voltage drop across RA, RB, RC, and RD to be ≤ 2V with the maximum current passing through them. However, these resistor values can be changed to support different applications.

Increasing the maximum current beyond the nominal range is not recommended. However, decreasing the maximum current is allowed.

Short Circuit Protection

The Edge737 is designed to survive a direct short circuit to any voltage within the supply rails at the FORCE and SENSE pins.

Transient Clamps

The Edge737 has on-board clamps to limit the voltage and current spikes that might result from either changing the current range or changing the operating mode.

Common Mode Error/Calibration

In order to attain a high degree of accuracy in a typical ATE application, offset and gain errors are accounted for through software calibration. When forcing or measuring a current with the Edge737, an additional source of error, common mode error, should be accounted for. Common mode error is a measure of how the common mode voltage, V_{CM}, at the input of the current sense amplifier affects the forced or measured current values (see Figure 2). Since this error is created by internal resistors in the current sense amplifier, it is very linear in nature.

Using the common mode error and common mode linearity specifications, one can see that with a small number of calibration steps (see Applications note PMU-A1), the effect of this error can be significantly reduced.

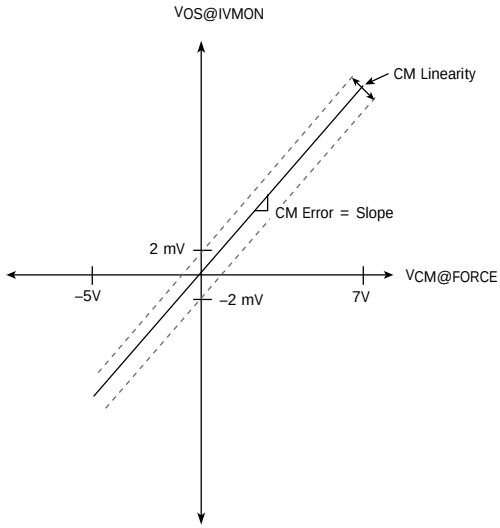


Figure 2. Graphical Representation of Common Mode Error

Compensation Capacitors

COMP1 and COMP2 are internal op amp compensation pins that require a 120 pF capacitor connected between the two pins.

CAPI is an external noise compensation pin that can be used as a low pass filter to eliminate noise from the IVIN and VINP input pins through the connection of an external capacitor from CAPI to GND. The relationship between the roll-off frequency of noise filtered (in Hz) to the external capacitance (in farads) can be seen below:

$$\text{Filter Frequency} = \frac{1}{80{,}000\ \pi\ \text{X}\ C_{CAPI}}$$

CA and CB are internal compensation pins that require a 120 pF capacitor connected between them.

Power Supply Sequencing

The following sequence should be used when powering up the Edge737:

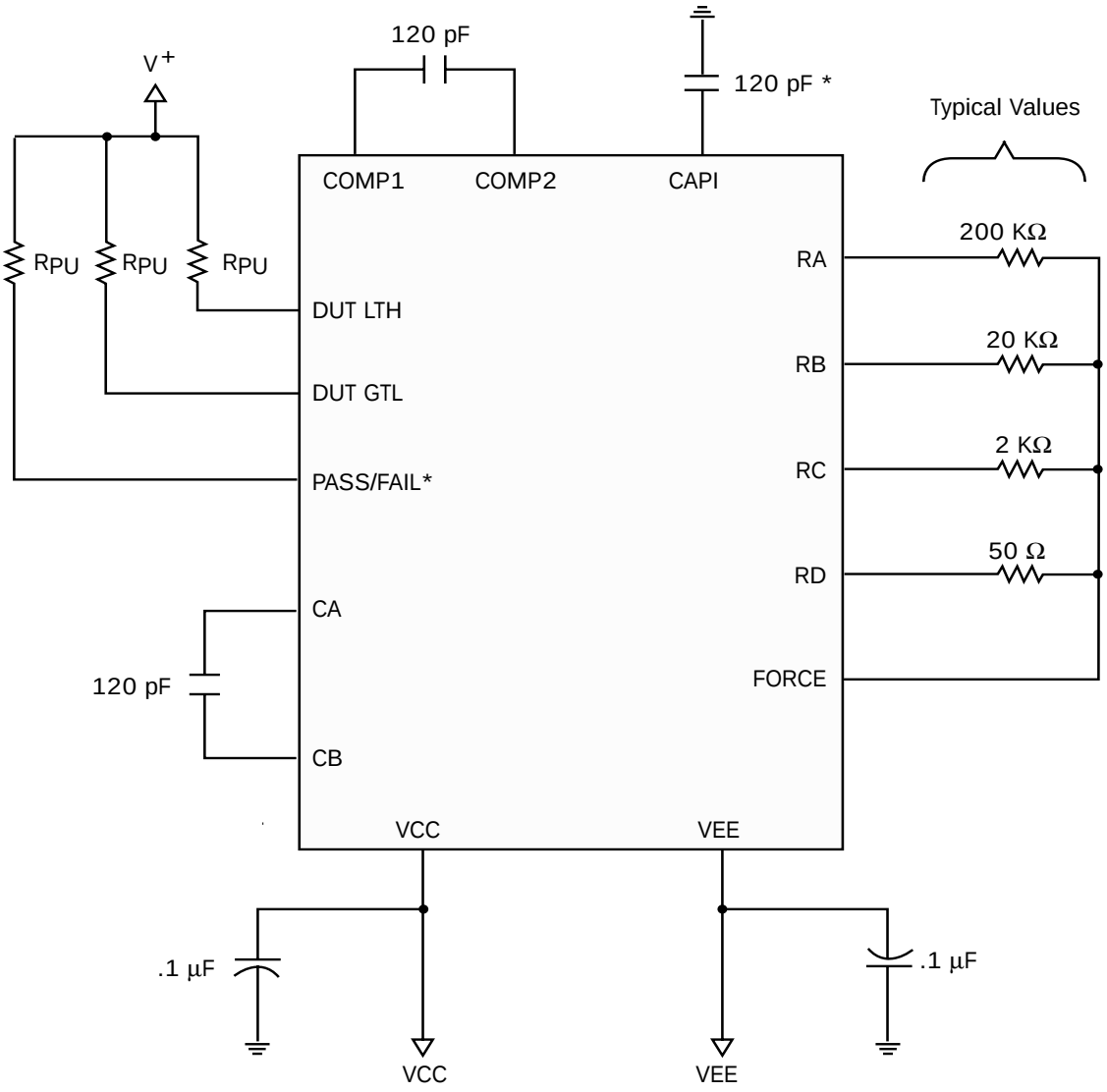
1. VCC
2. VEE

(VCC ≥ All Inputs ≥ VEE at all times)

Application Information

Required External Components

Choose Rext such that:
Iout (low) = $V^+ / R_{PU} < 1$ mA, $V^+ \leq$ VCC



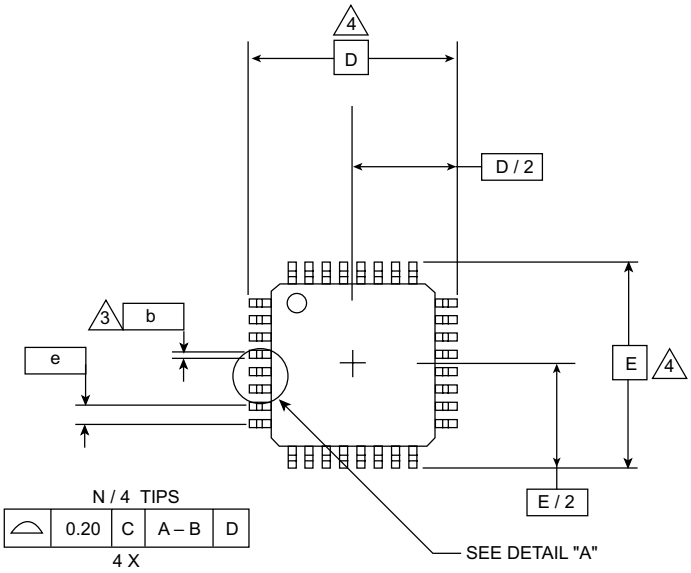
* Optional (see Compensation Capacitors Section)

Actual decoupling capacitor values depend on the actual system environment.

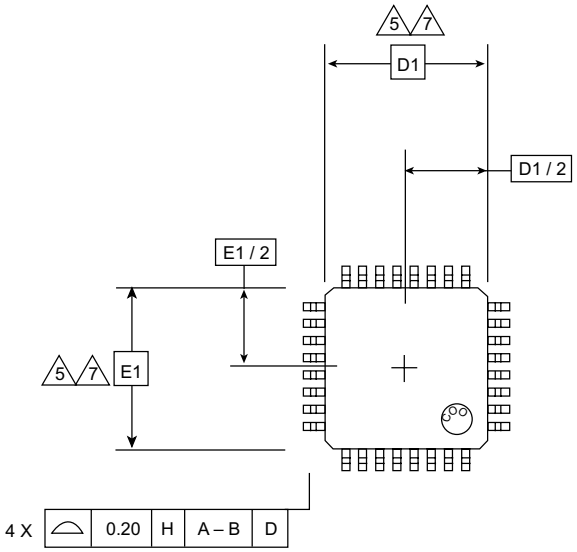
Package Information

32 Pin TQFP Package
7 mm x 7 mm x 1.4 mm

TOP VIEW

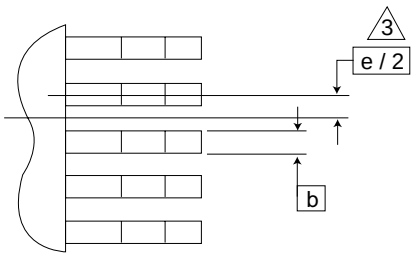


BOTTOM VIEW



Package Information *(continued)*

DETAIL "A"



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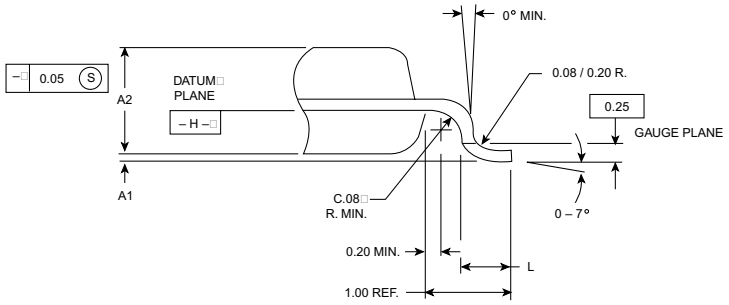
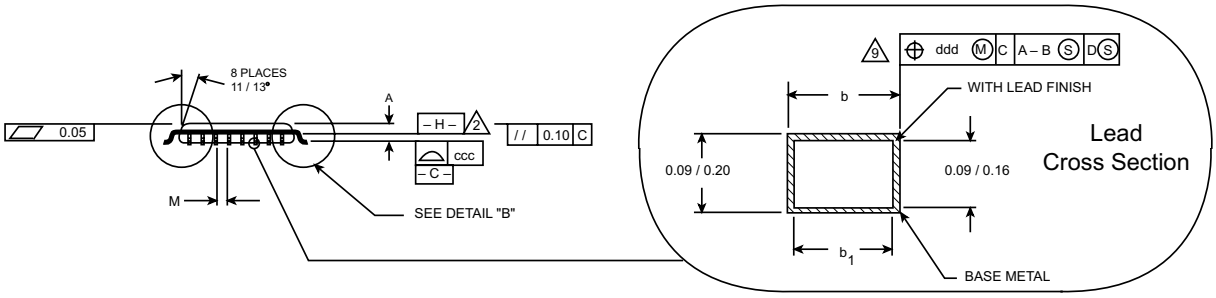


SECTION C–C



Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at centerline between leads where leads exit plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion.
6. "N" is the total # of terminals.
7. These dimensions to be determined at the datum plane -H-.
8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.30 millimeters.
12. This outline conforms to JEDEC publication 95, registration MO-136, variations AC, AE, and AF.

	JDEC Variation Dimensions in Millimeters				
Sym	Min	Nom	Max	Note	Comments
A			1.60		Package Stand Off Height
A1	0.05	0.10	0.15		Air Gap
A2	1.35	1.40	1.45		Package Body Thickness
D		9.00 BSC		4	
D1		7.00 BSC		7,8	Package Body Length
E		9.00 BSC		4	
E1		7.00 BSC		7,8	Package Body Width
L	0.45	0.60	0.765		
M	0.15			5	
N		32			Lead Count
e		0.80 BSC			Lead Pitch
b	0.30	0.37	0.45	9	Lead Thickness
b1	0.30	0.35	0.40		
ccc			0.10		
ddd			0.20		

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Power Supply (Relative to GND)	VCC	11.5	12	13	V
Negative Analog Power Supply (Relative to GND)	VEE	–11	–10	–9.5	V
Total Analog Power Supply	VCC – VEE	21	22	22.5	V
Case Temperature	TC	+25		+75	˚C
Junction Temperature	TJ			+125	˚C
Thermal Resistance of Package (Junction to Case)	θ_{JA}		14.1		˚C/W

Production tested @ +12V, –10V for linearity and min/max parametric testing.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC	0		14.0	V
Negative Power Supply	VEE	–13.0		0	V
Total Power Supply	VCC – VEE	0		23.0	V
Digital Inputs		–.5		7.0	V
Ambient Operating Temperature	TA	0		+125	˚C
Storage Temperature	TS	–55		+150	˚C
Junction Temperature	TJ	–65		+150	˚C
Soldering Temperature				+260	˚C

Stresses above listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

DC Characteristics

Description	Symbol	Min	Typ	Max	Units
Power Supplies					
Power Supply Consumption (no load)					
Positive Supply	ICC	3		11	mA
Negative Supply	IEE	–11		–3	mA
Power Supply Rejection Ratio (up to 1 MHz, Guaranteed by Design and Characterization)	PSRR			20	dB
Force Voltage / Measure Current Mode					
Input Voltage Range @ VINP	VINP	VEE + 4		VCC – 4	V
Input Bias Current @ VINP	IBIAS	–0.4		0.4	µA
Capacitive Loading Range @ FORCE for Stability	C_{FORCE}	0		TBD	nF
Output Forcing Voltage Range	V_{FORCE}	VEE + 4.5		VCC – 4.5	V
Forcing Voltage Accuracy (@ FORCE)					
Offset (VINP = 0V, no load)	VOS	–100		100	mV
Linearity	FV INL	–0.083		0.083	% FSVR
Gain Error	FV Gain Error	–0.015		+0.015	V/V
FORCE/SENSE Combined Leakage Current in HiZ Mode	I_{LEAK}	TBD		TBD	TBD
Compliance Current Measurement Range					
Range A		–10		10	µA
Range B		–100		100	µA
Range C		–1		1	mA
Range D		–40		40	mA
Current Measurement Accuracy (@ I/V MONITOR)					
Offset	VOS	–400		400	mV
Linearity	MI INL	–0.122		0.122	% FSCR
Gain Error	MI Gain Error	TBD		TBD	
Common Mode Error	CM Error	–4.3		4.3	mV/V
Common Mode Linearity	ΔCM Error	–.9		–.9	mV
I/V MONITOR Output Leakage Current in Disable Mode	I_{LEAK}	TBD		TBD	µA
I/V MONITOR Output Current Range	$I_{I/V\ MONITOR}$			TBD	TBD
Capacitive Loading Range @ I/V MONITOR	$C_{I/V\ MONITOR}$			TBD	TBD

DC Characteristics *(continued)*

Description	Symbol	Min	Typ	Max	Units
Force Current / Measure Voltage Mode					
Input Voltage Range @ IVIN	IVIN	VEE + 1.0		VCC – 3.0	V
Input Bias Current @ IVIN	IBIAS	–0.4		0.4	µA
Capacitive Loading Range @ FORCE for Stability	C_{FORCE}	0		TBD	nF
Output Forcing Current	I_{FORCE}				
Range A		–10		10	µA
Range B		–100		100	µA
Range C		–1		1	mA
Range D		–40		40	mA
Forcing Current Accuracy (@ FORCE)					
Offset	IOS	–4		4	% FSCR
Gain Error	FI Gain Error	TBD		TBD	% FSCR
Linearity @ FORCE = –5V to 7V	FI INL	–0.35		0.35	% FSCR
Common Mode Error	ICM Error	–0.7		0.7	% FSCR/V
Common Mode Linearity	Δ CM Error	–0.1		0.1	%FSCR
FORCE/SENSE Combined Leakage Current in HiZ Mode	I_{LEAK}	TBD		TBD	TBD
Compliance Voltage Range	$V_{COMPLIANCE}$	VEE + 4.5		VCC – 4.5	
Voltage Measurement Accuracy (@ I/V MONITOR)					
Offset	VOS	–100		100	mV
Gain Error	MV Gain Error	TBD		TBD	TBD
Linearity	MV INL	–0.025		0.025	% FSVR
I/V MONITOR Output Leakage Current in Disable Mode	I_{LEAK}	TBD		TBD	µA
I/V MONITOR Output Current Range	$I_{I/V\ MONITOR}$			TBD	TBD
Capacitive Loading Range @ I/V MONITOR	$C_{I/V\ MONITOR}$			TBD	TBD
Comparator					
Input Voltage Range (I/V MIN, I/V MAX)	VIN	VEE + 1		VCC – 3	V
Input Offset Voltage	VOS	–100		100	mV
Input Bias Current (I/V MIN, I/V MAX)	IIN	–0.4		0.4	µA
Output Low Level @ IOL = 1 mA (DUT LTH, DUT GTL, PASS/FAIL*)	VOL			400	mV
Output Leakage in DISABLED Mode	IOH			100	µA
Output Leakage	I_{LEAK}			TBD	µA
DISABLE Input Bias Current	IIN	–0.2		0.2	µA

DC Characteristics *(continued)*

Description	Symbol	Min	Typ	Max	Units
Analog MUX (RS1, RS2)					
Input High Level	VIH	2.4			V
Input Low Level	VIL			0.8	V
Input Bias Current	IIN	–0.2		0.2	µA
Other Digital Inputs					
Input High Level (MODE SEL, HIZ)	VIH	2.4			V
Input Low Level (MODE SEL, HIZ)	VIL			0.8	V
MODE SEL Input Bias Current	IIN	–0.2		0.2	µA
HIZ Input Bias Current	IIN	–0.2		50	µA

DC Test Conditions: CAPI = 120 pF connected to GND, CA – CB = 120 pF, COMP1 – COMP2 = 120 pF, TA = 25˚C unless otherwise noted.

Unit Definitions:
FSCR = Full Scale Current Range
Range A, FSCR = 20 µA
Range B, FSCR = 200 µA
Range C, FSCR = 2 mA
Range D, FSCR = 80 mA
FSVR = Full Scale Voltage Range = 12V nominal (–5V to 7V)

AC Characteristics

Description	Symbol	Min	Typ	Max	Units
Force Voltage / Measure Current Mode					
FORCE Voltage Settling Time (All Ranges) (Note 1) 100 pF Load @ FORCE	t_{settle}			TBD	TBD
FORCE Amp Saturation Recovery Time	t_{sat}			TBD	TBD
Disable Time, HiZ Low to High	t_z			TBD	µs
Enable Time, HiZ High to Low	t_{oe}			TBD	µs
Force Current / Measure Voltage Mode					
FORCE Output Current Settling Time (All Ranges) (Note 2) 100 pF Load @ FORCE	t_{settle}			TBD	TBD
FORCE Amp Saturation Recovery Time	t_{sat}			TBD	TBD
Disable Time, HiZ Low to High	t_z			TBD	ns
Enable Time, HiZ High to Low	t_{oe}			TBD	ns
Comparator					
Propagation Delay	t_{pd}			20	ns
Disable Time, DISABLE Low to High	t_z			20	ns
Enable Time, DISABLE High to Low	t_{oe}			20	ns
I/V MONITOR					
Output Settling Time (All Ranges) (Note 3) 100 pF Load @ I/V MONITOR	t_{settle}			TBD	TBD
Disable Time, DISABLE Low to High	t_z			40	ns
Enable Time, DISABLE High to Low	t_{oe}			40	ns
Mode/Range Selection					
MODE SEL Propagation Delay	t_{pd}			TBD	TBD
RS0/RS1 Propagation Delay	t_{pd}			TBD	TBD

AC Test Conditions: CAPI = 120 pF connected to GND, CA – CB = 120 pF, COMP1 – COMP2 = 120 pF, TA = 25˚C unless otherwise noted.

Settling times guaranteed by design and characterization (not production tested).

Note 1: FORCE voltage settling times are measured using a TBD V step to TBD % accuracy.
Note 2: FORCE current settling times are measured using a TBD V step to TBD % accuracy.
Note 3: I/V MONITOR settling times are measured using a TBD V step to TBD % accuracy.

Ordering Information

Model Number	Package
E737ATF	32-Pin TQFP 7 mm x 7 mm
EVM737ATF	Edge737H Evaluation Module

This device is ESD sensitive. Care should be taken when handling and installing this device to avoid damaging it.

Contact Information

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High-Performance Division
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Phone: (858)695-1808 FAX (858)695-2633

Revision History

Current Revision Date: January 14, 2002
Previous Revision Date: October 23, 2001

Page #	Section Name	Previous Revision	Current Revision
2	Pin Description	DISABLE … outputs in high impedance.	DISABLE … outputs and I/V MONITOR in high impedance.
5	Circuit Description	DISABLE Section … which places DUT LTH, DUT GTL, and PASS/FAIL* …	DISABLE Section … which places DUT LTH, DUT GTL, I/V MONITOR, and PASS/FAIL* …
6	Circuit Description		Replace Detailed Block Diagram with Functional Schematic
12	Recommended Operating Conditons	Ambient Operating Temperature, Symbol: TA Thermal Resistance (Junction to Still Air), Typ: 92.4	Case Temperature, Symbol: TC Thermal Resistance (Junction to Case, Typ: 14/4 *Add:* Thermal Resistance of Package *Add:* Capacitive Loading Range @ I/V MONITOR
13, 14	DC Characteristics		*Add:* Capacitive Loading Range @ FORCE for Stability *Add:* FORCE/SENSE Combined eakage Current *Add:* Compliance Current Measurement Range *Add:* Compliance Voltage Range *Add:* I/V MONITOR Output Leakage Current in Disable Mode *Add:* I/V MONITOR Output Current Range *Add:* DC Test Conditions *Add:* Capacitive Loading Range @ I/V MONITOR
14	DC Characteristics	Input High Level, Min: 2	Input High Level, Min: 2.4
16	AC Characteristics		New Table

Current Revision Date: October 23, 2001
Previous Revision Date: September 27, 2001

Page #	Section Name	Previous Revision	Current Revision
12	DC Characteristics	 Input Voltage Range @ IVIN, Min: VEE + 1.5, Max: VCC – 3.5	Force Voltage/Measure Current and Force Current/Measure Voltage Modes *Add:* Output Leakage Current in HiZ *Add:* Symbol info for Linearity & Gain Error Input Voltage Range @ IVIN, Min: VEE + 1.0, Max: VCC – 3.0
13	DC Characteristics		Output Leakage - add symbol info
14	AC Characteristics		*Delete:* Measured Current Settling Time *Add:* Disable Time and Enable Time specs
15			*Add*: ESD Note